2022-09-22

Investigating Inverter Efficiency at Low Power for LED Lighting

Ahmed, Syed Kaiser

UNIVERSITY OF CALGARY

Investigating Inverter Efficiency at Low Power for LED Lighting

by

Syed Kaiser Ahmed

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE

DEGREE OF MASTER OF SCIENCE

GRADUATE PROGRAM IN ELECTRICAL ENGINEERING

CALGARY, ALBERTA

SEPTEMBER, 2022

Abstract

With the industrialization of society, concerns about the environment have led to the development of renewable energy approaches. Efforts are underway to provide renewable energy in remote villages, including the use of photovoltaic energy. An issue with a battery based photovoltaic energy system for a village residence is the efficiency of the DC to AC power inverter. A sub issue, not well addressed in the literature, is inverter efficiency at low power, such as the operation of a single LED light at night. It is proposed in the literature that efficiency can be increased with the use of a very low switching frequency of the inverter power transistors. A 200W MOSFET Full Bridge inverter is modelled and characterised for operation down to 3.5 W with a switching frequency of 200Hz. Using a SimuLink simulation, it is found that inverter efficiency can be increased from 59% to 77% employing this approach.

Acknowledgements

First and foremost, I would like to thank Allah for His showers of blessings throughout my research work to complete my thesis successfully. Thank you, our dear beautiful all-loving Allah, for being so close by, always, with every step we take, and for sending your angels to guide us, on our journey together aboard spaceship earth.

I would like to express my special thanks and sincere gratitude to my supervisor, Dr. Ed Nowicki, brother Ed, for providing invaluable guidance throughout the research and thesis writing period. It was a great honour to work with you brother Ed. You have taught me how to do research, how to present my work to others and much about life. I would like to extend my gratitude to your wonderful wife Elke and your children Sophia, Peter and Chris for the friendship, support, empathy and especially for the fresh brown eggs from your chickens.

And I wish to thank my brothers and sisters in the Masjid for your help and shelter during challenging times. I will always be grateful for everything you have done, especially brother Zaid for assisting me in finding employment.

I also wish to express my appreciation to the undergraduate students, graduate students, professors and staff in the Department of Electrical and Software Engineering. Your ongoing support through turbulent times is much appreciated. In particular I wish to thank Dr. Majid Pahlevani, Dr. Babak Roodsari, and my good colleagues Eric and Amir. And also, I express my sincere appreciation to the oral examination professors, Dr. Abu Sesay and Dr. Ignacio Galiano Zurbriggen. Your review of my thesis and your feedback are most appreciated.

Dedication

I dedicate this thesis to my numerous friends and family. My friend Maaz, you and your family are very treasured in my memory and you have never left my mind and heart. I also dedicate this thesis to my friends and family who have suffered and are no longer on this earth. I pray for your safe travels in that world above us.

Table of Contents

List of Tables

List of Figures

List of Abbreviations, and Nomenclature

AC	Alternating Current
Ah	Amp hour
CFL	Compact Fluorescent Light
CSI	Current Source Inverter
DC	Direct Current
DCMLI	Diode-Clamped Multi-Level Inverter
FBI	Full Bridge Inverter
HBI	Half Bridge Inverter
HFT	High-Frequency Transformer
IGBT	Insulated Gate Bipolar Transistor
LED	Light Emitting Diode
LC	Inductor Capacitor
LLC	Inductor Inductor Capacitor
MOSFET	Metal Oxide Field Effect Transistor
MPPT	Maximum Power Point Tracking
MSPC	Multi-Stage Power Converter
MLI	Multi-Level Inverter
PRC	Parallel Resonant Converter
PSpice	Personal Computer Simulation Program with Integrated Circuit Emphasis
RMS	Root Mean Square
PI	Proportional Integral
PV	Photovoltaic
SEPIC	Single-Ended Primary-Inductor Converter
SPRC	Series-Parallel Resonant Converter
SPWM	Sinusoidal Pulse Width Modulation
SRC	Series Resonant Converter
THD	Total Harmonic Distortion
SSPC	Single Stage Power Converter
TSPC	Two-stage Power Converter

VAC	RMS AC Voltage rating
VSI	Voltage Source Inverter

Chapter 1: Introduction

1.1 THESIS OVERVIEW

With global concerns about energy security and the impact on our environment by industrialization of society (and associated disparities), greater attention is being given to renewable energy, including solar photovoltaic (PV) energy. In particular, for the PV system of a remote village residence, selecting the appropriate power inverter (i.e., a DC to AC power converter) significantly impacts the system's overall performance. In recent decades, tremendous improvements have emerged in the power electronics sector to reduce cost and improve performance. In general, many inverter configurations have been developed to integrate various distinctive features to meet PV system requirements, such as inherent boost characteristics, high energy efficiency, proper energy decoupling, twin grounding, single-stage photovoltaic transformation abilities, modular layout, and proper power consistency, for both off-grid and gid-connected systems (Tazay, 2017). However, one performance characteristic has been neglected in the quest for greater efficiency, impacting inexpensive rural PV systems. That performance characteristic is the inverter efficiency at low power levels. Low efficiency at low power levels is inherent in most power conversion devices. Consider a simple construction iron-core transformer. At low power levels, the full rated voltage is usually present on the windings, and though copper losses are low, the core losses can be significant. In many applications, low efficiency at low power is not a concern or is tolerated since the total energy loss is not significant over a 24-hour period. However, one might imagine a situation where low power inefficiency is a concern in rural PV systems. For example, a village

home where a single outdoor light is powered at night by the PV system. In a rural application, especially in the developing world, the low capital cost of the PV system is important. Thus, a battery is sized to be as small as possible. As a result, a single lightbulb operating all night long can significantly drain the battery. The research underlying this thesis regards improving inverter efficiency at low power levels through transistor switching frequency variation, as an extension of the research by (Loba, 2015) and (Loba et al., 2015).

In this chapter, some background related to solar PV power and inverter systems is presented in Section 1.2. Presented in Section 1.3 is the objective of this thesis study. Section 1.4 provides a discussion of the contribution of the research underlying this thesis, and the scope of the research is presented in Section 1.5. The last section, 1.6, of this chapter outlines the thesis structure and the layout of the chapters.

1.2 BACKGROUND

Solar photovoltaic energy is increasingly emerging as a suitable source of renewable energy among all alternative energy resources due to its advantages such as availability of solar energy, low greenhouse gas emissions, no moving or rotating components, minimal maintenance, low noise, lower operating costs, and high adaptability (US Energy Information Administration, 2020). In addition, most governments provide subsidies or tax concessions. Also, for distributed power production, PV solutions provide additional flexibility. In many cases, with electricity generation close to the load point, the transmission losses are minimised.

For grid-connected systems, it is common practice to increase PV system performance by implementing the Maximum Power Point Tracking (MPPT) method. With MPPT, the PV module is operated at a point on its characteristic IV curve, i.e., the current vs. voltage output characteristic,

such that the product of current and voltage is at a maximum. As a result, MPPT operation leads to the greatest energy harvest. In the case of a residence, excess power is injected into the grid. This thesis is not concerned with grid-connected PV systems. In off-grid situations, PV system performance and longevity are highly dependent on proper battery management. In particular, a high state of charge or a low state of charge can deteriorate battery lifetime.

A common interest for researchers and designers of PV systems, grid-connected or not, is the efficiency of the PV system. Interestingly, the PV modules' efficiency is relatively low (commercial PV modules range in efficiency from about 10% to 22%). This contrasts with the inverter efficiency. For a residential PV system, the inverter efficiency is typically on the order of 90% to 97% over a wide range of power settings. Figure 1-1 is a typical efficiency plot for an inverter intended for residential applications in North America, based on the author's experience and reading of the literature. Note, as shown in Figure. 1-1, the efficiency of a power inverter drops dramatically for power output below approximately 10% of the inverter's rated power output.

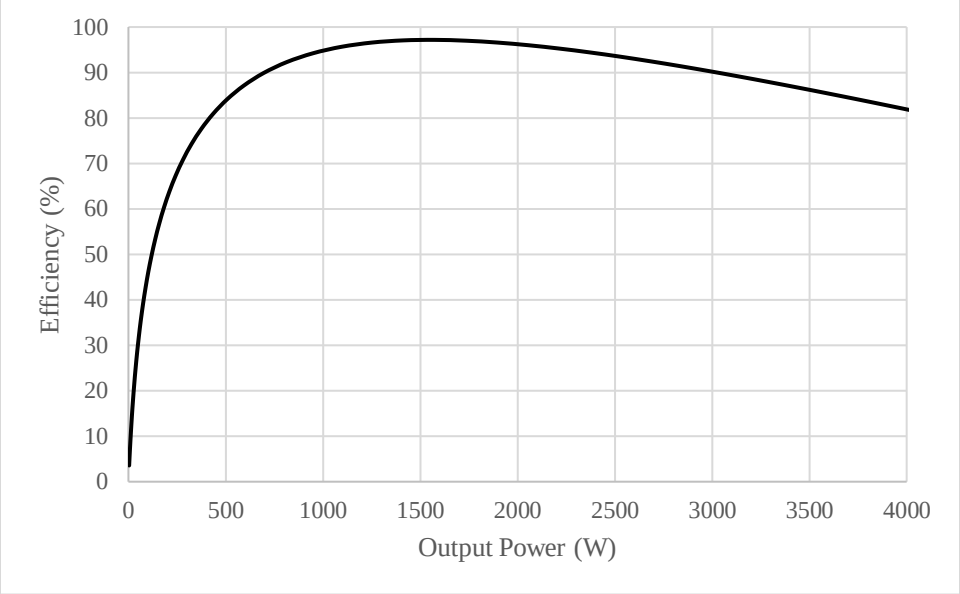


Figure 1-1 Typical efficiency curve for a residential power inverter (rated 4000W)

As noted above, this thesis is concerned with inverter operation at low power levels, i.e., well below 10% of the rated power output. If a residential off-grid PV system operates at low power for several hours (such as overnight operation), given existing commercial inverters, the low efficiency can significantly drain the battery state of charge. This thesis examines a power transistor switching scheme for the inverter to enhance the inverter efficiency at low power.

1.3 OBJECTIVE OF THE THESIS

The objective of the thesis is to investigate transistor switching of an inverter for very low power operation, namely, with a power output of 3.5W, for a 200W rated Full Bridge inverter. The 200W full power rating is selected as a typical value for a remote village home.

The rationale is that commercial LED (light emitting diode) lights have become much more efficient in recent years, even more efficient than CFLs (compact fluorescent lights). For example (a running example in this thesis), a single LED lightbulb that consumes 3.5W of power (commercially available for 120Vrms 60Hz or 220Vrms 50Hz AC grid systems) is designed to replace a 9W CFL. That 9W CFF itself, was designed to replace the older tungsten filament lightbulb with a power consumption of 40W. If an inverter is rated for an output of 200W, the operation of a single 3.5W LED lightbulb will correspond to a 1.75% power operating point.

The research underlying this thesis is an extension of the research performed by Tahsina Hossain Loba, where a low power switching method was introduced for a power output of 9W (to operate a single CFL) from a 200W rated inverter (Loba, 2015) (Loba et al., 2015). A power inverter, rated at 200W, is also the basis for the research study in this thesis, as it might be used in a single residence in a remote village where grid power is not available. One distinction of this thesis compared to the research of Loba is that an even lower power operation is examined in this thesis,

i.e., 3.5W here, compared to 9W in the study performed by (Loba, 2015). Another distinction is that Loba employed IGBT devices, however, the principle of reduced losses at low switching frequency also applies to MOSFET devices which are employed in this thesis.

1.4 CONTRIBUTION OF THE THESIS

The main contribution of the thesis is a characterisation of inverter efficiency at very low power output, i.e., with a benchmark power output of 3.5W as would be required for a single modern LED lightbulb (this is a value of 1.75% of the rated inverter power output of 200W). Such knowledge may be instrumental in improving PV system design for single-residence remote village photovoltaic power systems. With improved overall efficiency of the PV system, battery sizing may be decreased and thus total system cost reduced and potential negative impact on the environment mitigated. In addition to inverter low power characterisation, the first stage DC to DC converter is modelled as a Push Pull converter to provide a more realistic DC link voltage applied to the power inverter under study.

1.5 SCOPE OF THE THESIS

In this study, the transistor switching frequency is reduced to enhance inverter efficiency for low power operation, as was also done by Loba (2015). A major loss component of inverter operation at low power is the on/off switching the power transistors in the inverter, which is a function of the switching frequency, the DC-link voltage, and the current flowing through the switching device. For commercial inverters, the switching frequency is chosen by balancing the need for high efficiency, sinusoidal output power quality, and low cost. A cursory analysis might suggest that low power operation implies less current, which means less I^2R loss, as is indeed the case.

However, the switching losses become more significant, i.e., not dropping as fast as I^2R losses, as the load level decreases. That is to say, improving inverter efficiency at low power would be benefitted by reduced switching loss at low power.

As with (Loba, 2015), it is suggested in this thesis that the switching frequency is lowered to enhance inverter efficiency at low power. While operating at a lower switching frequency, inverter output characteristics and power quality are also considered. Although the lower switching frequency reduces power quality, it is believed that most home loads will handle the degradation, including the operation of a single LED lightbulb. This assumption is based on the operation of previous generation 12V DC to 120VAC inverters where the load waveform was a modified square wave having significant distortion (on the order of 30%).

The following are included in the scope of this thesis:

1. Evaluation of the inverter loss and efficiency based on a model including on resistance for the Metal Oxide Field Effect Transistor (MOSFET) switching devices employed in the Full Bridge (also called H Bridge) inverter.
2. Simulation of the inverter performance using the commercial software, SimuLink, to characterise the losses in the inverter and the distortion of the load voltage waveform.
3. Exploration of the feasibility of employing a low switching frequency in the inverter, as low as 200Hz, for operation of a single 220VAC 3.5W LED light (as might be used outside a village home at night).

The following are beyond the scope of this thesis:

1. LED operation and lifetime, as related to inverter output voltage distortion.
2. A detailed model of the 220VAC LED is not constructed, due to the lack of information on such modelling, hence a pure resistive load is employed.

3. All power transistors are modelled with an on resistance however capacitive effects (gate to source, gate to drain, drain to source) are not modelled.
4. A very different approach to that of this thesis would be the design of a separate power converter, rated at 3.5W, purely for the purpose of operating a single LED light. This approach, although reasonable, was not pursued in this thesis study.

1.6 THESIS OUTLINE

The thesis has been organised in the following structure:

Chapter 1 provides a broad overview of the thesis, as presented above. Chapter 2 contains an extensive literature overview of power inverter circuits investigated in the academic community, including multilevel and multisource inverters (although such inverters are generally found only in high power applications, these serve to provide some context for the variety of inverter structures employed in PV applications). Discussed in this chapter also are the Half Bridge and Full Bridge (also called H Bridge) inverters and as well as the Push Pull based inverter, all of which are examined for possible study in this thesis. Chapter 3 provides a discussion of the methodology employed in the thesis, including the system description. The simulation results are given in Chapter 4, including typical waveforms obtained from the SimuLink model and efficiency values from the steady state SimuLink simulations. A thesis summary, conclusion and possible future work are presented in Chapter 5.

Chapter 2: Literature Review

2.1 INTRODUCTION

Regarding recent global concerns about environmental threats and the potential of new energy sources to reduce greenhouse gas effects, the implementation of renewable energy systems is becoming more and more widespread. Although many studies have been done on photovoltaic systems related to performance and efficiency, minimal research has been done on PV systems with a wide range of power demands, especially for low power consumption.

In most cases, a residential off-grid PV system has a topology where subsystem components (PV module, DC charge controller, battery, inverter) are connected in tandem. Thus, overall efficiency can be found by multiplying the efficiencies of each subsystem. The power inverter, from an installer's perspective, is often considered a high efficiency subsystem commodity. However, as discussed in Chapter 1, at very low power levels, a commercial inverter has very low efficiency, as is addressed in this thesis. In this chapter a literature review of inverter topologies and operation modes is presented.

In this chapter, Section 2.2 presents a discussion of inverter topology classifications, with some added discussion about modulation control of transistor switches. In Section 2.3, multi-stage inverter topologies are reviewed in some detail, while the more common single-stage inverter topologies are discussed in Section 2.4 (the single-stage Full Bridge inverter is chosen for study in this thesis, which is also referred to as an H Bridge inverter). Presented in Section 2.5 is a discussion regarding switch implementation, emphasizing the parallel switch method. The final

section, Section 2.6 provides a discussion about transistor switching frequency, which is related to the reduced switching frequency approach that is implemented in the research work of this thesis and discussed in further detail in Chapter 3.

2.2 CLASSIFICATION OF INVERTER TOPOLOGIES

DC to AC power converter technologies (i.e., inverter topologies) are currently employed for systems with a power rating from a few Watts to Mega Watts. In a renewable energy system, the energy sources, such as solar or wind, may have an intermittent nature. However, the electrical loads in a home require continuous, smooth and uninterrupted power (Ansari et al., 2018). Hence, it is common practice to include a battery in remote PV systems where there is no access to a power grid. For the inverter topologies and operating modes discussed in this chapter, it is assumed that the inverter input power is provided by a battery or PV panel.

The classification of inverters might seem a complicated task. However, according to the arrangement of power transistor switches in the core of the inverter circuit, they can be divided into the Half Bridge class and the Full Bridge class (Tekgun et al., 2018). Shown in Figure 2-1 is the basic Half Bridge inverter (HBI) circuit, and shown in Figure 2-2 is the basic Full Bridge inverter (FBI) circuit. Note that the Half Bridge inverter requires a split DC input power source. If the DC source does not have a centre tap, then a split DC source is occasionally created by placing two electrolytic capacitors in series across the single-ended DC source. Switch control of the inverter in this situation requires attention to the charge on the capacitors in order to maintain an equal voltage on each capacitor. The Half Bridge inverter is sometimes used for very small inverters (rated up to say 100W). However, with dropping costs of power transistors, even small inverters are often implemented with the Full Bridge topology.

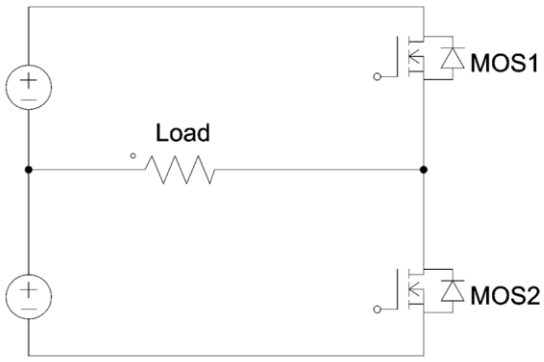


Figure 2-1 The basic Half Bridge inverter topology

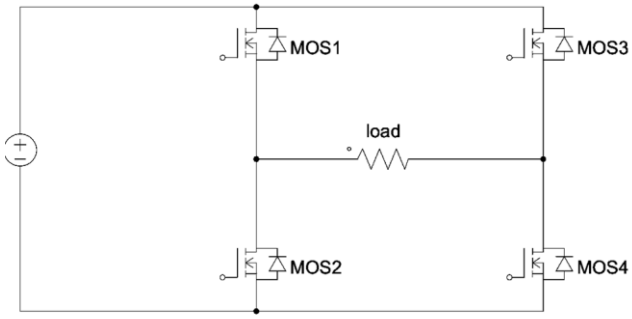


Figure 2-2 The basic Full Bridge inverter topology

It should be noted that classifying inverters as either Half- or Full Bridge is an oversimplification of the classification of inverter topologies. There are in fact a wide range of circuit layouts (i.e., circuit topologies) among commercial inverters. Shown in Figure 2-3 is one such classification. A discussion now follows about these classifications shown in Figure 2-3.

A simple inverter layout may consist of just the Half Bridge or just the Full Bridge, either of which would be an example of a single stage inverter. Or two or more circuits can be connected in a wide variety of ways to form a multi-stage inverter (such is the case for example in High Voltage DC lines regarding the inverters located in the DC to AC substation). Soft-switching refers to power transistor gating control where the transistor on-current is gradually increased following turn-on, or where the transistor off-voltage is gradually increased following turn-off. For hard-switching,

such gating control is not used. An isolated inverter includes a transformer within the circuit, providing galvanic isolation between inverter input and output terminals. While non-isolated inverters do not have galvanic isolation. The next column of categories of inverters, shown in Figure 2-3, refer to the number of inverters in the system. If only one inverter is used, this is referred to as a central inverter, and at the other extreme, if each individual PV module has its own power inverter, the inverter is referred to as a microinverter. A two-level inverter has two voltage levels (for example, the positive battery voltage and the negative battery voltage) across the bridge output terminals, whereas a Multi-Level inverter has three or more voltage levels. The last column of categories of inverters, shown in Figure 2-3, has been discussed briefly in Chapter 1, where a grid-connected inverter has its output terminals connected to the electrical power grid, while an off-grid inverter has no such connection.

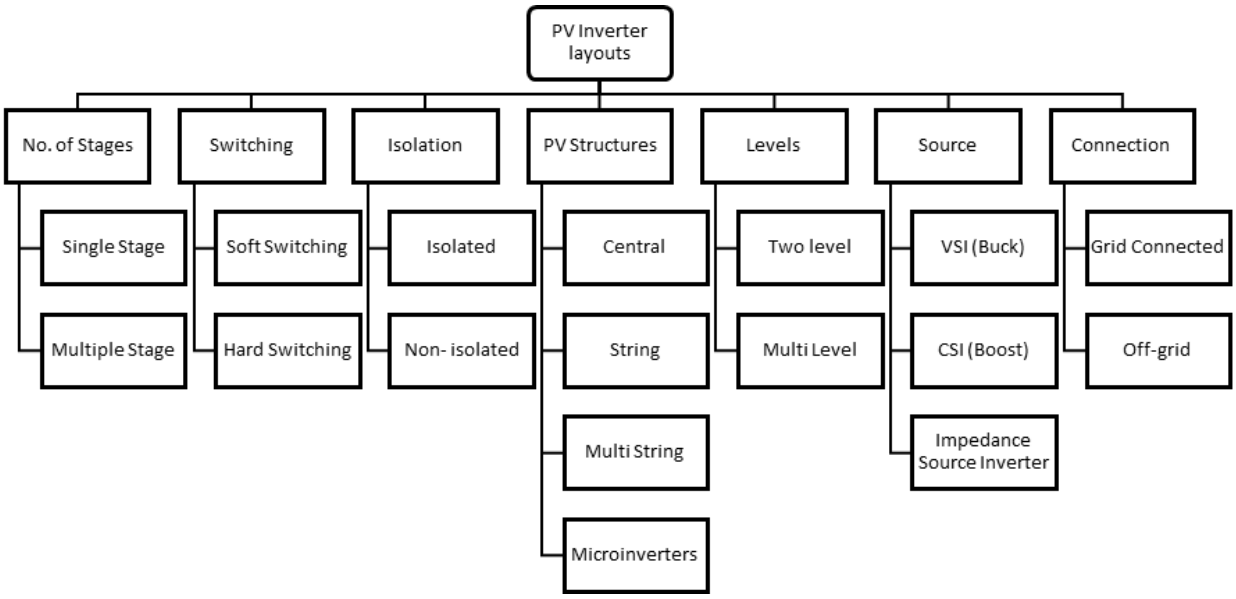


Figure 2-3 PV inverter classifications
(Dogga & Pathak, 2019) (Faraji et al., 2017) (Khan et al., 2020) (Shawky et al., 2020)

Before moving into a deeper discussion about inverter topologies, it is worthwhile to briefly discuss transistor control. Regardless of inverter topology, a common transistor control method is

Sinusoidal Pulse Width Modulation (SPWM) (Liu et al., 2019). Several studies have been done for improving the SPWM strategies in a wide range of implementations in Full Bridge inverters, including applications for AC motors and even in the telecoms field. SPWM can be accomplished by comparing a sinusoidal reference voltage to a triangle carrier signal (sometimes referred to as Natural SPWM). An illustration of Natural SPWM waveforms is shown is Figure 2-4.

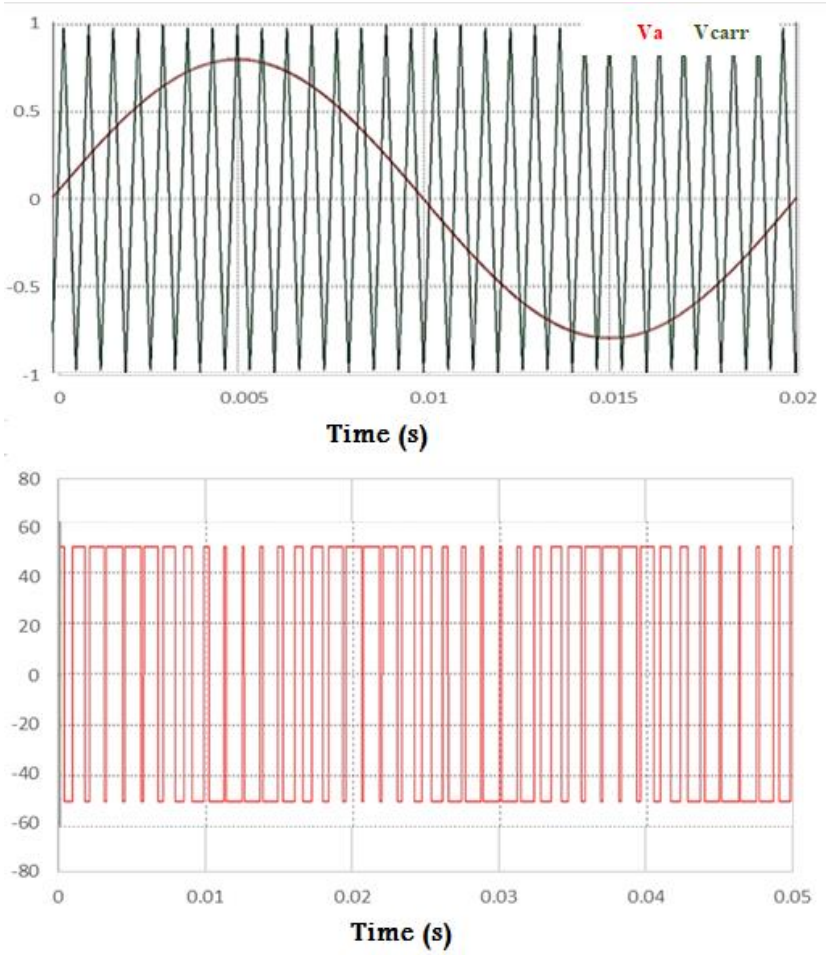


Figure 2-4 Illustration of waveforms for sinusoidal modulation with a triangular carrier in the case of bipolar Natural Sinusoidal Pulse Width Modulation (SPWM).

The upper plot in Figure 2-4 shows the sinusoidal reference waveform (the Va waveform) and tirangular carrier waveform (Vcarr). The lower plot illustrates the bridge output voltage waveform in the case of a 50V DC input voltage for a Full Bridge inverter (the choice of 50V is purely for illustration purposes). Note how the resulting bridge output voltage is switched at the times when the sinusoidal reference voltage intersects the triangular carrier voltage. Note also that the lower plot in Figure 2-4 is a bipolar waveform (since the voltage is switched between two levels: the positive DC voltage level and the negative DC voltage level). This waveform is seen across the terminals of the the Full Bridge output (i.e., across the resisrtor of Figure 2-2). Bipolar PWM is the simplist form of PWM, although it is not a difficult matter to improve the PWM by the use of unipolar PWM, where the Full Bridge output voltage waveform is switched between zero volts and the DC voltage during each half cycle of the power waveform (see for example, Figure 4-3). Note in Figure 2-4 that the lower waveform is similar to the switching signal used to control power transistors in the Full Bridge inverter. The voltage waveform that is seen across the bridge output terminals resembles the switching signal, which becomes almost sinusoidal after filtering with inductor and/or capacitor components (as is usually needed for the load).

When choosing an inverter unit, two factors should be addressed. These factors are the distortion of the load voltage waveform (the closer to a pure sinusoid, the better) and the unit's efficiency. The size of the filter and the PWM strategy are linked to efficiency. One strategy, is the use of unipolar PWM to allow the output LC filter to be slightly smaller than in the case of bipolar PWM (note again that the modulation technique illustrated in Figure 2-4 is bipolar PWM, and with slight modification to the gating pattern, unipolar PWM can be employed as is done in this thesis). Further details about these two factors are discussed in Chapters 3 & 4.

2.3 MULTI-STAGE INVERTER CONVERTER CIRCUITS

In this section, multi-stage inverters are discussed. The inverters in the following discussion were considered as candidates for investigation, however they were ruled out eventually, often based on the complexity and corresponding high cost that would not be suitable for lower-middle-income nations.

Based on the number of stages, inverters are classified as multi-stage and single-stage inverters. Figure 2-5 shows the circuit organization of multi-stage and single-stage inverters. The top two diagrams (i and ii) represent the multi-stage inverters, and the bottom diagram (iii) represents a single-stage inverter.

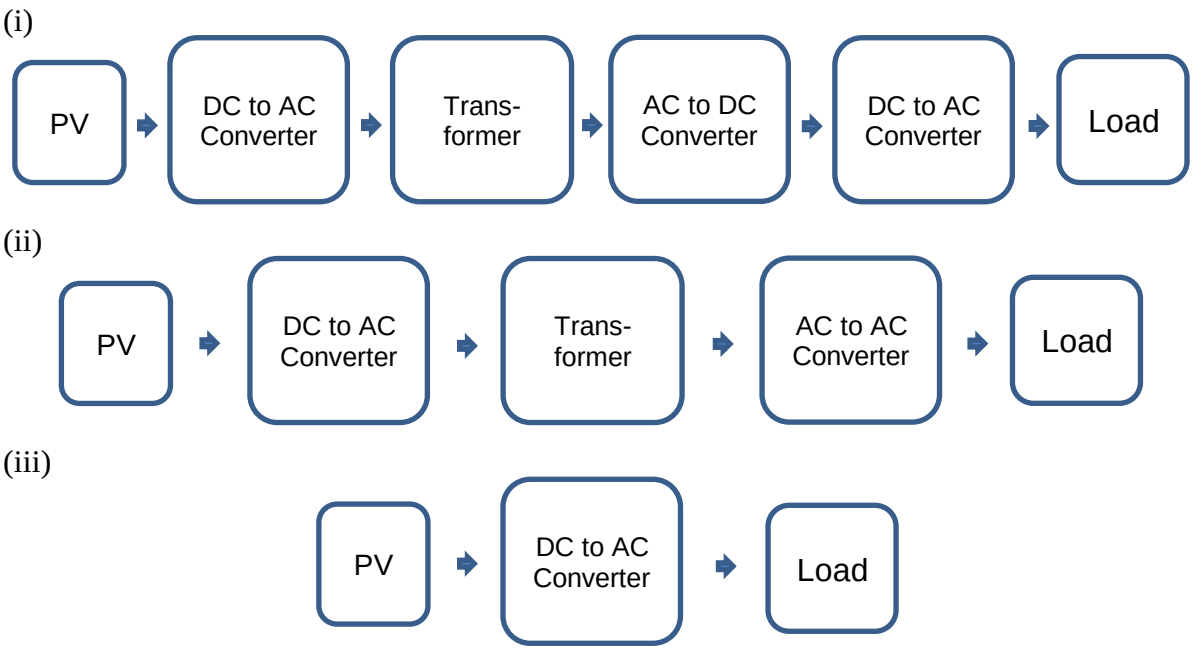


Figure 2-5 PV inverter layout categories: multi-stage vs single-stage
(Dogga & Pathak, 2019)

In the context of PV systems, the number of power processing stages can be combined to provide specific features such as more gain, isolation, a wide range of operation conditions, and reduced complexity of control strategies (with multiple stages it is sometimes possible to employ multiple controllers and thus one controller is not overtaxed computationally). In the literature Multi-Stage Power Converter (MSPC) systems have been introduced with variations in non-isolated DC-DC converters and isolated DC-DC converter layouts, including High-Frequency Transformer (HFT) configurations (discussed in Section 2.6).

Referring to Figure 2-5, these MSPC multi-stage systems can be classified as:

I. DC-AC-DC-AC converter circuits
II. DC-AC-AC converter circuits and
III. DC-DC-AC converter circuits

2.3.1 DC–AC–DC–AC Circuits

For the category of DC-AC-DC-AC converter circuits (see i of Figure 2-5), the variable DC voltage coming from a source, such as a PV module (or array), is converted to constant DC using the HFT based DC-AC-DC converter in the first stage, with the required voltage boosting ratio. The DC voltage is then converted into AC in the last stage. Here, the first stage converter may also offer Maximum Power Point Tracking (MPPT) operation and isolation. The cost and losses of these converters are high since there are several processing stages and there are a large number of components. Some variations in the incorporation of the DC-link are shown in Figure 2-6.

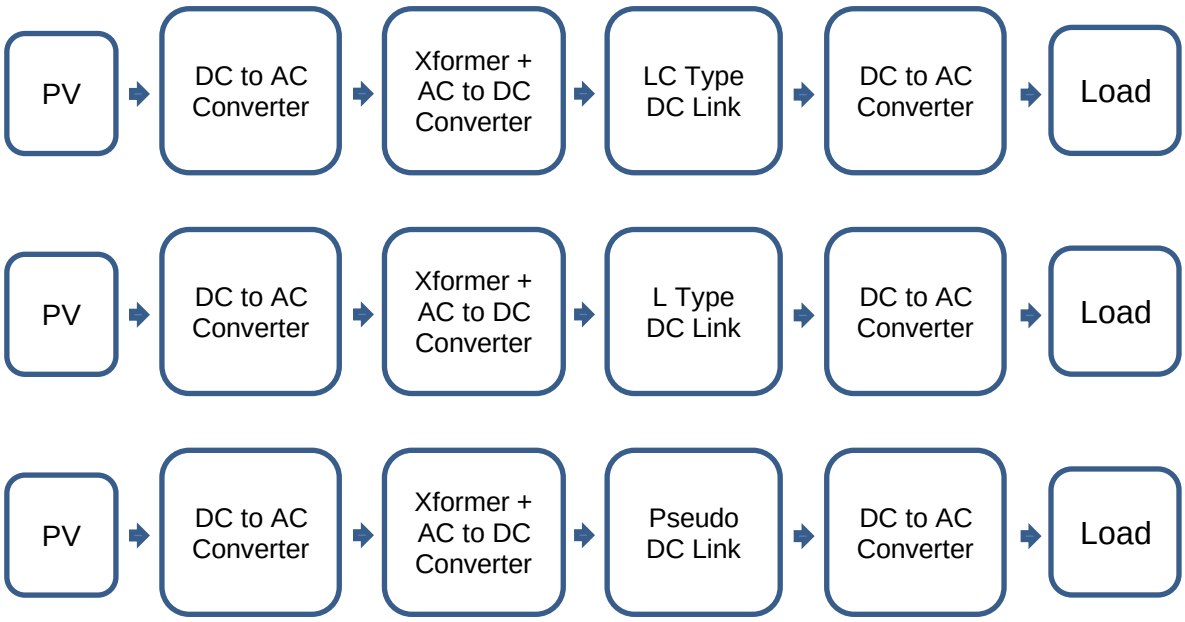


Figure 2-6 MSPC layouts resulting from DC-link implementation: LC, L and Pseudo-DC-link (Dogga & Pathak, 2019)

The DC-AC-DC-AC converter circuits can be divided into three sub-classes (see Figure 2-6):

I. LC-type DC-link based MSPC

II. L-type DC-link based MSPC

III. Pseudo-DC-link based MSPC

The LC-type DC-link is located between the DC-AC-DC converter and the final inverter, as is shown in Figure 2-7. As is well known, an LC filter in the DC-link results in a low ripple DC input to the final inverter, thus producing lower load voltage distortion. The LC filter also aids in power decoupling. Cost is an issue with this converter for remote village applications.

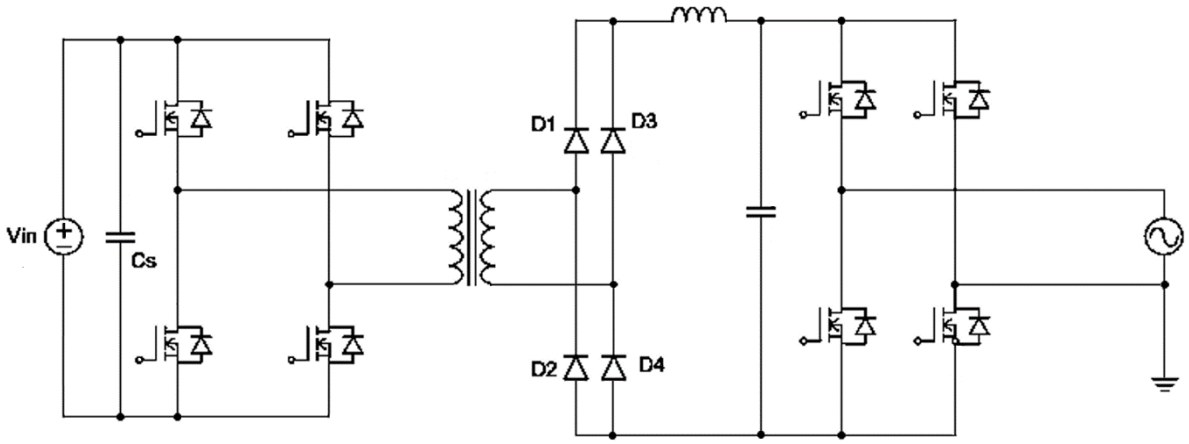


Figure 2-7 Multi-stage high-frequency layout of DC-AC-DC-AC layout with LC-type DC-link (Bose et al., 1985)

Another type of MSPC DC-AC-DC-AC converter circuit is the L-type DC-link MSPC system with the simple change of the DC-link as shown in Figure 2-8. The LC type DC-link inverter of Figure 2-7 is replaced with an L-type DC-link. By doing, this, the final inverter becomes a current source inverter, i.e., half-sinewave currents are generated through the inductor by proper control of power switches of the converter. These half-sinewaves are converted into full sinewaves by the final inverter and then fed to the load or to the grid (sometimes with the addition of a final filter for a grid connection, which is not shown in Figure 2-8). This converter circuit does not require a large DC-link capacitor, and results in better reliability and a lower cost compared to the converter circuit of Figure 2-7, and has the characteristic that the final inverter operates at the line frequency. However, this converter circuit offers lower power decoupling compared to the previous converter circuit of Figure 2-7 (Dogga & Pathak, 2019).

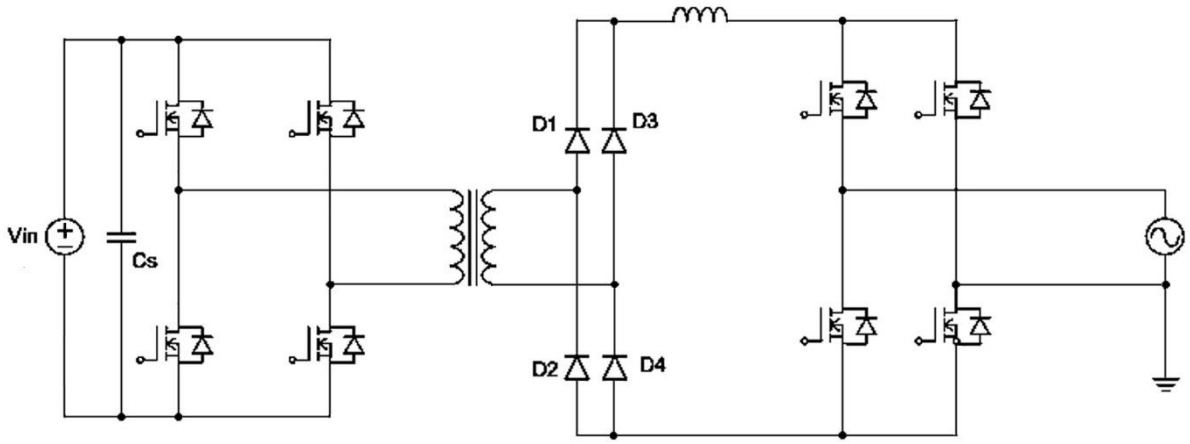


Figure 2-8 Multi-stage high-frequency layout of DC-AC-DC-AC layout with L-type DC-link (Bose et al., 1985)

The Pseudo DC-link based DC-AC-DC-AC multi-stage inverter is shown in Figure 2-9, in which the DC-link is replaced with a pseudo-DC-link (simply meaning, a wire DC-Link with no filter). Since the DC-link components are eliminated in this converter circuit, its cost and size are lower than the previous DC-AC-DC-AC converter circuits. However, this converter circuit has poor power decoupling and higher harmonic content than the previous two DC-AC-DC-AC converter circuits.

To summarize, note that all the DC-AC-DC-AC converter circuits discussed above have a high-frequency DC-AC inverter at the input of the converter, which converts the input DC voltage into high-frequency AC. This high-frequency AC amplitude can be increased using a High-frequency Transformer (HFT) and then the transformer AC voltage rectified into DC. The ripple voltage of the bridge rectifier output is reduced with the help of a DC-link placed after the bridge rectifier (except for the pseudo-DC-link). The DC-link output is fed to the final inverter, which processes the DC voltage (or current for the pseudo-DC-link converter) into AC voltage (or current for the pseudo-DC-link converter).

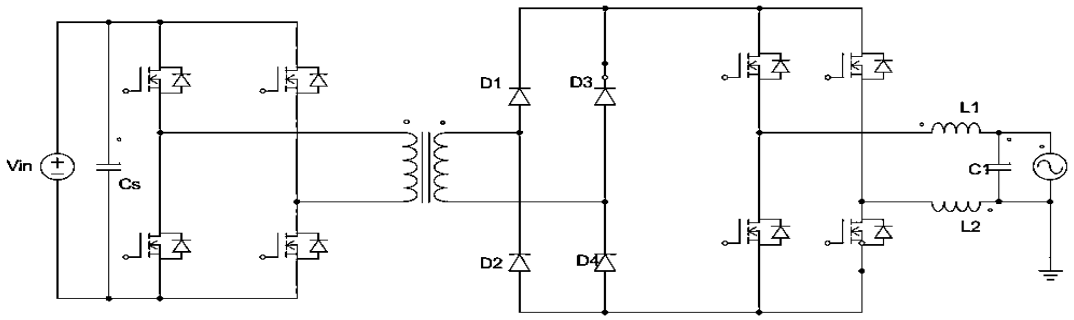


Figure 2-9 Multi-stage high-frequency layout of DC-AC-DC-AC layout with pseudo-DC-link (Dogga & Pathak, 2019)

2.3.2 DC-DC-AC Circuits

The DC-DC-AC layout in the categories of MSPCs is the most common one. The DC-DC-AC converter utilises two-stage power conversion (TSPC). To improve design flexibility, voltage step up, and efficiency capabilities, an input DC to DC power converter is placed between the PV module and the inverter, as shown in Figure 2-5 (ii). The main difference between the DC-AC-DC-AC and the DC-DC-AC power conversion schemes is that the isolated converter employed in the DC-AC-DC-AC converters is replaced with a transformerless DC-DC converter. The Boost converter, Buck-Boost converter, Single-Ended Primary-Inductor converter and the Cuk converter, are often employed in TSPC systems. A DC-DC boost converter fed Half Bridge Inverter (HBI) is shown in Figure 2-10, and a DC-DC boost converter fed Full Bridge Inverter (FBI) is shown in Figure 2-11. These two inverter circuits are examples of how to realize a simple TSPC, and are commonly employed two-stage inverter configurations for PV applications. In the case of the HBI converter circuit, the DC-link is sometimes formed using two capacitors (as in Figure 2-10). These two capacitors provide a centre tapped DC source to the HBI.

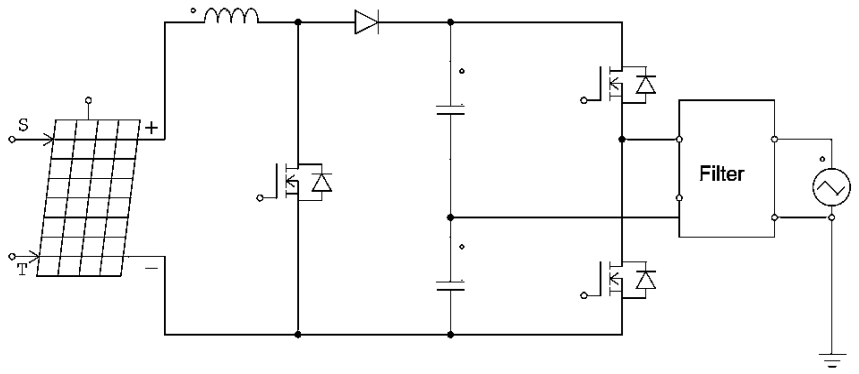


Figure 2-10 Half Bridge inverter with DC-DC front-end boost stage
(Khaligh & Onar, 2010)

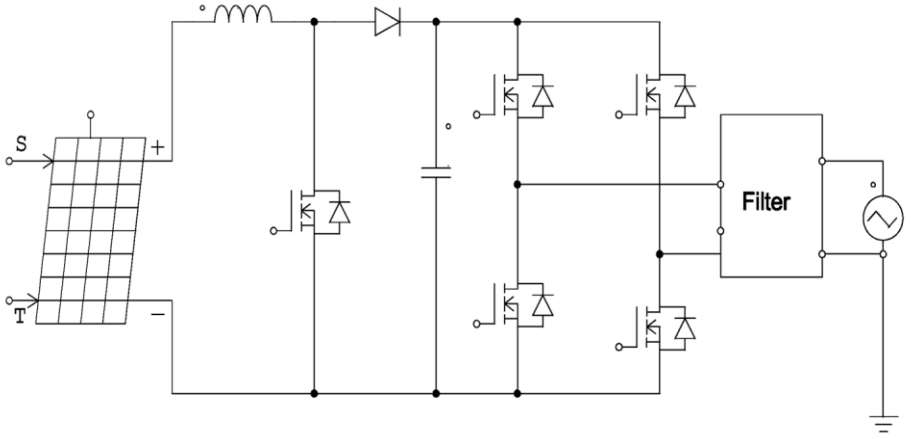


Figure 2-11 Full Bridge inverter with DC-DC front-end boost stage
(Khaligh & Onar, 2010)

Note that for the FBI type of TSPC, the full output voltage of the boost converter is equal to the amplitude of the AC voltage. So, a higher output voltage is possible in FBI-based TSPCs. This has a consequence that device peak reverse voltage is half of the value for the HBI for a given power rating of the converter. As a result, FBI type TSPCs are often selected in place of the HBI type converter circuit (as is done in this thesis study). An alternative to the boost type first stage for TSPCs is the use of a buck-boost converter, an example of which is shown in Figure 2-12.

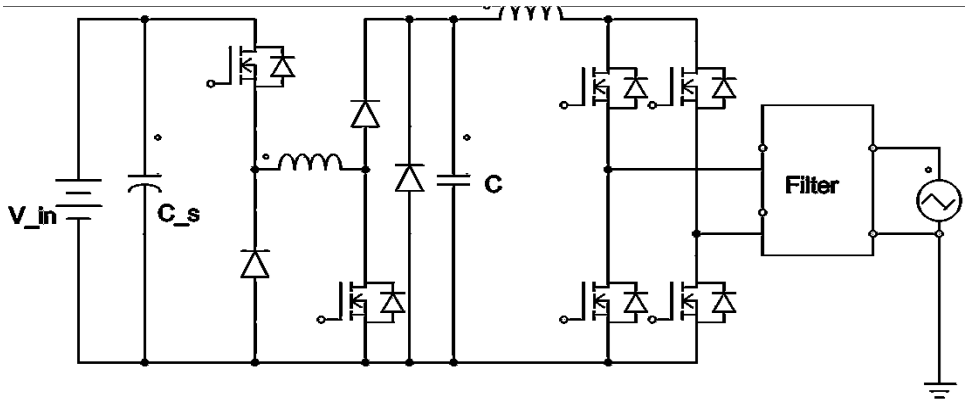


Figure 2-12 Full Bridge inverter with DC-DC front-end buck-boost stage (Saha & Sundarsingh, 1996)

Saha & Sundarsingh (1996), proposed the Full Bridge inverter with DC-DC front-end buck-boost stage as shown in Figure 2-12. Saha & Sundarsingh suggest that the DC input voltage be limited to 100 V for safety in the operation of a PV system. A DC voltage is produced with the first stage buck-boost converter and provided to the second stage. Although this converter circuit has a simple structure, its voltage multiplication capability and DC voltage variation are restricted. Also, this converter circuit requires twice as many semiconductor devices as for conventional non-isolated boost DC to DC converters (see Figure 2-12). Saha & Sundarsingh extended their research and developed a simple transformer type Full Bridge inverter with DC-DC front-end buck-boost stage, as shown in Figure 2-13.

The operation of this converter circuit is similar to the buck-boost version of Figure 2-12, since in the first stage a DC voltage is produced by buck-boost action, and full wave inverter action is accomplished in the second stage. With the transformer and half wave rectification of the DC to DC operation, this type of converter tends to be used for low to medium power levels.

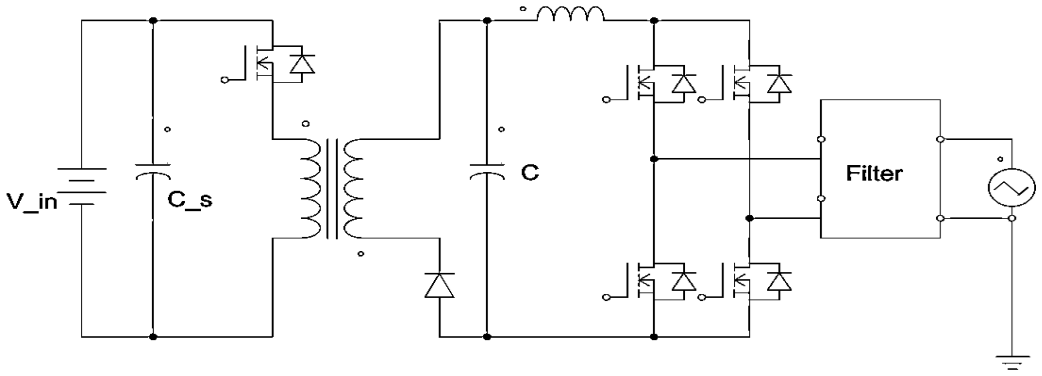


Figure 2-13 Isolated Full Bridge inverter with DC-DC front-end buck-boost stage (Saha & Sundarsingh, 1996)

2.3.3 Use of Active Decoupling

Shimizu et al., (2006) suggested a Flyback, combined with buck-boost, inverter configuration shown in Figure 2-14. Their proposed isolated two-stage inverter consists of a buck-boost converter with an intermediate capacitor accompanied in the final stage by a Flyback inverter. The top-left MOSFET provides Flyback operation and the lower left MOSFET provides buck-boost operation, and the lower left capacitor acts as an intermediate storage device. The key converter, i.e., the buck-boost converter, employs the MPPT process for solar power applications, and energy is retained in the intermediate capacitor. The voltage of the capacitor includes two elements: DC and AC, where the AC ripple has a frequency double the load frequency ripple. The Flyback inverter utilises energy in the intermediate capacitor, to reduce (i.e., to decouple) the ripple frequency in the voltage across the front-end capacitors.

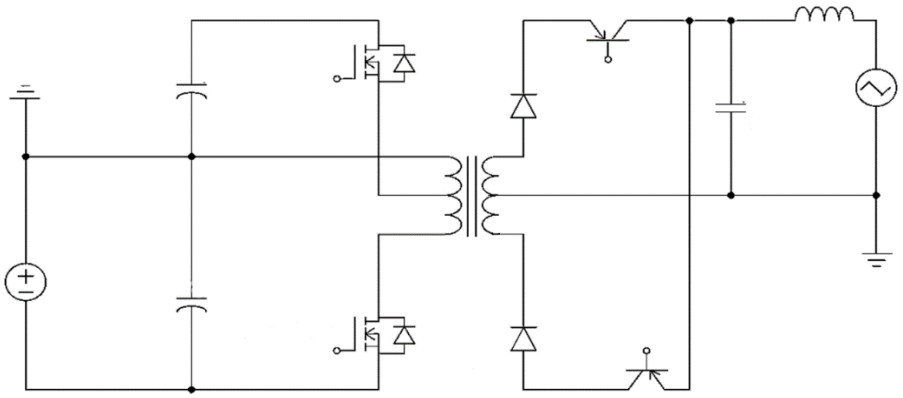


Figure 2-14 Flyback and buck-boost inverter with active power decoupling (Shimizu et al., 2006)

2.3.4 Resonant DC-AC-DC-AC Converter Circuits

For MSPC schemes such as DC-AC-DC-AC inverters, losses are likely to be significant owing to the added number of stages. Implementing a soft-switching approach in such cases is advantageous as efficiency is a central issue in PV frameworks.

In the literature, there are several resonant DC to DC converter topologies. The Series-Parallel Resonant Converter (SPRC) maintains the benefits of Series Resonant Converter (SRC) and the Parallel Resonant Converter (PRC) with lower circulated energy (S. Bhattacharya et al., 2017). Nevertheless, these converters (SRC, PRC, and SPRC) must work at higher switching frequencies to have a high voltage multiplication factor. The SRC, PRC, and SPRC thus have high circulated energy compared to non-resonant circuits, which decreases performance. As a result of lower circulated energy in the Inductor Inductor Capacitor (LLC) resonant converter, the efficiency can be higher. This configuration is shown in Figure 2-15 (S. Zhang et al., 2016). There are also other variations in this category, like the current fed with Full and Half Bridge configurations, though these are beyond the scope of this literature review. One final note regarding resonant converter front-end stages: It is well known, that resonant operation reduces switching energy (hence the switching frequency can be as high as 1MHz), however there is the issue that peak voltage or peak

current for the power transistors can be very high (due to the oscillatory nature of the voltage or current). The high voltage or current peak value, increases power device stress, and consequently increases device cost as well.

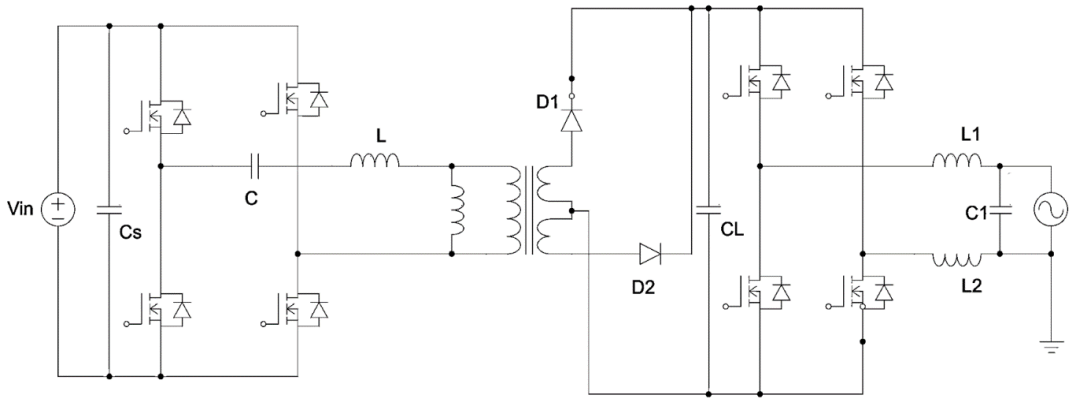


Figure 2-15 Full Bridge inverter with LLC resonant DC-DC front-end (S. Zhang et al., 2016).

2.3.5 Multi-Level Two-stage Power Converters

The Multi-Level inverter (MLI) concept is an alternative transformerless converter circuit with high and medium power applications. One of the MLI converter circuits known as a Diode-Clamped Multi-Level inverter (DCMLI) is shown in Figure 2-16 (Lee et al., 2011).

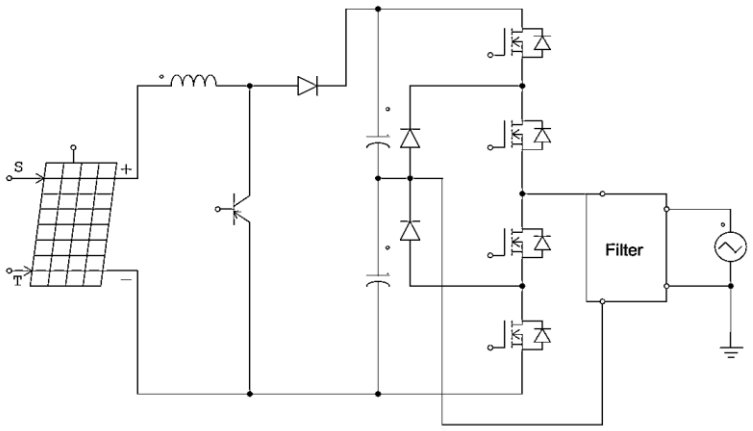


Figure 2-16 Diode clamped multi-level inverter (Lee et al., 2011).

In the case of the converter of Figure 2-16, half of the boost converter output voltage is equal to the peak value of AC voltage. Another converter circuit was developed with two individual boost converters feeding the MLI, as shown in Figure 2-17 (Hinz & Mutschler 1996). Variations on the converter of Figure 2-17 include capacitor clamped, cascaded H-bridge and modular Multi-Level converters. Among these converters, the modular Multi-Level and cascaded H-bridge inverters are commonly employed for solar PV applications (Dogga & Pathak, 2019).

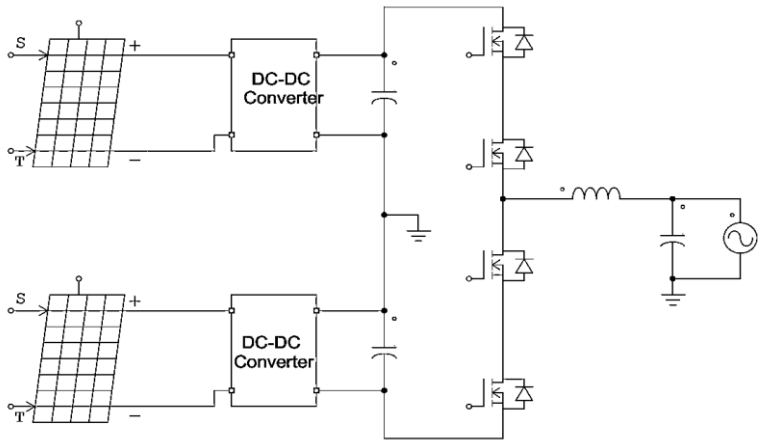


Figure 2-17 Multi-DC source Multi-Level inverter
(Hinz & Mutschler 1996)

There are two major categories of Multi-level TSPC layouts depending on the output of the DC-DC converter:

- Constant DC based DC-DC converter fed PWM inverter layout
- Rectified DC fed line-frequency inverter layout

The first approach is the traditional way of converting the energy in a switch mode two-stage inverter, whereas in the second approach, a modified sinewave is generated at the outputs of the DC-DC converter with suitable control methods. Thus, it is possible to swap a high-frequency

inverter with a line-frequency inverter. However, the half-sinewave based DC transformation approach suffers from a complex control method, and this method also requires that a DC-DC converter be developed for peak power instead of average power. Generally, TSPC schemes (see Figure 2-18) have some common disadvantages, including a high component count, two separate control systems, as well as significant size, price, and weight (Dogga & Pathak, 2019). In the next section, single-stage schemes are considered.

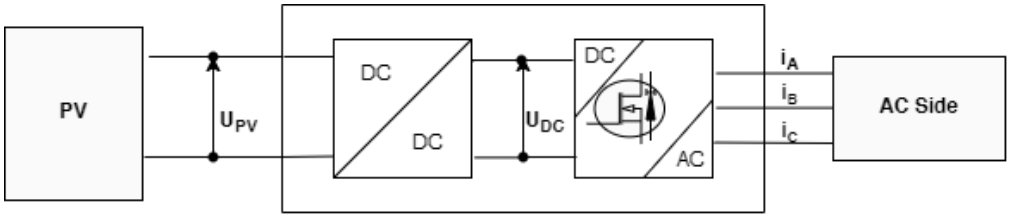


Figure 2-18 TSPC layout
(Dogga & Pathak, 2019)

2.4 SINGLE-STAGE INVERTER CONFIGURATIONS

In the above discussions, one might consider that the boost functionality, offered by the DC-DC converter in many of the inverter configurations presented, could be removed if the voltage of the solar PV array is relatively high. Thus, a Single-Stage Power Converter (SSPC) would be preferred for situations where the DC source is sufficiently high (such as a PV array). It is possible to characterise these SSPCs as done by (Reddy et al., 2011):

1- Step-down voltage single-stage

2- Step-up voltage single-stage

Alternatively, it is possible to use the Flyback converter as the basis for PV inverter systems where each panel, or a grouping of panels, has its own inverter (referred to as a micro-inverter). Several variations of this category have been introduced in the literature and in industry. One variation proposed by (Z. Zhang et al., 2011) can be incorporated for the single-stage grid-connected PV system, where a discontinuous control method is suggested to reduce the switching frequency. For the proposed layout, a Flyback transformer is replaced with coupled inductors. This converter is only applicable for low power applications because of the coupled coils. The operation of the converter during two half-cycles is asymmetrical, and the conduction and switching losses are also on the higher side.

In a similar manner, Xue & Chang, (2004) proposed a single-stage converter circuit base on the buck-boost converter, as shown in Figure 2-19, where the two inductors shown are coupled. The converter operates with one pair of diagonal power transistors controlled for each half cycle of the power waveform, such that one transistor is on while PWM is applied to the other diagonal transistor. The switching and conduction loss are low and the electromagnetic interference of this converter circuit is low, and as in the case of the (Z. Zhang et al., 2011) converter, the converter proposed by Xue & Chang is only appropriate for low power applications.

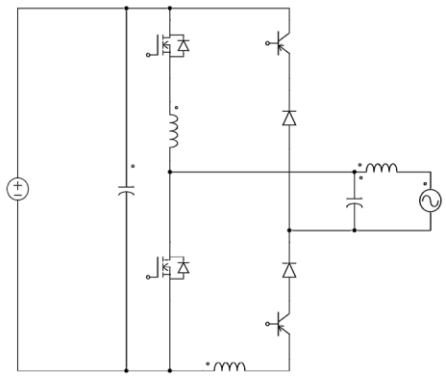


Figure 2-19 Buck-boost based coupled inductor inverter for grid-connected operation (Xue & Chang, 2004)

Another buck-boost derived converter circuit is shown in Figure 2-20, proposed by Kasa et al. (2000). Like the Zhang and Xue converters discussed above, half of the power transistors are not used for each half cycle of the power waveform. However, one advantage of the Kasa converter of Figure 2-20 is the common ground line from the DC source to the AC grid.

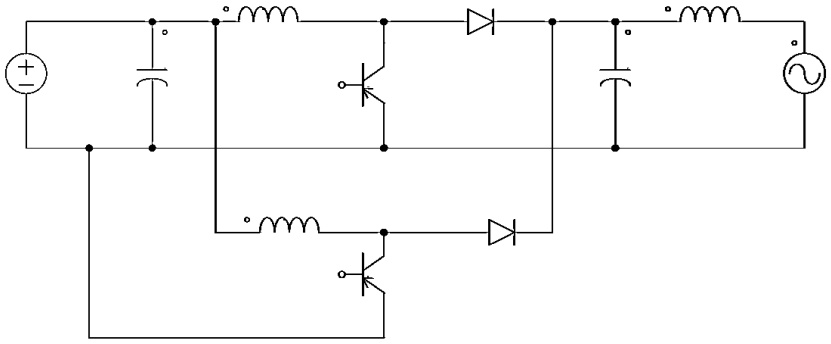
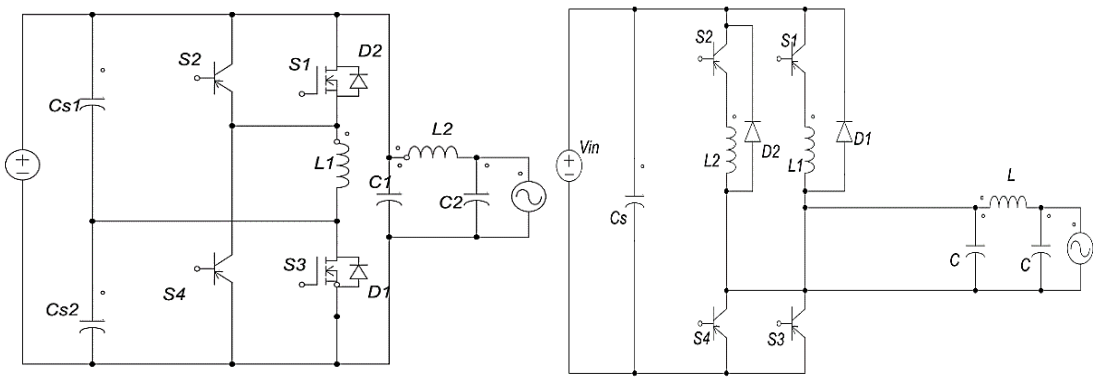


Figure 2-20 Buck-boost converter with common ground line
(Kasa et al., 2000)

Promising single-stage series resonant buck-boost inverters were introduced by Wang (2004). These converter circuits have a mode of operation to reduce losses through the use of zero current switching (see Figure 2-21). Referring to Figure 2-21 (b), he principle of operation is as follows. Switches S_1 & S_3, and diode D_2 are employed during the positive half cycle; whereas switches S_2, S_4, and diode D_1 are employed during the negative half cycle. Switches S_3 and S_4 are turned on using zero current switching with the LC series-resonant circuit that significantly reduce the switching losses. Low electromagnetic interference problems are an advantage of this converter which can operate at a high switching frequency. However, there is the issue of asymmetrical operation in the half cycles.



(a) (b)

Figure 2-21 (a) Half Bridge resonant buck-boost inverter; (b) Full Bridge resonant buck-boost inverter (Wang, 2004)

2.4.1 Impedance source converters

There is interest in the literature regarding impedance source (or Z-source) converters, which have the ability to provide step-up or step-down voltage action without a transformer. Huang et al. (2006) proposed a Z-source inverter, as depicted in Figure 2-22. However hard-switching does increase the switching losses.

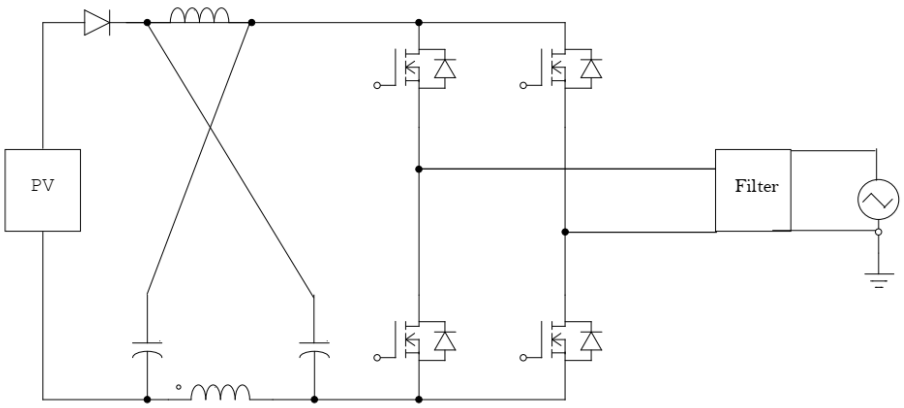


Figure 2-22 Example of a Z-source inverter (Huang et al., 2006)

2.5 PARALLEL SWITCHES IN NEUTRAL POINT CONVERTERS

It has been suggested in the literature that a next-generation inverter design is the three-level Neutral Point Converter approach (Steinmetz, 2013). This converter circuit is attractive to uninterruptable power supply manufacturers. Usually MOSFETS are employed, however above about 15 kW the on resistance of the MOSFET device becomes an issue for higher conduction losses (Steinmetz, 2013). As shown in Figures 2-23 and 2-24, novel switch configurations have been proposed to address this higher frequency requirement by replacing the reverse recovery diode with a low power MOSFET. The overall switching losses (both on and off) are reduced. Thus, the use of a parallel switch also aids in efficiency improvement. The principles of the Neutral Point Converter can also be applied in 3-phase cases, as shown in Figure 2-25.

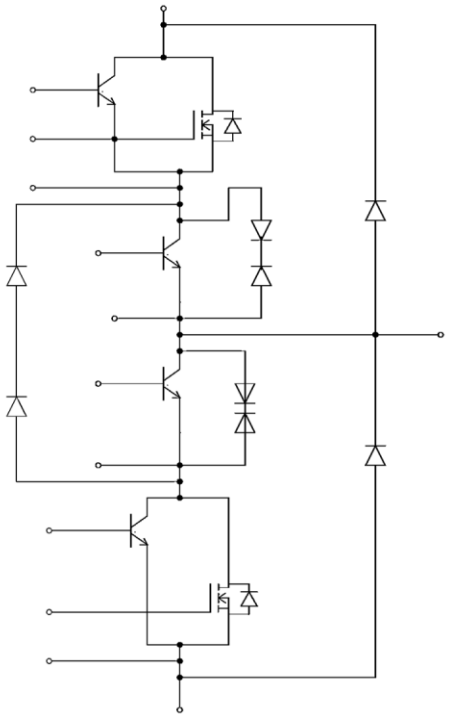


Figure 2-23 Parallel Switch realised by replacing the reverse recovery diode with power transistor and lower power MOSFET
(Steinmetz, 2013)

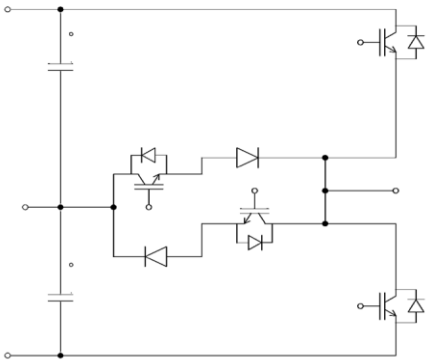


Figure 2-24 Single-phase Mixed Neutral Point Converter;
(Steinmetz, 2013)

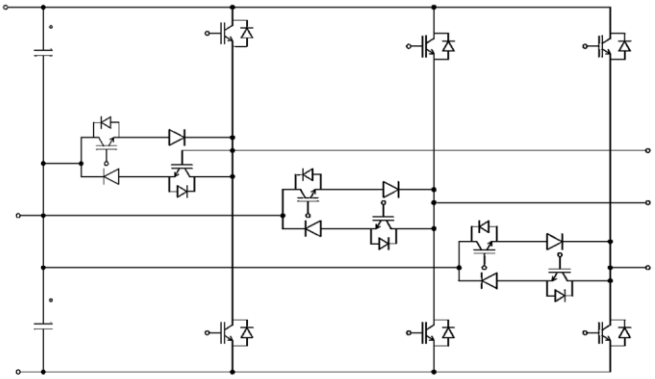


Figure 2-25 Integrated three-phase Mixed Neutral Point Converter
(Steinmetz, 2013)

2.6 INVERTER SWITCHING FREQUENCY

Based on the switching frequency of the power transistors in a given inverter, it is reasonable to classify inverters into three categories: power-frequency (50Hz or 60Hz), intermediate-frequency (400Hz to 10kHz) and high-frequency (10kHz to 1MHz) categories (GoHz, 2016). A discussion about the switching frequency now follows.

For residential and commercial buildings, the power-frequency of an inverter (this is the frequency of the waveform delivered by the inverter to the load) is usually 50 Hz or 60 Hz. Figure 2-26 illustrates the common inverter circuit that utilizes a power-frequency step-up transformer. If this

inverter were to be used for the application of this thesis, a 50Hz square wave (or modified square wave) would be seen at the input and output of the transformer, with a DC voltage such that the RMS value of the load voltage is 220V. Although this type of inverter is simple to design and construct, and costs can be reduced by even eliminating the filter after the transformer, there are issues with the cost and large size of the power-frequency transformer, and with the higher distortion and difficult-to-filter harmonics of the square wave waveform (the modified square wave typically has a THD of about 30% and the square wave has a THD of 48% with significant 3^{rd}, 5^{th} and 7^{th} harmonic components).

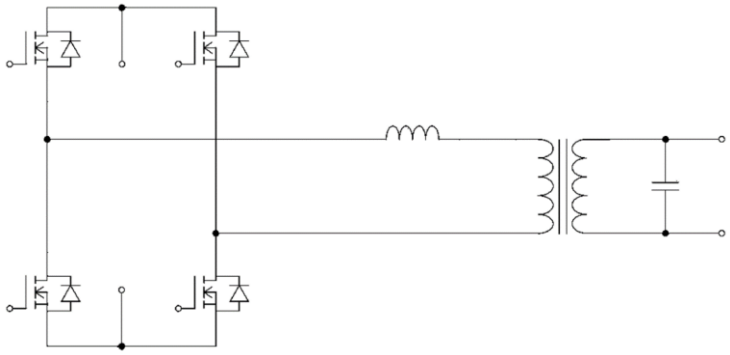


Figure 2-26 Common power-frequency transformer inverter

(GoHz, 2016)

It has long been known that the higher the frequency of a waveform applied to a transformer, the smaller the size and weight of the transformer. Hence, as aircraft were developed, a standard was developed to employ 400Hz in aircraft power systems to keep weight low. In the 1960s, in part driven by technological innovation for light DC to DC power converters to be used in satellites, high-frequency converters were developed (with the high-frequency operation, a small light weight transformer can be used). This has led to the development of high-frequency inverters, for example, the Centre Tapped DC-DC converter, as shown in Figure 2-27.

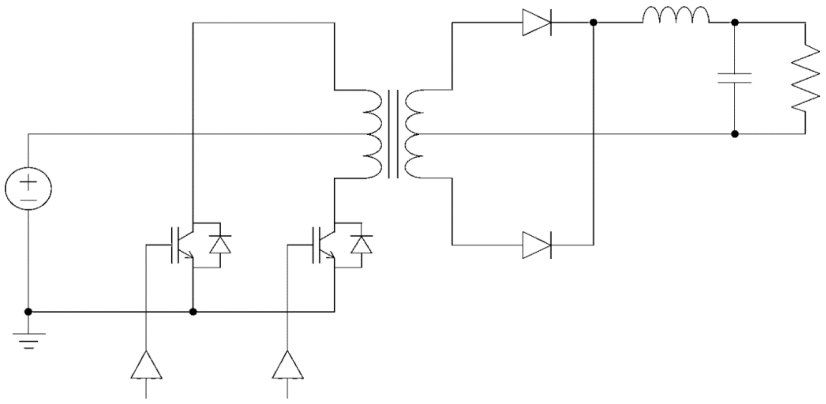


Figure 2-27 Centre tapped high-frequency DC-DC converter circuit

(Trujillo et al., 2011)

The primary issue of concern for this thesis is efficiency at low power loading. As can be seen in Figure 2-28, are the typical efficiency curves for power-frequency (e.g. 50Hz or 60Hz) and high-frequency (i.e., above 10kHz) inverters, as adapted from GoHz (2016) (there is an error in the labelling of the curves in (GoHz, 2016), which has been corrected in Figure 2-28). Note that the power-frequency inverter has considerably lower efficiency at mid-power loading. This is a result of large core (also called magnetizing) losses in the transformer, where a large voltage is still across the transformer terminals, even when the load is light, hence magnetization losses are high. As a result, despite the simplicity of the power-frequency transformer inverter of Figure 2-26, it is not used for study in this thesis.

Note: In a very different vein, an alternative approach that was not pursued in this thesis, would be the design of a completely separate 12VDC to 220VAC converter, rated at 3.5W to operate just one LED light during the night; though maybe this option can be explored in the future.

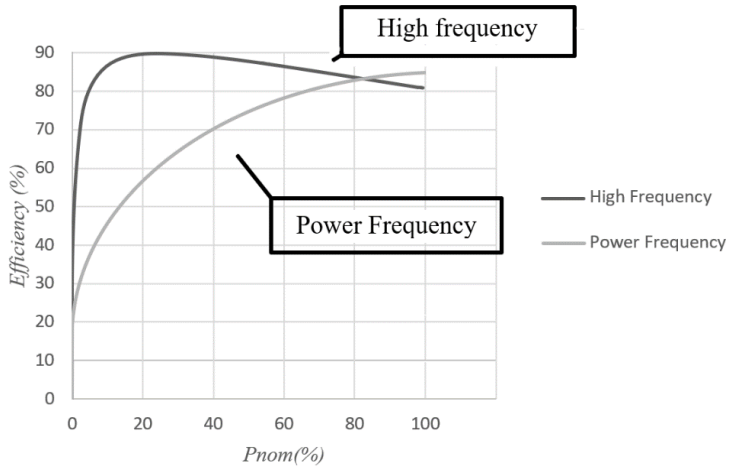


Figure 2-28 Efficiency curves of high frequency and power-frequency inverters (GoHz, 2016)

The converter of Figure 2-27, employs centre taps on the primary and the secondary of the transformer. By modifying the transformer topology (i.e., with or without the use of a centre tap on the primary or on the secondary of the transformer) there are several variations of the converter of Figure 2-27. If the primary winding has a centre tap, a common name of the first stage DC to DC converter is the Push Pull converter (see Figure 2-29). With low component count, the cost can be kept low for the Push Pull based inverter, and hence it is selected for study in this thesis.

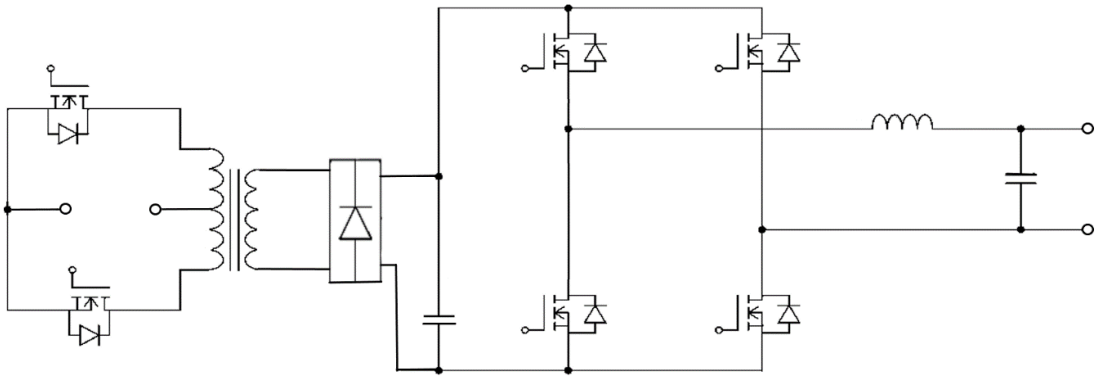


Figure 2-29 A Push Pull based inverter circuit (GoHz, 2016)

Chapter 3: Methodology and System Modelling

3.1 INTRODUCTION

As noted above, the objective of the thesis is to investigate transistor switching of an inverter for very low power operation, such as 3.5W, given a 200W rated Full Bridge inverter with MOSFET switching devices. If the transistor switching frequency can be reduced, it may be possible to reduce switching losses such that inverter efficiency remains sufficiently high. It is expected that the distortion of the inverter 50Hz load voltage waveform can become quite large, however, for a rural village application, the cost savings in system implementation, may justify the increased harmonic distortion in the 50Hz load output voltage waveform. The ultimate objective of this thesis research is that the battery of a solar power system for a residence in a village can be sized smaller, and still have sufficient state of charge to operate a single 3.5W 220VAC LED light overnight. As discussed above, previous research has concentrated on inverter operation for compact florescent light (CFL) operation of 9W. The research of this thesis represents an extension of low power operation, down to a lower power level of 3.5W. Four switching frequencies are investigated: 20kHz, 10kHz, 2.5KHz and 0.2kHz. Note, that at the current time (2022), a 200W switch mode converter would typically be designed to have a switching frequency of 100kHz or higher, thus, the upper value of 20kHz was selected as illustrative of the efficiency that might be obtained at a high switching frequency. The Push Pull DC to DC converter is operated with a switching frequency of 10kHz. Component ratings (including the DC link voltage) centre on the requirement for a load voltage of 220VAC. To provide some margin for situations such as overloading of the system, it was decided that the modulation index be set to 80% for rated operating conditions.

3.2 SYSTEM OVERVIEW AND SIMPLIFIED SIMULINK MODEL

Shown in Figure 3-1 is a block diagram representing the system that is investigated, and modelled in SimuLink. The battery voltage has a nominal value of 12V, though in practice the voltage can be higher or lower (for example a fully charged lead-acid battery can have a voltage as high as 13.5V). The nominal DC link voltage at the output of the Push Pull converter is 389V. This voltage is chosen so that the ideal (lossless) AC load voltage is 220Vrms with a modulation index of 80% for inverter operation (i.e., 389V x 0.8 = 311V corresponding the peak value of an ideal sinusoidal AC voltage of 220V (i.e., 220V x $\sqrt{2}$ = 311V). The LC filter, is chosen, for the purposes of this research, to keep cost low in a village residential application, namely, L=1mH and C=1000µF. Note that a low-pass LC filter has a corner frequency of approximately $1/(2\pi\sqrt{LC})$, in this case a value of 159Hz. This value is lower than would be found in a high-frequency switching inverter, however, since the intention of this research is to investigate low switching frequency operation, a correspondingly low corner frequency was selected to avoid excess distortion at a switching frequency of 200Hz. In practice a smaller LC filter would be employed and the increase in distortion of the power system would be tolerated to the level possible to reliably operate a 220VAC 3.5W LED light. As noted previously, the nominal AC load voltage is 220Vrms with a power-frequency of 50Hz. These values of voltage and power-frequency are popular in many developing countries.

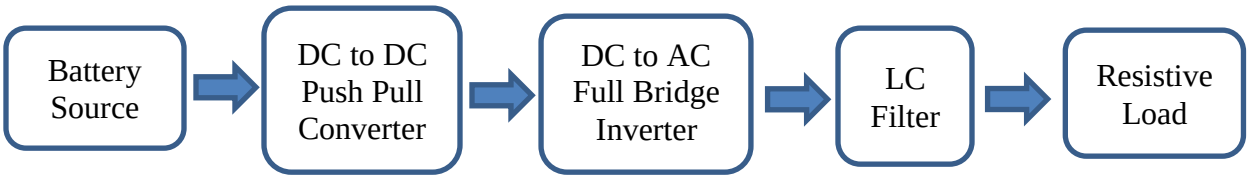


Figure 3-1 Block diagram of power system investigated

Shown in Figure 3-2, is a simplified diagram of the SimuLink model employed, with a range of switching frequencies from 20kHz down to 200Hz, and output power levels from the rated value of 200W down to 3.5W. Details about the SimuLink model are given in Section 3.3. The load resistor is set to a constant value for a given output power of the inverter. A brief overview of the system modelling is now given here (more details are given in Section 3.3). Refer to Figure 3-2. The power circuit consists of two stages, a Push Pull DC to DC converter followed by the Full Bridge MOSFET inverter. The Push Pull DC to DC converter steps up the DC voltage from the nominal battery voltage of 12V to a nominal DC Link voltage of 389V with a voltage ripple that depends on operating conditions (the peak to peak voltage ripple was generally on the order of 5% to10% of the DC value). The switching frequency of the Full Bridge inverter is fixed in separate simulations with values of 20kHz, 10kHz, 2.5kHz and 200Hz. Naturally Sampled Pulse Width Modulation is employed for the Full Bridge inverter with unipolar switching (i.e., 3-level H bridge voltage such as in Figure 4-3). Inverter power output is calculated in the SimuLink model by multiplying the RMS values of the load voltage and load current (since the load is a fixed resistance). The simulations were performed with the discrete time stepping parameter set to: 25μs for switching frequencies of 200Hz and 2.5kHz, 10μs for the switching frequencies of 10kHz and 5μs for the switching frequency of 20kHz. Steady state values were used for all power calculations (i.e., at time greater than 1.0 seconds of operation, after all transients had subsided). The proportional integral (PI) load-voltage control-loop was studied with a trial and error approach to obtain the proportional coefficient of 0.001 and integral coefficient of 0.04, found to be effective for many of the trial simulations. However it was found that the SimuLink simulations sometimes became unstable, and it was decided that an open loop control would be most effective as discussed in Section 3.3.

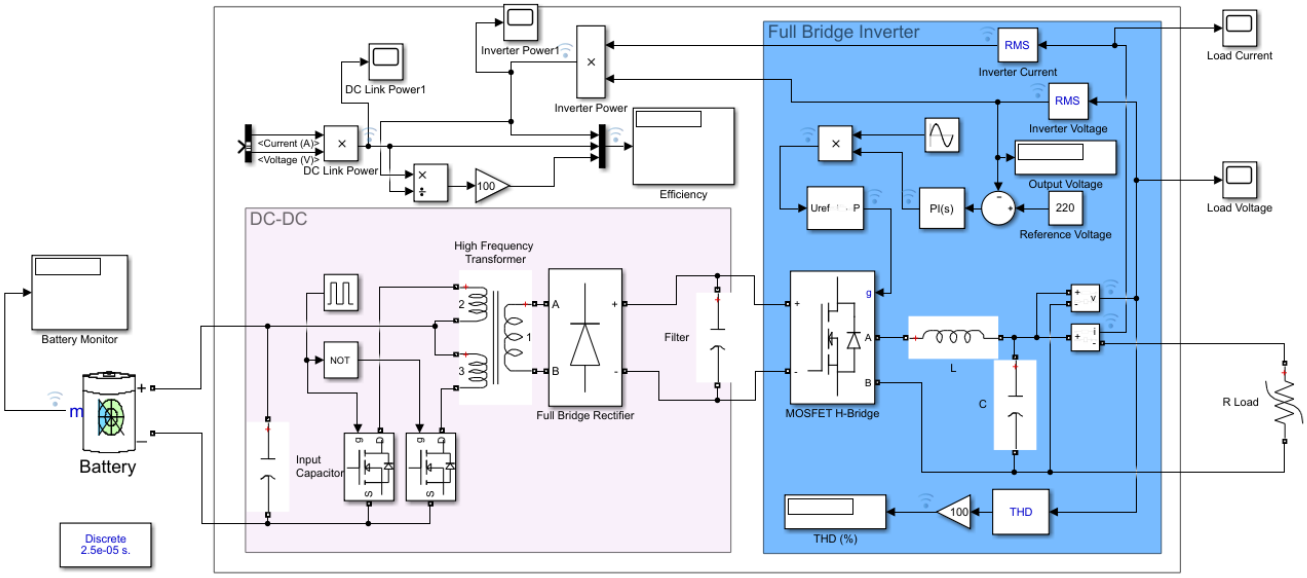


Figure 3-2 Simplified diagram of SimuLink model
Note: The load is a linear resistor that is set to a constant value for a given power level.

3.3 DISCUSSION OF SIMULINK MODELLING

Shown in Figure 3-3 is the model used to perform the simulations discussed in Chapter 4.

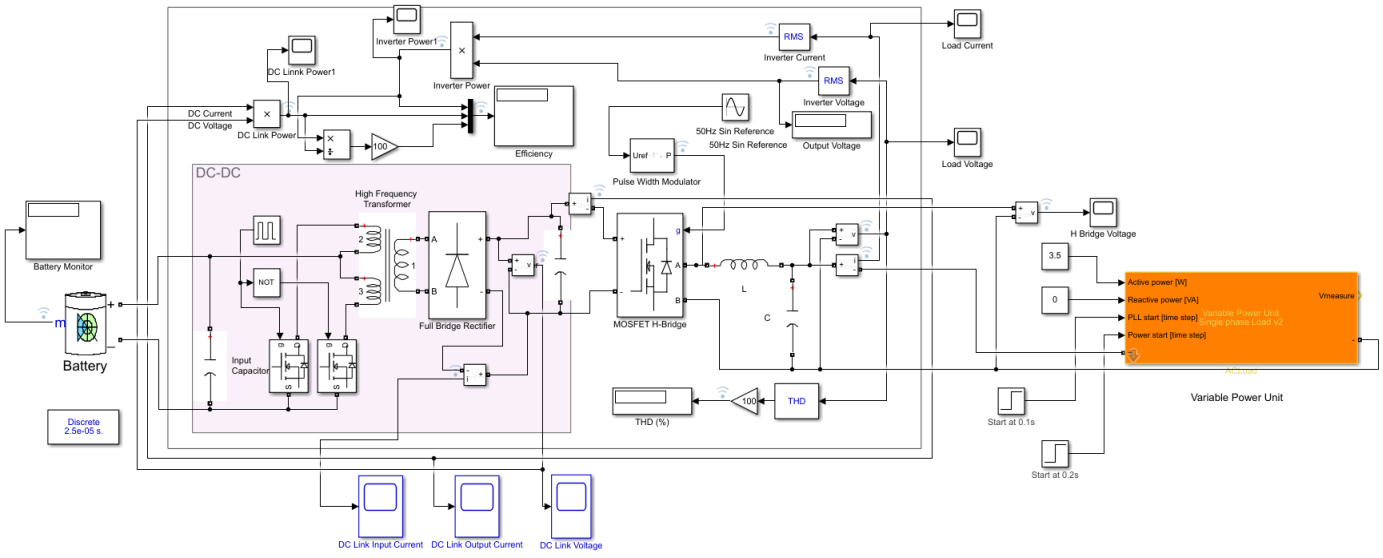


Figure 3-3 SimuLink model employed to perform efficiency study

SimuLink (developed by MathWorks) is a computer simulation program that models the behavior of electrical circuits and electrical systems containing analog, digital and control devices. SimuLink is suitable to simulate practical electrical systems in research and development, especially where control characterisation is paramount. It can also be employed to find steady state waveforms as is done in this thesis. As with PSpice, an inverter can be modelled in SimuLink with details regarding control, and device parameters. Although the commercial component access with SimuLink is not as straightforward as with PSpice, SimuLink is more versatile in varying circuit operating parameters and conditions especially for research purposes. With SimuLink, it is possible to model MOSFET devices, pulse width modulation (PWM) algorithms, loading conditions, etc., to provide characterisation of a given circuit, including steady state, transient, harmonic analysis, Total Harmonic Distortion (THD), and other useful characterisations. For this reason SimuLink was chosen for the purposes of this thesis. Referring to the SimuLink model of Figure 3-2, after a trial and error process, it was found that a proportional coefficient of 0.001 and integral coefficient of 0.04 was effective in many of the situations studied. However, after some time (as little as about 30ms to over one second) the PI controller was not always able to control operation in an acceptable stable manner. Even when P and I coefficients were effective (i.e., stable operation with a fairly constant RMS load voltage) for several sets of operating parameters, the coefficients were not effective for all sets of operating parameters under study. Hence, by observing the amplitude of the sinusoidal reference waveform, entering into the Pulse Width Modulation block of Figure 3-2, with PI control, it was then possible to estimate a reasonable sinusoidal reference amplitude to be employed in the open-loop SimuLink system of Figure 3-3. In this way, it was possible to modify the sinusoidal reference amplitude for stable system

operation and perform the efficiency and THD study necessary for this thesis (results given in the next chapter).

With the above SimuLink model of Figure 3-3, the switching frequency was varied from 20kHz to 200Hz to observe the change in inverter efficiency. Also varied was the load resistance, using the Variable Power Unit sub-block where the power consumption can be adjusted by a control variable (for example, 3.5W, as shown in Figure 3-3). The Variable Power Unit sub-block was custom designed for this thesis, so that the power setting can be fed into the sub-block as a parameter, and the Unit will adjust the resistance with time to maintain a constant power in the load. Efficiency was calculated in the SimuLink model (as seen in Figure 3-3) by taking the ratio of the system output power to the inverter input power. Output power was calculated by the product of the RMS load voltage and RMS load current. Inverter input power was calculated by the product of the DC Link voltage waveform and the DC current waveform into the inverter (see Figure 3-3).

Comments Regarding the Load Profile for a Village Home

Based on the author's experience and discussions with professors at the University of Calgary, for a remote village renewable energy application such as microhydro or solar power, the power allotted to each home is anywhere in the range of 50W to 300W. Hence the selection of a 200W rating for the inverter system under study. During the daytime, typical loads could be: an air fan, satellite equipment, a sewing machine, and in some occasions, a small refrigerator. It is not difficult to obtain daytime peak loads on the order of 200W, and it is not unlikely that the rated load will be exceeded at some times. During the night a village home may have a single light outside the home entrance, even if only to assist seeing the way to an outdoor latrine. A decade ago, that light

would likely be a compact florescent light, and today that light would be an LED light. At this time (2022), a commercial 220VAC LED light can have an electrical power input rating as low as 3.5W and have a radiated visible light power output slightly less than that of an old style 40W incandescent light. Hence, the selection of a 3.5W load to be investigated for this thesis.

Pulse Width Modulation

Shown in Figure 3-4 is an example of naturally sampled sinusoidal pulse width modulation to obtain a bipolar waveform across the H Bridge output terminals, prior to the LC filter. The DC input voltage to the inverter is set to 500V, simply for illustration purposes. The triangular carrier waveform is at the switching frequency (in this case 4kHz for illustration). The modulating waveform is a pure sinusoidal wave (which is referred to in the SimuLink model of Figure 3-3, as the 50Hz Sin Reference). For bipolar PWM, the carrier wave and the modulating wave are compared to produce the waveform of the bottom plot in Figure 3-4.

Although bipolar PWM was initially investigated, it was later found that unipolar PWM provided a lower THD, especially for a switching frequency of 200Hz. Hence, unipolar PWM was adopted for the study of this thesis. By modifying the timing of the gating waveforms to the power transistors in the inverter, it is possible to produce unipolar PWM (see for example Figure 4-3), as can be done by the PWM block in the SimuLink model of Figure 3-3.

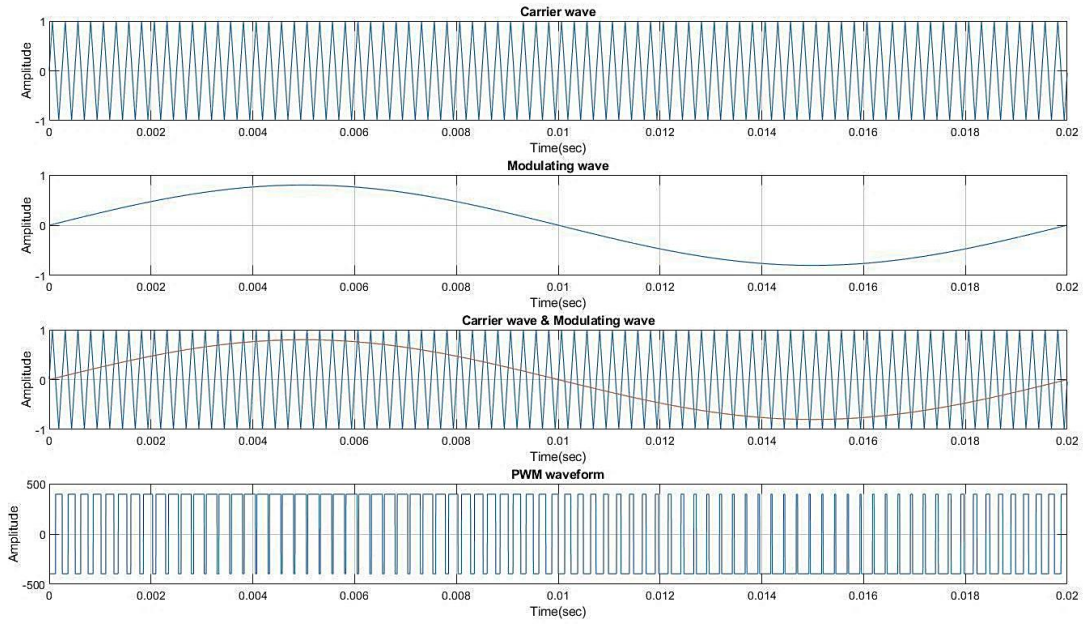


Figure 3-4 Illustration of bipolar PWM

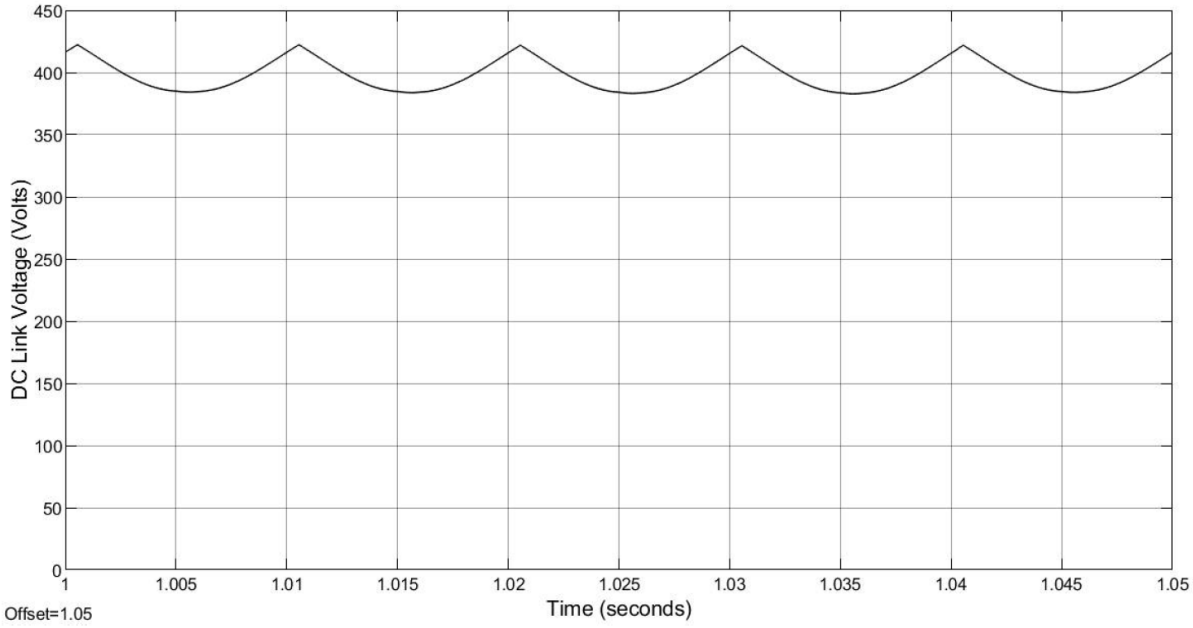
Note: the bottom plot illustrates the H bridge output waveform for a DC source of 500V.

Chapter 4: Simulation Results and Analysis

4.1 SIMULATED INVERTER WAVEFORMS

Shown in Figures 4-1 to 4-12 are the H Bridge output voltage (or DC Link voltage in the case of high switching frequencies) and load voltage waveforms for power outputs of 200W, 9W and 3.5W, and switching frequencies of 20kHz, 10kHz, 2.5kHz, and 200Hz. The load voltage is across the load resistance and the sin amplitude reference parameter is the amplitude of the sinusoidal reference waveform entering the pulse width modulator (see Figure 3-3). As noted above, to provide a more realistic simulation of the inverter operation, the first stage DC to DC converter is modelled as a Push Pull converter. Although bipolar pulse width modulation was initially investigated, it was observed that the load distortion can be significantly reduced by the use of unipolar pulse width modulation, especially for a switching frequency of 200Hz. Also as noted above, in this thesis MOSFET power switching devices are employed in both stages of power converter under study.

Note for the figures that display the DC Link voltage, that the ripple frequency is 100Hz (i.e., twice the power frequency) as discussed in Section 2.3.3 above. The 100Hz ripple is quite significant; that ripple is coupled back to the DC Link from the 50Hz power frequency output.



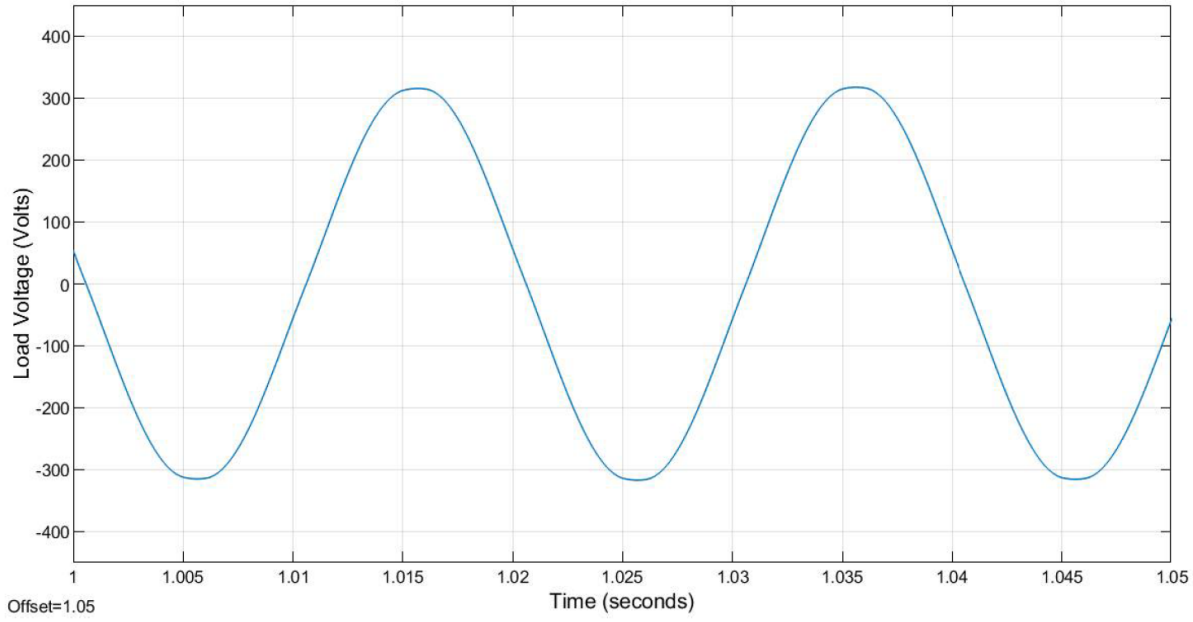


Figure 4-1 Steady state DC Link voltage and Load voltage waveforms for 200W, 20,000Hz Sin reference amplitude = 0.405, Load voltage RMS = 226.3V, Load voltage THD = 1.27%

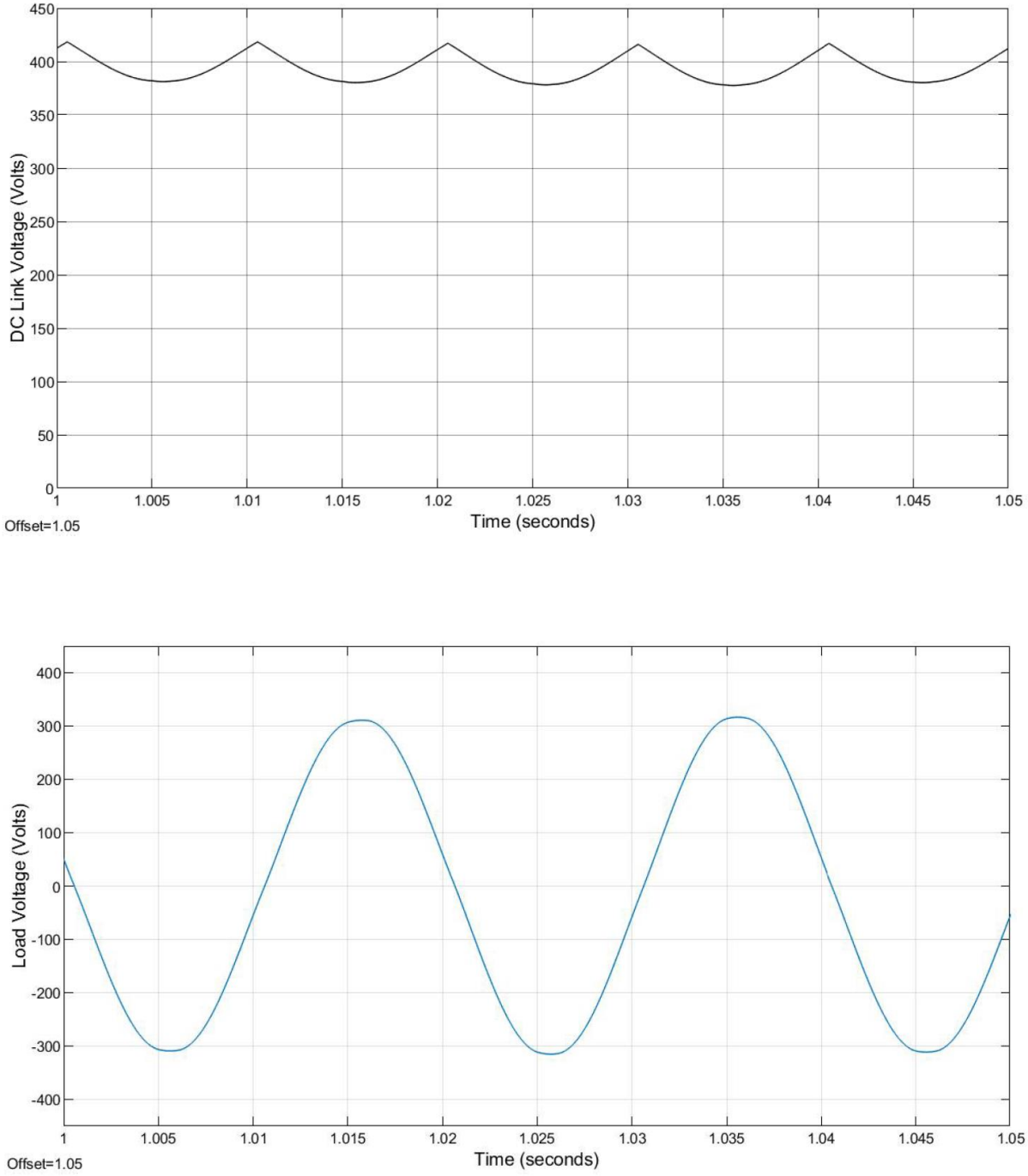
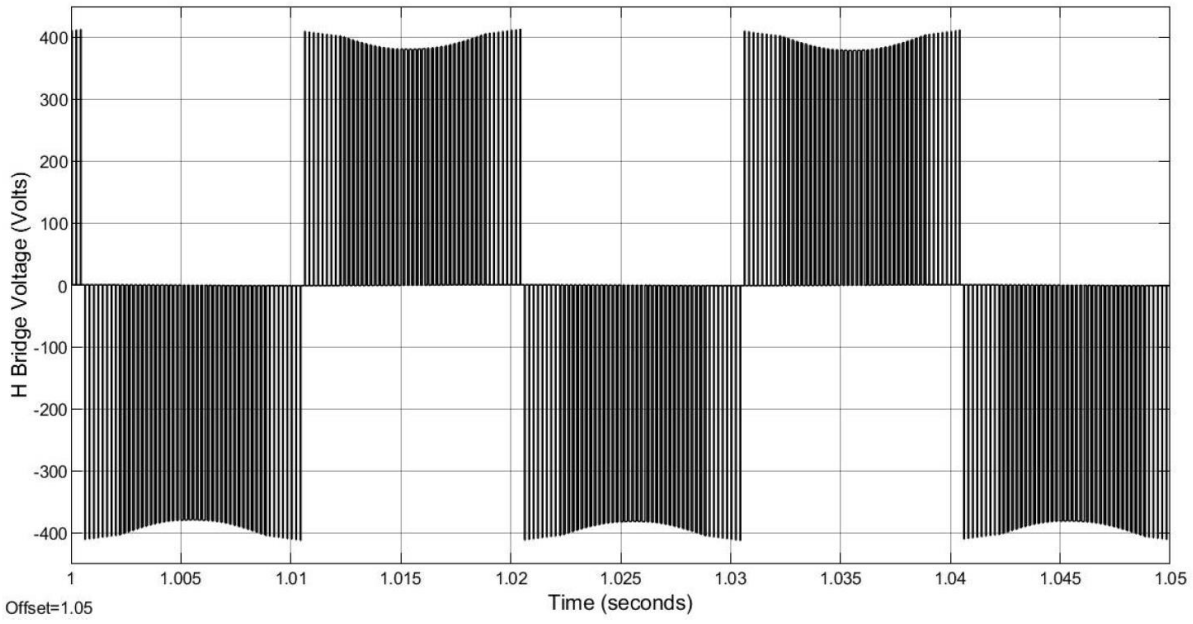


Figure 4-2 Steady state DC Link voltage and Load voltage waveforms for 200W, 10,000Hz Sin reference amplitude = 0.405, Load voltage RMS = 224.3V, Load voltage THD = 1.52%



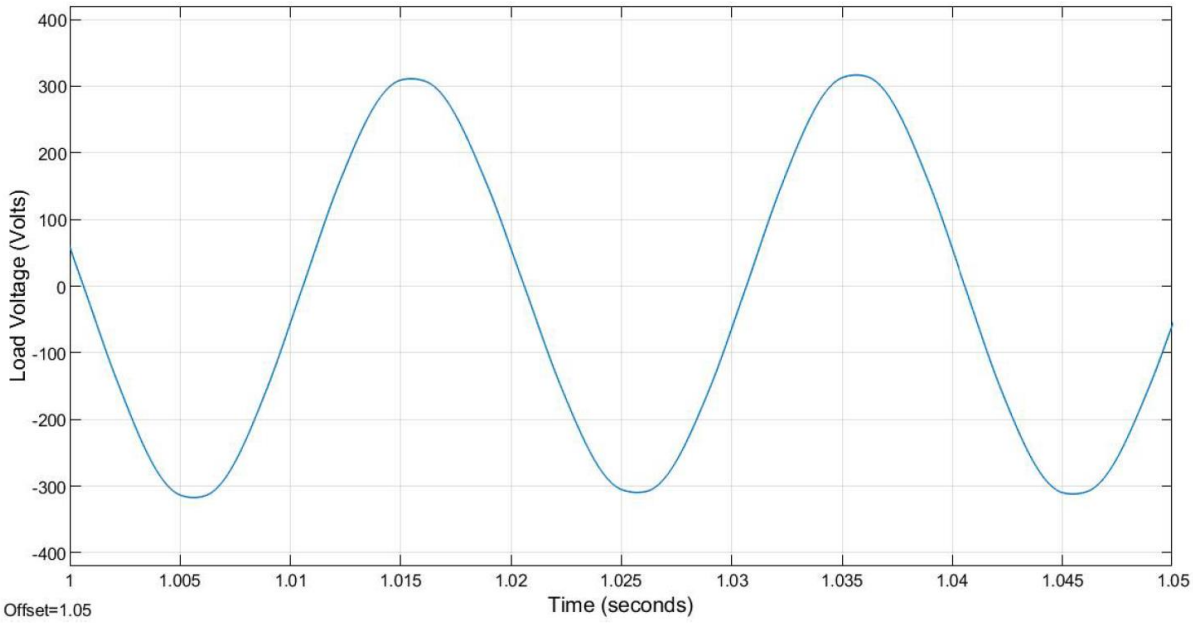
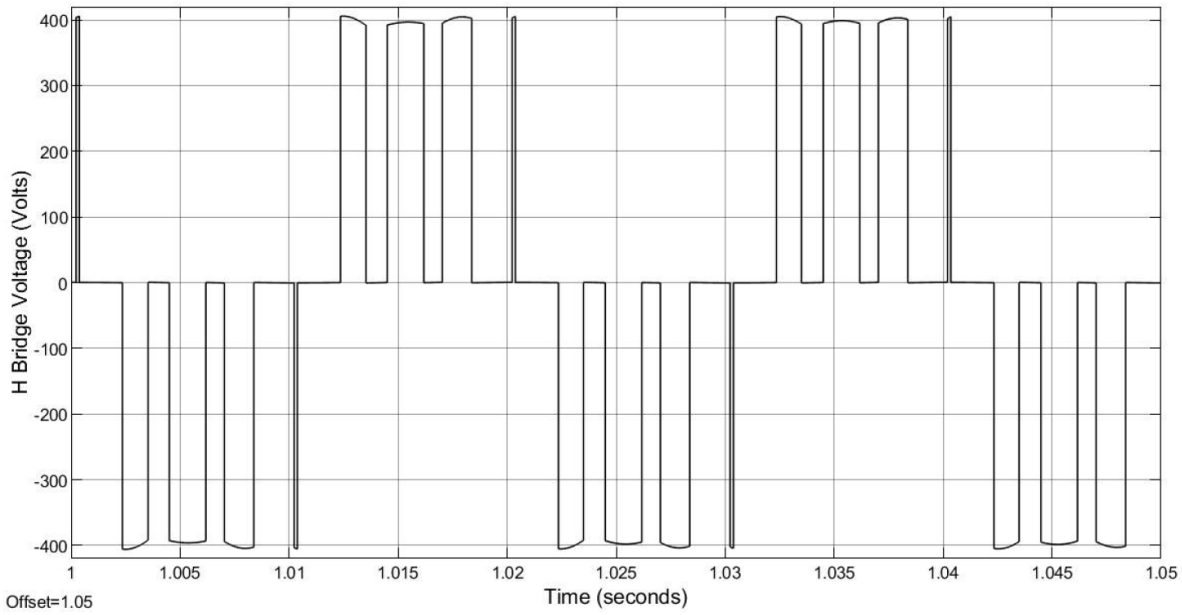


Figure 4-3 Steady state H Bridge and Load voltage waveforms for 200W, 2500Hz

Sin reference amplitude = 0.507, Load voltage RMS = 222.7V, Load voltage THD = 1.80%



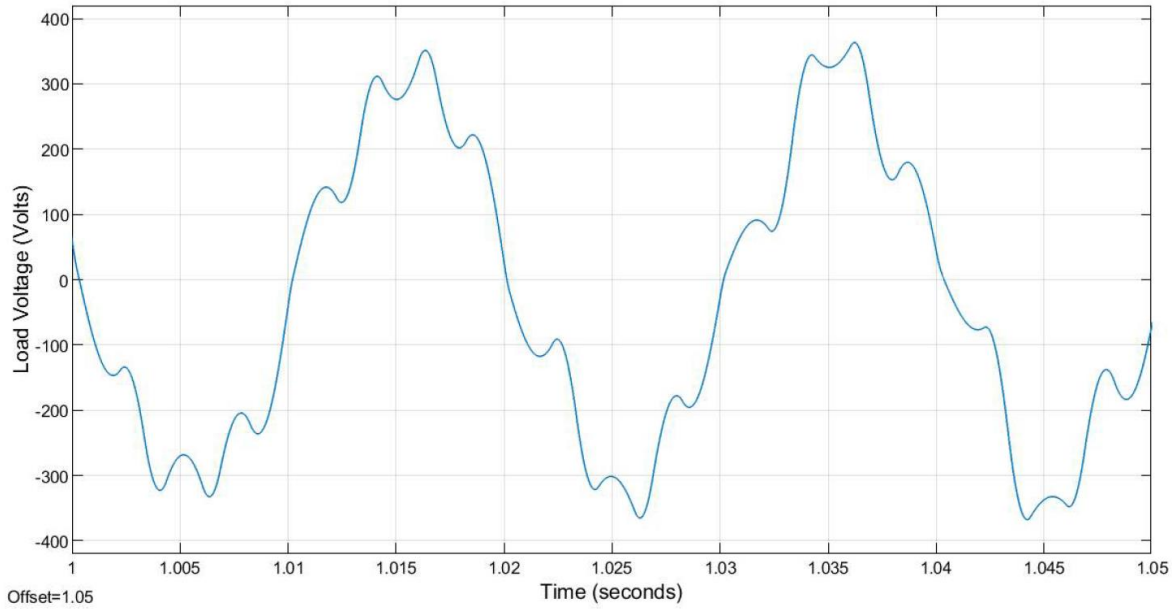


Figure 4-4 Steady state H Bridge and Load voltage waveforms for 200W, 200Hz

Sin reference amplitude = 0.700, Load voltage RMS = 222.4V, Load voltage THD = 17.14%

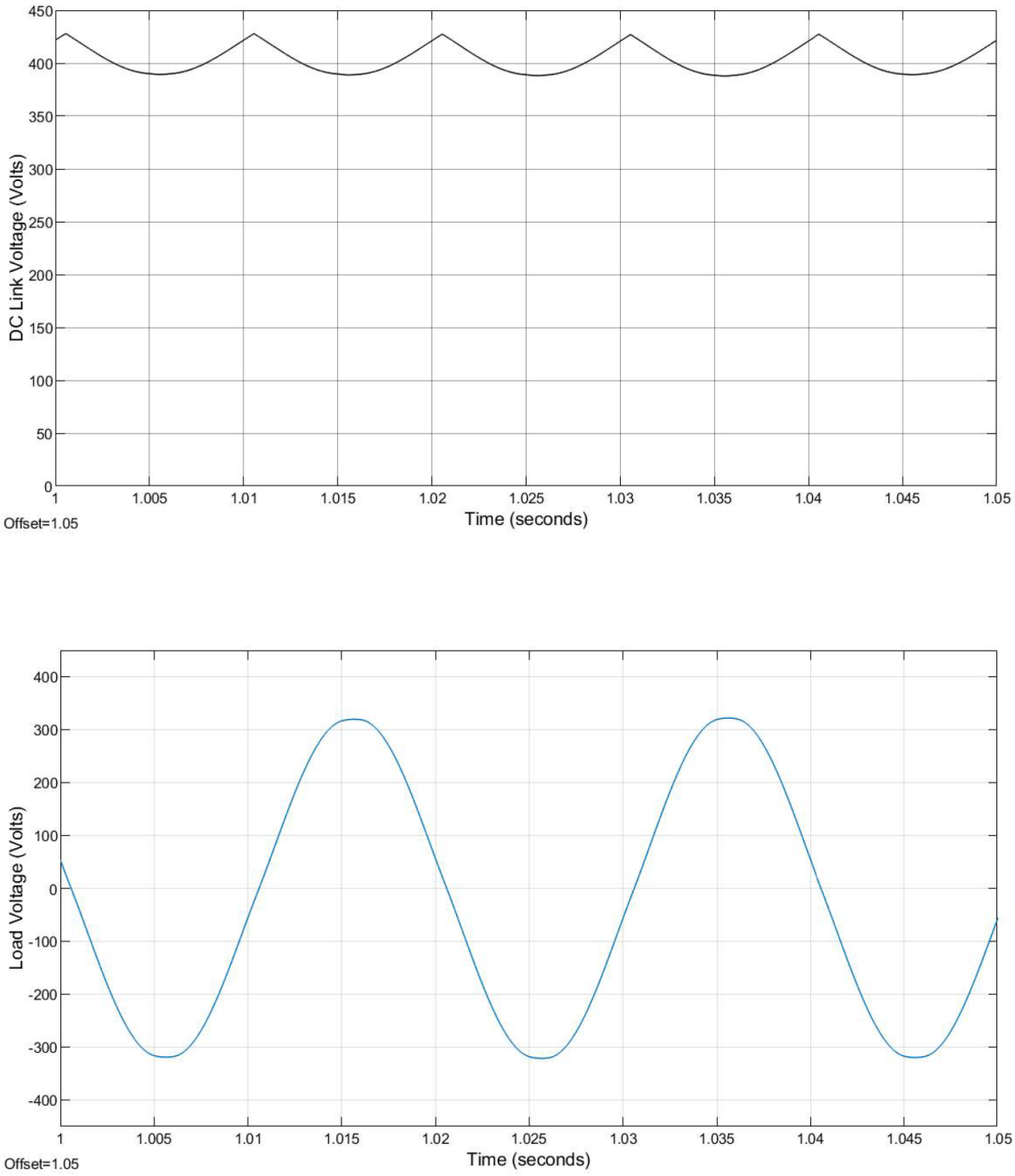
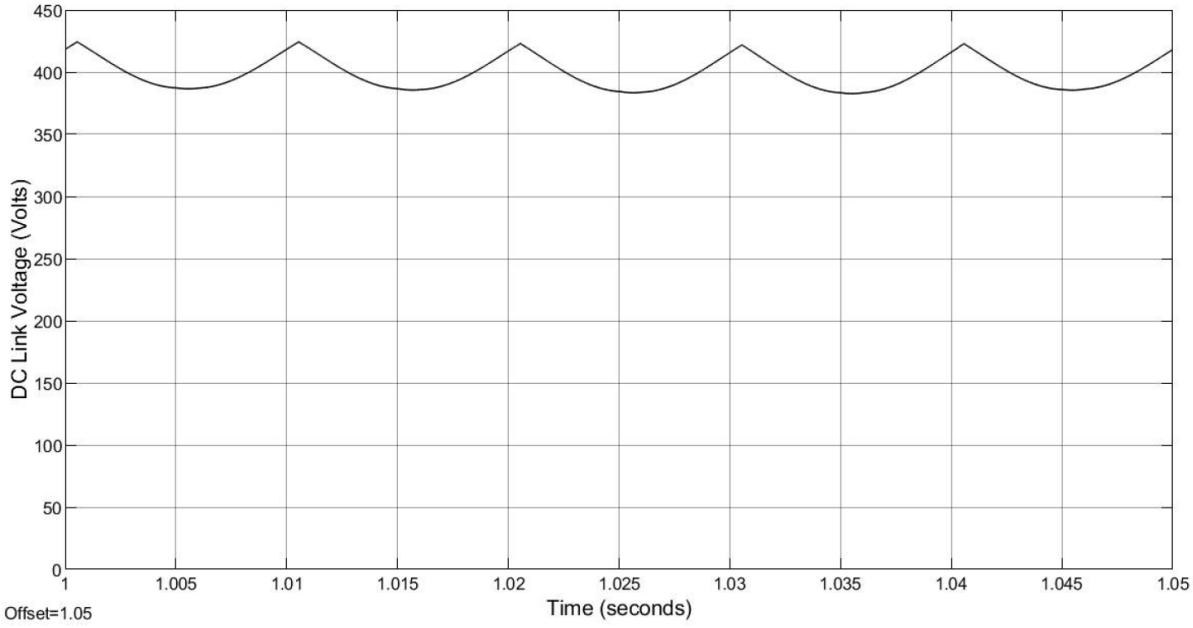


Figure 4-5 Steady state DC Link voltage and Load voltage waveforms for 9W, 20,000Hz Sin reference amplitude = 0.405, Load voltage RMS = 229.4V, Load voltage THD = 1.27%



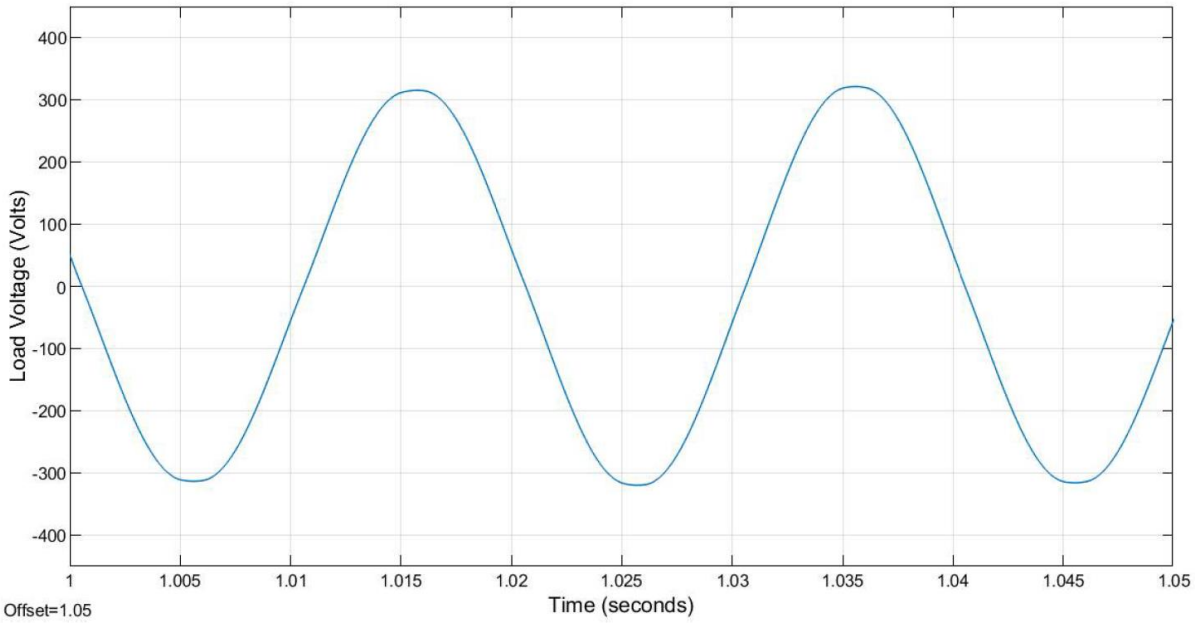


Figure 4-6 Steady state DC Link voltage and Load voltage waveforms for 10,000Hz, 9W

Sin reference amplitude = 0.405, Load voltage RMS = 227.5V, Load voltage THD = 1.54%

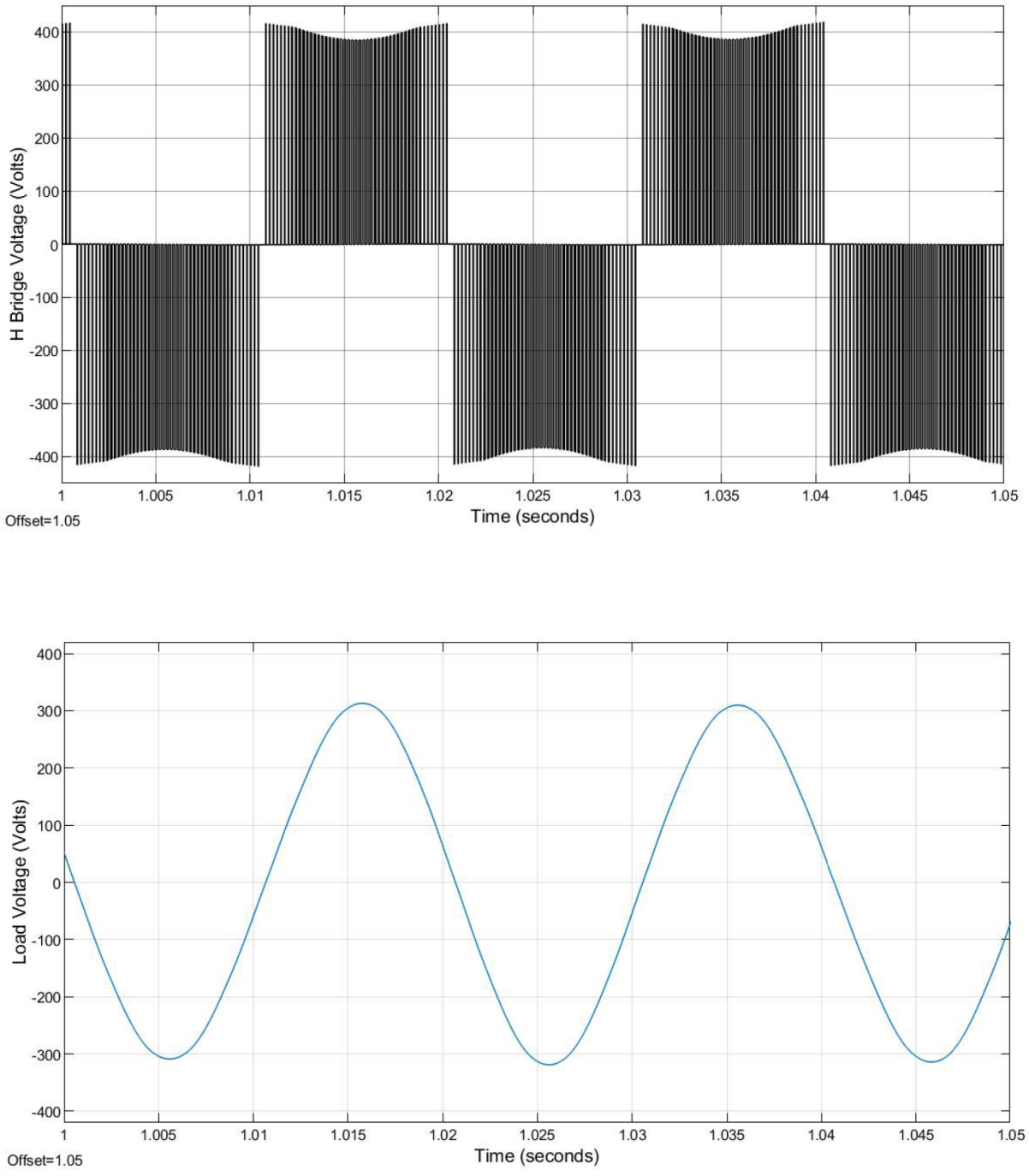


Figure 4-7 Steady state H Bridge and Load voltage waveforms for 9W, 2500Hz

Sin reference amplitude = 0.507, Load voltage RMS = 219.3V Load voltage THD = 2.88%

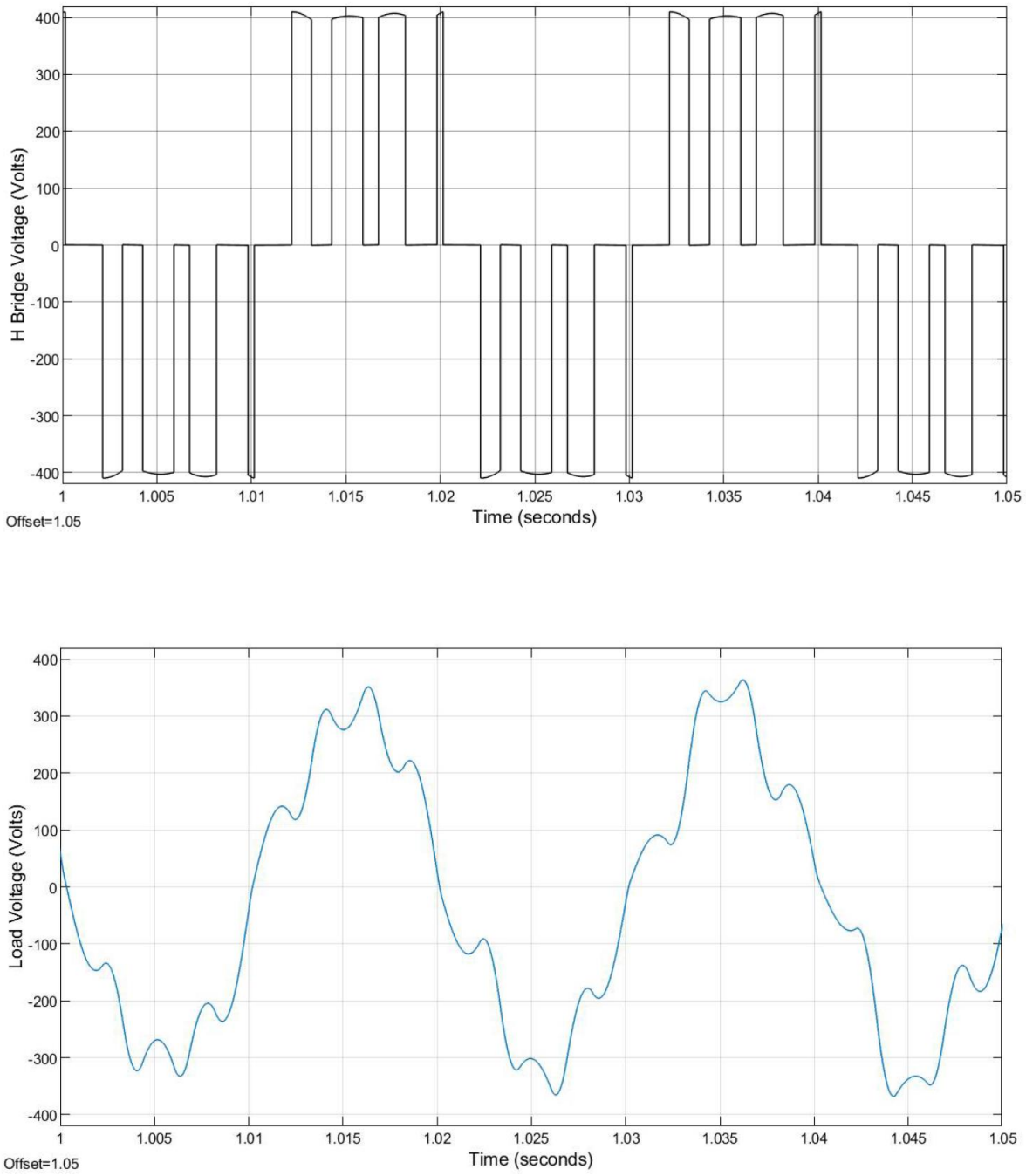


Figure 4-8 Steady state H Bridge and Load voltage waveforms for 9W, 200Hz

Sin reference amplitude = 0.700, Load voltage RMS = 224.2V, Load voltage THD = 23.03%

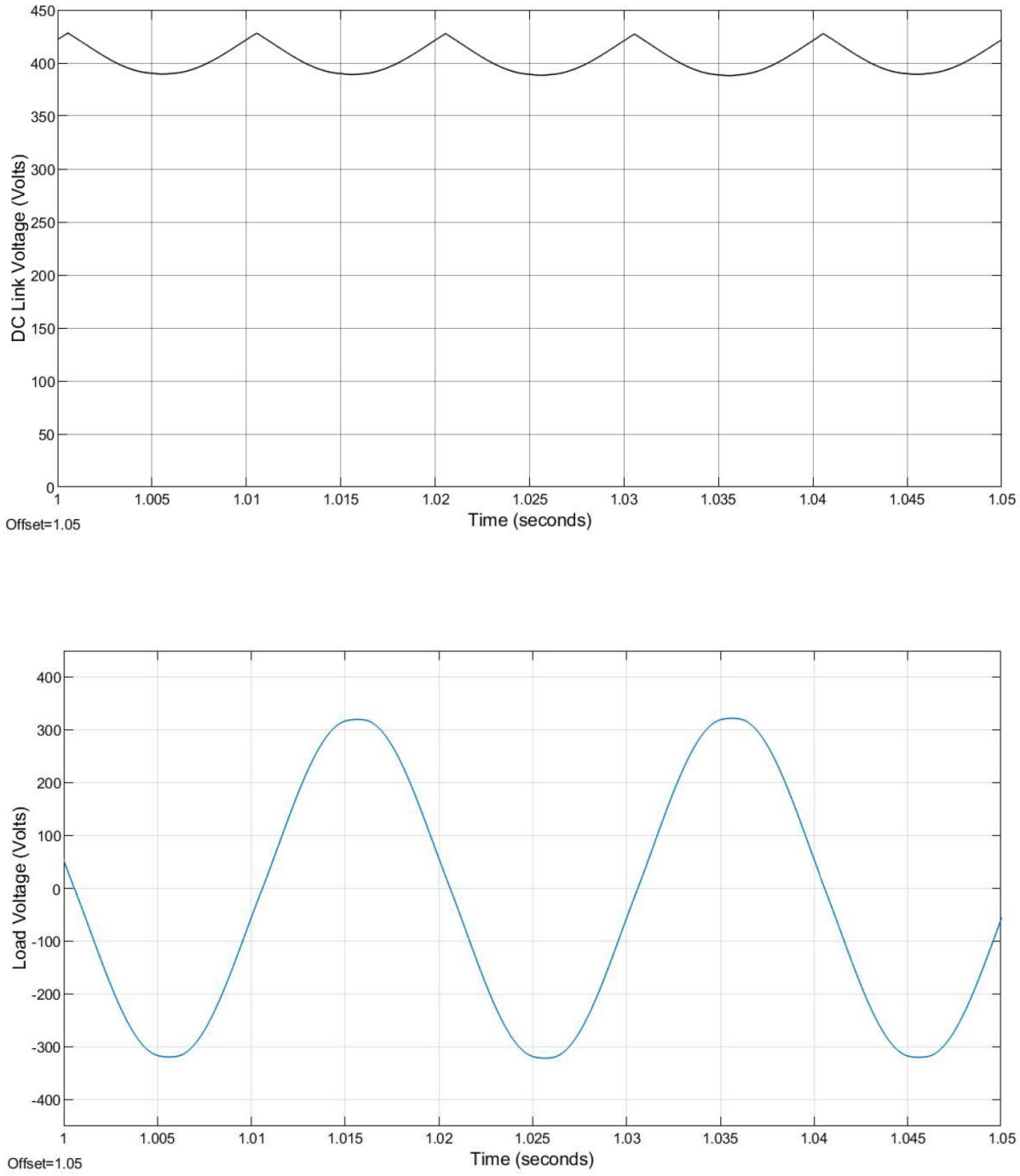


Figure 4-9 Steady state DC Link voltage and Load voltage waveforms for 3.5W, 20,000Hz Sin reference amplitude = 0.405, Load voltage RMS = 229.5V, Load voltage THD = 1.27%

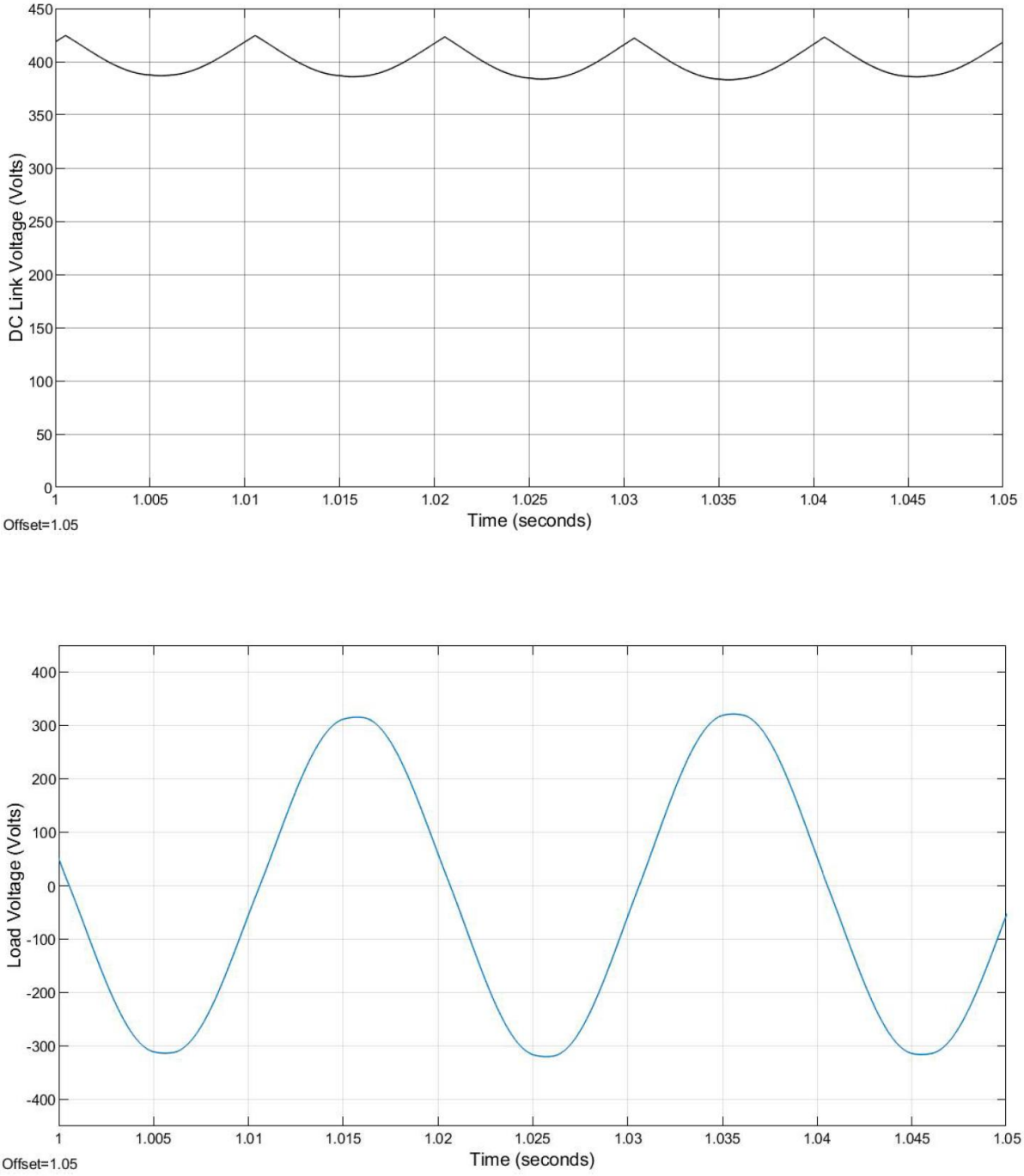


Figure 4-10 Steady state DC Link voltage and Load voltage waveforms for 3.5W, 10,000Hz Sin reference amplitude = 0.405, Load voltage RMS = 227.6V, Load voltage THD = 1.54%

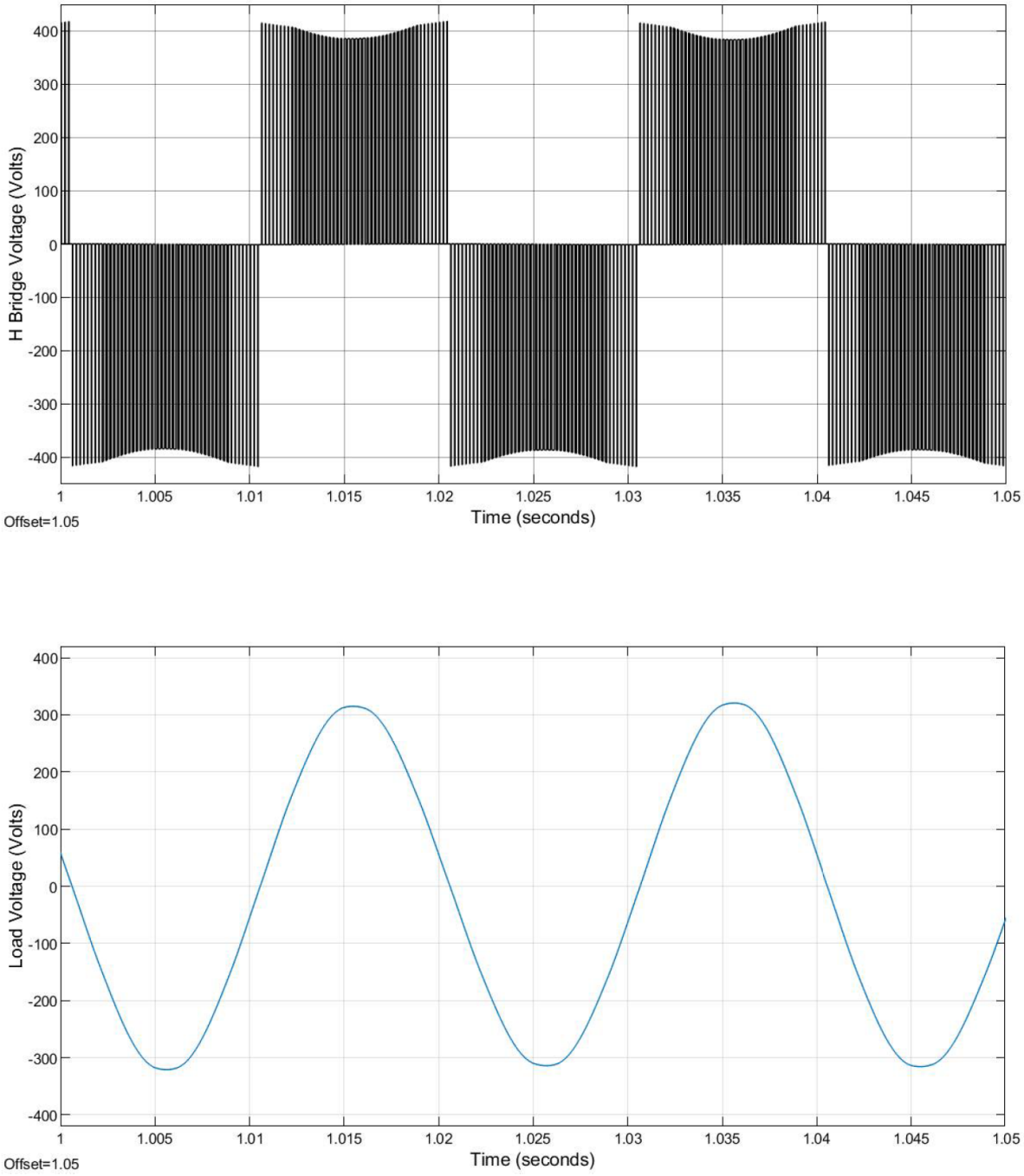


Figure 4-11 Steady state H Bridge and Load voltage waveforms for 3.5W, 2500Hz

Sin reference amplitude = 0.507, Load voltage RMS = 225.4V, Load voltage THD = 1.68%

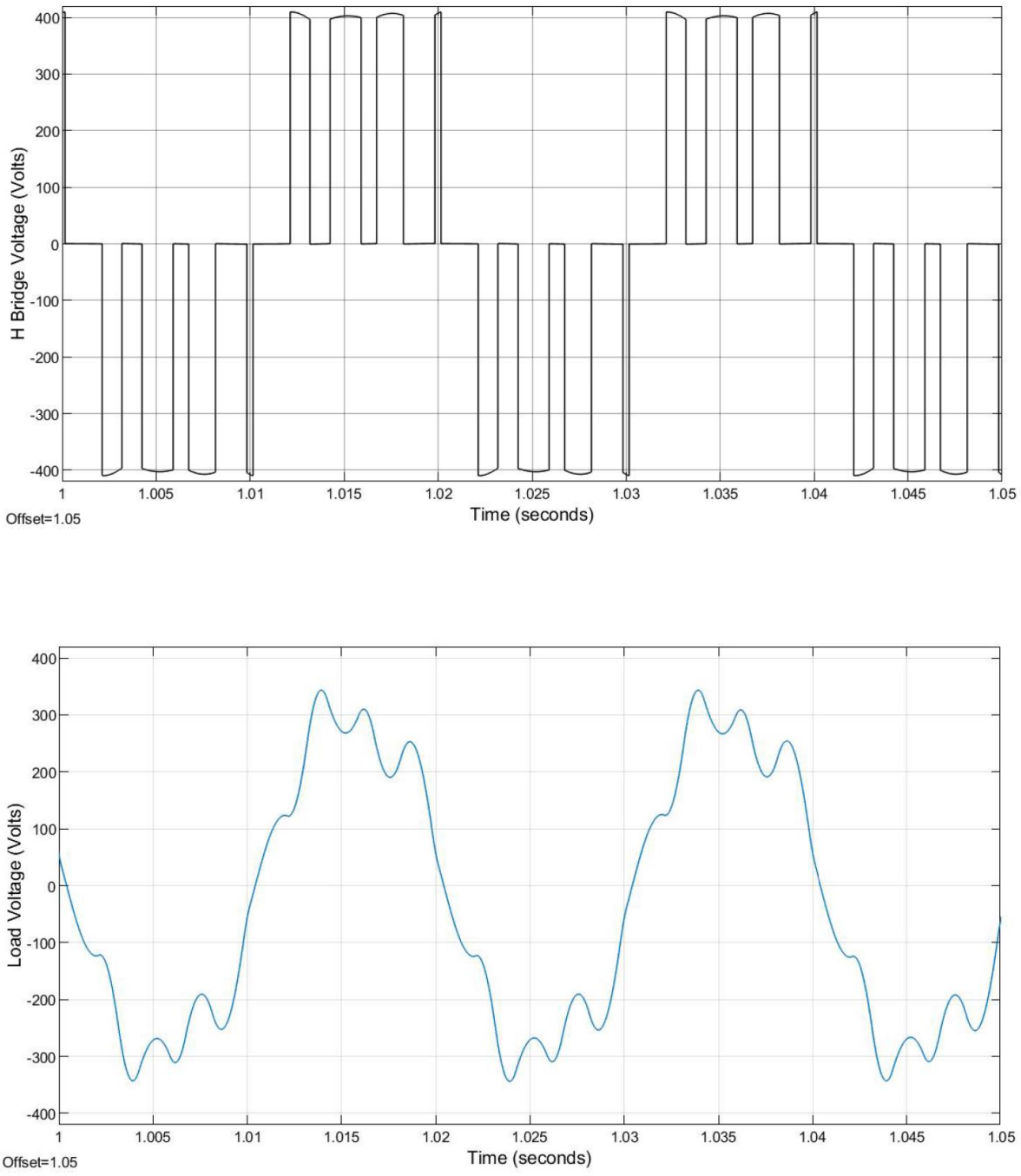


Figure 4-12 Steady state H Bridge and Load voltage waveforms for 3.5W, 200Hz

Sin reference amplitude = 0.700, Load voltage RMS = 224.7V, Load voltage THD = 19.71%

4.2 EFFICIENCY OF THE INVERTER FROM SIMULATION

Shown in Table 4-1 is a summary of inverter efficiency values as a function of power output (to the resistor load) of 200W, 9W and 3.5W for switching frequencies of 20kHz, 10kHz, 2.5kHz, 200Hz, as obtained from steady state simulation in SimuLink, as described in Chapter 3, and corresponding to Figures 4-1 to 4-12 above.

Table 4-1 Inverter Efficiency as a Function of Load Power & Switching Frequency

Load Power	Switching Frequency (kHz)	Output Power (W)	Total Loss (W)	Input Power (W)	Efficiency (%)
Rated Load (200W)	20	200.3	40.77	241.07	83.1%
	10	200.5	29.41	229.91	87.2%
	2.5	200.8	21.38	222.18	90.4%
	0.2	203.8	16.17	219.97	92.6%
CFL Load (9W)	20	9.02	5.18	14.20	63.5%
	10	9.03	3.36	12.39	72.9%
	2.5	9.00	2.66	11.66	77.2%
	0.2	9.16	1.83	10.99	83.3%
LED Load (3.5W)	20	3.51	2.41	5.92	59.3%
	10	3.51	1.64	5.15	68.2%
	2.5	3.52	1.36	4.88	72.1%
	0.2	3.57	1.05	4.62	77.3%

4.3 INTERPRETATION OF SIMULATION EFFICIENCY FINDINGS

As expected, the DC Link voltage ripple is at a frequency of 100Hz (twice the 50Hz power frequency). An interesting observation, to begin with, is the high ripple of the DC Link voltage. This was intentional, so as to keep costs down for a remote village application, by having the DC Link capacitor as small as possible.

Regarding the losses within the inverter, a discussion of relevant losses is provided in Appendix A. Note that drive losses are relatively independent of the switching frequency and load power. Conduction losses are relatively independent of switching frequency however, they are very dependent on loading, following an I^2R relationship. Hence a change in load current by a factor of one half produces a change in conduction losses by a factor of one quarter. Switching losses are directly proportional to the switching frequency. Thus, the results observed in this chapter, as expected, have a non-linear, and strong dependence on switching frequency.

The results shown in Figures 4-1 to 4-12, and Table 4-1 indicate that efficiency can be increased to address battery sizing in a remote village residential battery-based PV installation. In particular, note in the case of a 3.5W system output power, that efficiency in increased from 59.3% to 77.3% when the inverter switching frequency is decreased from 20kHz to 200Hz with corresponding DC Link power of 5.92W and 4.62W respectively. If one considers a 200W system with Push Pull first stage operating at constant efficiency, for example 70% (simply for illustrative purposes), then the power draw from the battery would be 5.92/0.70 = 8.57W for a 20kHz switching frequency and 4.62/0.70 = 6.60W for a 200Hz switching frequency. Then in the case of a battery voltage at the nominal value of 12.0V, the Amp-hours delivered by the battery in 12 hours of

operation would be 8.57W/12V x 12 hours = 8.57 Ah for the case of a switching frequency of 20kHz, and 6.60W/12V x 12 hours = 6.60 Ah for the case of a switching frequency of 200Hz. For example, assuming a lead acid battery, with an overnight discharge from 75% state of charge to 50% state of charge, the Amp-hour ratings would be 8.57 Ah x 1/(0.75 – 0.50) = 34.28 Ah in the case of a switching frequency of 20kHz, and be 6.60 Ah x 1/(0.75 – 0.50) = 26.4 Ah in the case of a switching frequency of 200Hz. Of course, the above analysis of battery Amp-hour rating may depend on other factors when designing the PV system for a remote village home. Nonetheless, the above analysis indicates that the battery sizing may be reduced significantly (from 34.28 Ah to 26.4 Ah for the example just discussed) by the employment of switching frequency reduction from 20kHz to 200Hz at the low power level of 3.5W.

Chapter 5: Conclusion and Future Work

5.1 SUMMARY OF THE THESIS

The research underlying this thesis is based on the issue of battery sizing of a photovoltaic energy system for a remote village residence. If the inverter efficiency can be increased at low power levels , such as operation of a single LED light (rated at 3.5W) through the night, it may be possible to reduce the Amp-hour rating of the battery, and thus result in a more cost-effective photovoltaic system for the residence. A 200W MOSFET Full Bridge inverter is modelled in SimuLink and characterised for operation at 200W, 9W and 3.5 W with a pure resistive load model. The switching frequency is set at four values: 20kHz, 10kHz, 2.5kHz, and 200Hz.

5.2 CONCLUSION

Using the SimuLink simulation, open loop control of a 200W MOSFET inverter is investigated with unipolar pulse width modulation and a sinusoidal modulating reference waveform, for 12 conditions of power loading and switching frequency variation. With a power output of 3.5W it is observed that inverter efficiency can be increased from 59% to 77% by changing the switching frequency from 20kHz to 200Hz. For the LC filter with L = 1mH and C = 1000μF, the distortion of the load voltage waveform is increased from 1.3% at a switching frequency of 20kHz to 20% at a switching frequency of 200Hz. Although it has not been determined if this level of THD is appropriate (perhaps even a larger distortion value may still allow a 3.5W 220VAC LED light to operate reliably), it has been shown that there is potential to reduce the Amp-hour rating of the battery by employing switching frequency reduction.

5.3 FUTURE WORK

The following avenues of research are suggested for future consideration.

1. Since the LC filter components (values of 1mH and 1000µF respectively) are modelled in SimuLink as lossless, the LC filter output power (i.e., the power to the resistive load) is equal to the H Bridge output power. However a more realistic model of system losses would include losses in the LC filter.
2. In addition, it would be worthwhile to investigate the trade-off in changing the values of the LC filter components (while keeping constant the low pass corner frequency of 159Hz), and the effect on the physical size and cost of those L and C components.
3. Another trade-off worth examining is the effect of the LC low pass corner frequency and load distortion at lower switching frequencies.
4. In addition, it would be very worthwhile to study in greater detail, all the sources of losses, including transistor/diode switching, conduction, drive losses etc.
5. The Push Pull DC to DC converter models a realistic DC link voltage in the SimuLink model, however the switching frequency is constant at 10kHz. It would be interesting to see if the concept of reduced switching frequency could be applied to the first stage Push Pull converter. And of course, to model power losses in the first stage converter.
6. The DC Link voltage, has an AC ripple frequency is 100Hz (i.e., twice the power frequency). As a continuation of this thesis study, it would be worthwhile to investigate this 100Hz ripple further and to explore possible mitigation approaches.
7. An experimental implementation of the system would be valuable to not only determine how the simulation model might be improved upon, but also to investigate how much THD can be tolerated by a 220VAC 3.5W LED load.

8. As noted above, a very different approach that was not pursued in this thesis, is the design a completely separate 12VDC to 220VAC converter, rated at 3.5W to operate just one LED light during the night. Thus, the 200W inverter system would be used during daylight hours and the 3.5W inverter would be used at night. Perhaps this approach might be investigated.

References

Abdelhakim, A., Mattavelli, P., Davari, P., & Blaabjerg, F. (2018). Performance evaluation of the single-phase split-source inverter using an alternative DC–AC configuration. *IEEE Transactions on Industrial Electronics*, 65(1), 363–373. https://doi.org/10.1109/TIE.2017.2714122

Abdelhakim, A., Mattavelli, P., & Spiazzi, G. (2016). Three-phase split-source inverter (SSI): Analysis and modulation. *IEEE Transactions on Power Electronics*, 31(11), 7451–7461. https://doi.org/10.1109/TPEL.2015.2513204

Akbar, F., Cha, H., Ahmed, H. F., & Khan, A. A. (2020). A family of single-stage high-gain dual-buck split-source inverters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(2), 1701–1713. https://doi.org/10.1109/JESTPE.2019.2894384

Anderson, J., & Peng, F. Z. (2008). Four quasi-Z-source inverters. *IEEE Power Electronics Specialists Conference (PESC)*, 2743–2749. https://doi.org/10.1109/PESC.2008.4592360

Ansari, S. A., Skandari, A., Milimonfared, J., & Moghani, J. S. (2018). A new control method for an interleaved flyback inverter to achieve high efficiency and low output current THD. *IEEE 9th Annual Power Electronics, Drives Systems and Technologies Conference (PEDSTC)*, 89–94. https://doi.org/10.1109/PEDSTC.2018.8343777

Babu, S. M., Veeramallu, V. K. S., Narasimharaju, B. L., Rathore, A. K., & Krishnamoorthy, H. S. (2020). Novel non-isolated differential buck-boost inverter with single-stage conversion and reduced device voltage stress. *IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE)*, 1–5. https://doi.org/10.1109/PESGRE45664.2020.9070643

Bhattacharya, A. (2016). 3-level Z-source inverter based PV system with bidirectional buck-boost BESS. *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 1–6. https://doi.org/10.1109/PEDES.2016.7914263

Bhattacharya, S., Sharma, S. K., Mascarella, D., & Joos, G. (2017). Subfundamental cycle switching frequency variation for switching losses reduction of a two-level inverter traction drive. *IEEE Transactions on Transportation Electrification*, 3(3), 646–655. https://doi.org/10.1109/TTE.2017.2695576

Bose, B.K., Szczesny, P.M., & Steigerwald, R.L. (1985). Microcomputer control of a residential photovoltaic power conditioning system. *IEEE Transactions on Industry Applications*, 21(5), 1182–1191. https://doi.org/ doi.org/10.1109/TIA.1985.349522

Caceres, R. O., & Barbi, I. (1999). A boost DC-AC converter: analysis, design, and experimentation. *IEEE Transactions on Power Electronics*, 14(1), 134–141. https://doi.org/10.1109/63.737601

Chamarthi, P. K., Rajeev, M., & Agarwal, V. (2015). A novel single stage zero leakage current transformer-less inverter for grid connected PV systems. *IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, 1–5. https://doi.org/10.1109/PVSC.2015.7356292

Darwish, A., Massoud, A. M., Holliday, D., Ahmed, S., & Williams, B. W. (2016). Single-stage three-phase differential-mode buck-boost inverters with continuous input current for PV applications. *IEEE Transactions on Power Electronics*, 31(12), 8218–8236. https://doi.org/10.1109/TPEL.2016.2516255

De, S., Banerjee, D., Siva Kumar, K., Gopakumar, K., Ramchand, R., & Patel, C. (2011). Multilevel inverters for low-power application. *IET Power Electronics*, 4(4), 384–392. https://doi.org/10.1049/iet-pel.2010.0027

Ding, X., Liu, Y., Zhao, D., & Wu, W. (2020). Generalized Cockcroft-Walton Multiplier Voltage Z-Source Inverters. *IEEE Transactions on Power Electronics*, 35(7), 7175–7190. https://doi.org/10.1109/TPEL.2019.2957018

Dogga, R., & Pathak, M. K. (2019). Recent trends in solar PV inverter topologies. *Elsevier Solar Energy*, 183(2), 57–73. https://doi.org/10.1016/j.solener.2019.02.065

Effah, F. B., Wheeler, P. W., Watson, A. J., & Clare, J. C. (2017). Quasi Z-source NPC inverter for PV application. *2017 IEEE PES PowerAfrica*, 153–158. https://doi.org/10.1109/PowerAfrica.2017.7991215

Ellabban, O., & Abu-Rub, H. (2016). Z-source inverter: Topology improvements review. *IEEE Industrial Electronics Magazine*, 10(1), 6–24. https://doi.org/10.1109/MIE.2015.2475475

Eskandari, B., Azizi, M., Roostaee, M., & Joorabi, M. K. (2020). Non-linear modulation for high gain three-phase boost inverter. *IEEE 11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC)*, 1–6. https://doi.org/10.1109/PEDSTC49159.2020.9088493

Faraji, F., Mousavi G., S. M., Hajirayat, A., Birjandi, A. A. M., & Al-Haddad, K. (2017). Single-stage single-phase three-level neutral-point-clamped transformerless grid-connected photovoltaic inverters: Topology review. *Renewable and Sustainable Energy Reviews*, 80(3), 197–214. https://doi.org/10.1016/j.rser.2017.05.181

Fathi, H., & Madadi, H. (2016). Enhanced-boost Z-source inverters with switched Z-impedance. *IEEE Transactions on Industrial Electronics*, 63(2), 691–703. https://doi.org/10.1109/TIE.2015.2477346

Gao, F., Ge, X., & Wang, J. (2013). A single-stage buck-boost three-level neutral-point-clamped inverter for the grid-tied photovoltaic power generation. *IEEE Energy Conversion Congress and Exposition (ECCE)*, 547–553. https://doi.org/10.1109/ECCE.2013.6646749

GoHz. (2016). *Power Inverter Basics*, GoHz.com. http://www.gohz.com/power-inverter-basics

Han, J., Zhou, X., Lu, S., & Zhao, P. (2020). A three-phase bidirectional grid-connected AC/DC converter for V2G applications. *Hindawi Journal of Control Science and Engineering*, published Sept. 7, 1–12. https://doi.org/10.1155/2020/8844073

Hinz, H., Mutschler, P. (1996). Single phase voltage source inverters without transformer in photovoltaic applications. *IEEE Power Electronics and Motion Control Conference (PEMC)*, 161– 165. https://nanopdf.com/download/voltage-source-inverters-for-grid-connected-photovoltaic-systems_pdf

Huang, Y., Shen, M., Peng, F. Z., & Wang, J. (2006). Z-Source Inverter for Residential Photovoltaic Systems. *IEEE Transactions on Power Electronics*, 21(6), 1776–1782. https://doi.org/10.1109/TPEL.2006.882913

Husev, O., Blaabjerg, F., Roncero-Clemente, C., Romero-Cadaval, E., Vinnikov, D., Siwakoti, Y. P., & Strzelecki, R. (2016). Comparison of impedance-source networks for two and multilevel buck-boost inverter applications. *IEEE Transactions on Power Electronics*, 31(11), 7564–7579. https://doi.org/10.1109/TPEL.2016.2569437

Jagan, V., Kotturu, J., & Das, S. (2017). Enhanced-boost quasi-Z-source inverters with two-switched impedance networks. *IEEE Transactions on Industrial Electronics*, 64(9), 6885–6897. https://doi.org/10.1109/TIE.2017.2688964

Jana, J., Saha, H., & Das Bhattacharya, K. (2017). A review of inverter topologies for single-phase grid-connected photovoltaic systems. *Elsevier Renewable and Sustainable Energy Reviews, 72*, available online Nov. 5, 2016, 1256–1270. https://doi.org/10.1016/j.rser.2016.10.049

Khaligh, Alireza & Onar, Omer C. (2010). *Energy harvesting: Solar, wind, and ocean energy conversion systems*. Taylor & Francis Group LLC.

Khan, A. A., Cha, H., Khan, U. A., & Kim, H.-G. (2017). Four-switch buck-boost inverter for stand-alone and grid-connected single-phase PV systems. *IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia)*, 460–465.

Khan, A. A., Eberle, W., Wang, L., Akbar, F., Khan, U. A., Lu, Y. W., & Agamy, M. (2019). Coupled-inductor buck–boost inverter with reduced current ripple. *IEEE Transactions on Power Electronics*, 35(8), 7933–7946. https://doi.org/10.1109/IFEEC.2017.7992082

Khan, M. N. H., Forouzesh, M., Siwakoti, Y. P., Li, L., Kerekes, T., & Blaabjerg, F. (2020). Transformerless inverter topologies for single-phase photovoltaic systems: A comparative review. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(1), 805–835. https://doi.org/10.1109/JESTPE.2019.2908672

Lee, S. S. (2018). Single-stage switched-capacitor module (S^3CM) topology for cascaded multilevel inverter. *IEEE Transactions on Power Electronics*, 33(10), 8204–8207. https://doi.org/10.1109/TPEL.2018.2805685

Li, H., Zhang, K., Zhao, H., Fan, S., & Xiong, J. (2013). Active power decoupling for high-power single-phase PWM rectifiers. *IEEE Transactions on Power Electronics*, 28(3), 1308–1319. https://doi.org/10.1109/TPEL.2012.2208764

Liu, B., Song, D., He, D., Song, S., Yang, J., Su, M., Lu, Y., Chen, Y., & Liu, H. (2019). A modified modulation for single-phase photovoltaic/battery inverter to improve AC power quality with low DC-link capacitance. *Elsevier International Journal of Electrical Power & Energy Systems*, 110, available online April 2, 2019, 705–712. https://doi.org/10.1016/j.ijepes.2019.03.048

Loba, Tahsina H. (2015). *Improving Inverter Efficiency at Low Power Using a Reduced Switching Frequency*. MSc thesis, University of Calgary. https://prism.ucalgary.ca/handle/11023/2455

Loba, T. H., Wood, D. H., & Nowicki, E. P. (2015). Improving inverter efficiency at low power by reducing switching frequency. *IEEE 28th Canadian Conference on Electrical and Computer Engineering*, 859–863. https://doi.org/10.1109/CCECE.2015.7129387

Manoj, P., Kirubakaran, A., Dhara, S., & Somasekhar, V. T. (2022). A quasi-Z-source based space vector modulated cascaded four-level inverter for photovoltaic applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10(4), 4749–4762. https://doi.org/10.1109/JESTPE.2021.3125695

Mansour, A. S., & Osheba D.S.M. (2019). Performance of a single-stage buck-boost inverter fed from a photovoltaic source under different meteorological conditions. *IEEE 21st International Middle East Power Systems Conference (MEPCON)*, 151–157. https://doi.org/10.1109/MEPCON47431.2019.9008200

Nahavandi, A., Roostaee, M., & Azizi, M. R. (2016). Single stage DC-AC boost converter. *IEEE 7th Power Electronics, Drive Systems and Technologies Conference (PEDSTC)*, 362–366. https://doi.org/10.1109/PEDSTC.2016.7556888

Nguyen, M. K., Lim, Y. C., & Park, S. J. (2015). A comparison between single-phase quasi-Z-source and quasi-switched boost inverters. *IEEE Transactions on Industrial Electronics*, 62(10), 6336–6344. https://doi.org/10.1109/TIE.2015.2424201

Nguyen, M. K., & Tran, T. T. (2018). A single-phase single-stage switched-boost inverter with four switches. *IEEE Transactions on Power Electronics*, 33(8), 6769–6781. https://doi.org/10.1109/TPEL.2017.2754547

Reddy, C. S., Purushotham, G. R., & Reddy, P. P. (2020). Classification of three-phase grid-tied microinverters in photovoltaic applications. *2nd International Conference on Innovations in Electrical & Electronics Engineering (ICIEEE)*, 90–99. https://www.iosrjournals.org/iosr-jeee/Papers/ICIEEE/12.90-99.pdf

Shawky, A., Ahmed, M., Orabi, M., & Aroudi, A. El. (2020). Classification of three-phase grid-tied microinverters in photovoltaic applications. *MDPI Energies*, 13(11), 2929–2940. https://doi.org/10.3390/en13112929

Shi, Y., Pan, Z., Rodrigues, R., & Wei, C. (2018). A low-cost single-stage PV inverter. *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 7(978), 387–392. https://doi.org/10.1109/APEC.2018.8341040

Shiluveru, K., Singh, A., Ahmad, A., & Singh, R. K. (2020). Hybrid buck-boost multioutput quasi-Z-source converter with dual DC and single AC outputs. *IEEE Transactions on Power Electronics*, 35(7), 7246–7260. https://doi.org/10.1109/TPEL.2019.2960268

Shimizu, T., Wada, K., Nakamura, N., 2006. Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the DC input for an AC photovoltaic module system. *IEEE Transactions on Power Electronics*, 21(5), 1264–1272. https://doi.org/10.1109/TPEL.2006.880247

Steinmetz, M. (2013). Parallel Switch Increases Efficiency of Power Module for PV Inverters. *Power Electronics Europe* (Issue 5). www.power-mag.com and www.vincotech.com

Saha, S. & Sundarsingh, V. P. (1996). Novel grid-connected photovoltaic inverter. *IEE Proceedings - Generation, Transmission and Distribution*, 143(2), 219-224. https://doi.org/10.1049/ip-gtd:19960054

Tang, Y., Bai, Y., Kan, J., & Xu, F. (2017). Improved dual boost inverter with half cycle modulation. *IEEE Transactions on Power Electronics*, 32(10), 7543–7552. https://doi.org/10.1109/TPEL.2016.2592979

Tazay, Ahmad F. (2017). *Smart Inverter Control and Operation for Distributed Energy Resources*. Phd Dissertation, University of South Florida. http://search.proquest.com/openview/920bf36262446dfac155f1cbe293ae26/1?pq-origsite=gscholar&cbl=18750&diss=y

Tekgun, B., Tekgun, D., Alan, I., & Badawy, M. (2018). Design and control of a single phase DC/Rectified AC/AC inverter for low THD applications. *IEEE 7th International Conference on Renewable Energy Research and Applications (ICRERA)*, *5*, 424–430. https://doi.org/10.1109/ICRERA.2018.8566841

Trujillo, C. L., Velasco, D., Figueres, E., Garcerá, G., & Ortega, R. (2011). Modeling and control of a push-pull converter for photovoltaic microinverters operating in island mode. *Applied Energy*, 88(8), 2824–2834. https://doi.org/10.1016/j.apenergy.2011.01.053

U.S. Energy Information Administration. (2021). *International Energy Outlook 2021*. https://www.eia.gov/outlooks/ieo/

Vairavasundaram, I., Varadarajan, V., Pavankumar, P. J., Kanagavel, R. K., Ravi, L., & Vairavasundaram, S. (2021). A review on small power rating PV inverter topologies and smart PV inverters. *MDPI Electronics*, 10(11), 1296–1302. https://doi.org/10.3390/electronics10111296

Ventosa-Cutillas, A., Montero-Robina, P., Umbría, F., Cuesta, F., & Gordillo, F. (2019). Integrated control and modulation for three-level NPC rectifiers. *MDPI Energies*, 12(9), 1–15. https://doi.org/10.3390/en12091641

Wang, C. (2004). A novel single-stage full-bridge buck-boost inverter. *IEEE Transactions on Power Electronics*, 19(1), 150–159. https://doi.org/ 10.1109/TPEL.2003.820583

Xue, Y., Chang, L. (2004). Closed-loop SPWM control for grid-connected buck-boost inverters. *IEEE Power Electronics Specialists Conference (PESC)*, 3366–3371. https://doi.org/10.1109/PESC.2004.1355070

Yin, C., Ding, W., Ming, L., & Loh, P. C. (2021). Single-stage active split-source inverter with high DC-link voltage utilization. *IEEE Transactions on Power Electronics*, 36(6), 6699–6711. https://doi.org/10.1109/TPEL.2020.3038688

Zhang, S., Wang, Y., Chen, B., Xing, W., Qiu, H. (2016). An implementation of flexible topology strategy for an interleaved full-bridge LLC resonant converter in residential photovoltaic power systems. *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 3579– 3585. https://doi.org/https://doi.org/10.1109/IPEMC.2016.7512869

Zhang, Y., Liu, J., Li, X., Ma, X., Zhou, S., Wang, H., & Liu, Y.-F. (2018). An improved PWM strategy for Z-source inverter with maximum boost capability and minimum switching frequency. *IEEE Transactions on Power Electronics*, 33(1), 606–628. https://doi.org/10.1109/TPEL.2017.2661321

Zhang, Z., Chen, M., Gao, M., Mo, Q., & Qian, Z. (2011). An optimal control method for grid-connected photovoltaic micro-inverter to improve the efficiency at light-load condition. *IEEE Energy Conversion Congress and Exposition (ECCE)*, 219–224. https://doi.org/10.1109/ECCE.2011.6063772

Zhao, B; Abramovitz, A. (2017). High gain single stage buck-boost inverter. *20th International Conference on Electrical Machines and Systems (ICEMS)*, 1–5. https://doi.org/10.1109/ICEMS.2017.8056184

Zhu, X., Zhang, B., & Qiu, D. (2019). A high boost active switched quasi-Z-source inverter with low input current ripple. *IEEE Transactions on Industrial Informatics*, 15(9), 5341–5354. https://doi.org/10.1109/TII.2019.2899937

Appendix A Inverter Power Losses

The following discussion is from the thesis study of (Loba, 2015), and is reproduced here as a review for context of discussions in Chapter 4.

A-1 INVERTER LOSS COMPONENTS

Evaluating the losses associated with the inverter provides a clearer idea of the reasons behind reducing the inverter efficiency at low power levels. Here a detailed mathematical analysis of the losses in the SPWM inverter is made. Based on these equations for estimating the various losses in the inverter, efficiency at light load and heavy load while varying the switching frequency from 200Hz up to 20kHz can be calculated.

Typically, two-thirds of the power loss in a hard-switched inverter result from conduction and switching losses in the inverter devices. Conduction losses occur due to the on-state voltage across the device and the current flow through the device while it is conducting current. More precisely, conduction losses occur between the end of the turn-on transition and the beginning of the turn-off transition. A practical model of conduction losses includes the effect of device on-voltage and conduction resistance. Switching losses arise from the transient situation where both device voltage and current are changing as the device turns on or turns off. Evaluation of the conduction and switching losses can be done using simplified device models described in and. However, there are also other losses associated with inverter operation. These include gate driver circuit loss, control circuit loss, and losses due to snubber circuits.

The snubber circuit loss and the control circuit losses have been ignored while developing the overall loss model, given that they contribute to a very minimal amount of loss compared to switching loss and conduction loss.

A-2 CONDUCTION LOSSES

To evaluate the conduction loss through a simplified model appropriate for both power transistors and diodes, the device is simplified as a constant voltage drop in series with a linear resistor. The on-state voltage of a power transistor and a diode can be calculated using a power transistor datasheet. During the time that the power transistor is on, the collector to emitter voltage, v_{ce}, is given by:

$$v_{ce} = V_q + i_q R_q \quad \text{(A1)}$$

The exact approximation can be used for the anti-parallel diode, giving:

$$v_{ak} = V_d + i_d R_d \quad \text{(A2)}$$

Here, the voltage source V_q represents the power transistor on-state zero-current collector-emitter voltage and R_q stands for the collector to emitter on-state resistance. Similarly, V_d denotes on-state zero-instantaneous current forward voltage for the anti-parallel diode and R_d stands for diode on-state resistance. i_q and i_d are the currents flowing through the power transistor and diode respectively. The parameters V_q, R_q, V_d and R_d can be estimated from the component datasheets.

To simplify the calculation of the device average and RMS currents, the load current is assumed to be sinusoidal. Power dissipated in a component with a constant voltage drop is the average current times the voltage drops. The RMS current squared times the resistance signifies the power dissipated in a resistor. The average and RMS currents of the power transistor and diode in an inverter (given sinusoidal pulse width modulation) are:

$$\bar{I}_q = I_o(pk)\left[\frac{1}{2\pi} + \frac{m_a \cos\emptyset}{8}\right] \quad \text{(A3)}$$

$$I_{q(rms)} = I_o(pk)\sqrt{\frac{1}{8} + \frac{m_a \cos\emptyset}{3\pi}} \quad \text{(A4)}$$

$$\bar{I}_d = I_o(pk)\left[\frac{1}{2\pi} - \frac{m_a \cos\emptyset}{8}\right] \quad \text{(A5)}$$

$$I_{d(rms)} = I_o(pk)\sqrt{\frac{1}{8} - \frac{m_a \cos\emptyset}{3\pi}} \quad \text{(A6)}$$

Here, $I_o(pk)$ denotes the peak load current, $\emptyset$ denotes the load power factor angle, m_a the modulation index, $\bar{I}_q$, $\bar{I}_d$ denote the average currents and $I_{q(rms)}$, $I_{d(rms)}$ denote RMS currents flowing through the power transistor and the anti-parallel diode. The conduction losses in the power transistor, P_{q-con} and diode, P_{d-con} are obtained using:

$$P_{q-con} = V_q\bar{I}_q + R_q{I_{q(rms)}}^2 \quad \text{(A7)}$$

$$P_{d-con} = V_d\bar{I}_d - R_d{I_{d(rms)}}^2 \quad \text{(A8)}$$

The total conduction losses, $P_{tot-con}$ of the four power transistors along with their anti-parallel diodes can be calculated from:

$$P_{tot-con} = 4(P_{q-con} + P_{d-con}) \quad \text{(A9)}$$

The total conduction loss associated with the inverter is found easily using equation (A9). Equation (A9) shows that the conduction losses depend on the load conditions.

A-3 SWITCHING LOSSES

In power inverters, switching loss typically contributes significantly to the total system losses. The switching loss in the power transistor depends on the power transistor and diode's dynamic characteristics. Three components of the switching losses in the hard-switching inverter can be identified: power transistor turn-on losses, power transistor turn-off losses, and the losses due to reverse diode recovery. During turn-on, the semiconductor is exposed to a high current peak due to the reverse recovery of the freewheeling diode. At the same time the collector-emitter voltage is still high, thus causing high switching losses. During turn-off, the losses can be even higher due to the long collector current tail. So, the turn-on losses are due to the rate of current change and the stored charge in the free wheel diode. On the other hand, the turn-off losses depend on the speed of the gate drive and the power transistor's current tail due to the recombination of minority carriers. The semiconductor is hard to switch under these conditions of simultaneous high current and high voltage during the switching transient.

Evaluation of the switching losses, in the hard-switching inverter consisting of four 15A, 600V power transistor and ultrafast soft recovery diodes, can be done using the measured values of switching energy from the data sheets. Generally, datasheets provide the values of turn-on and turn-off energy (E_{on} and E_{off}) for a conventional test voltage and current (V_{test} and I_{test}). The calculated values of turn-on energy comprise the losses due to diode reverse recovery and tail current losses. The total energy loss during turns on and turn off transients of the switch, E_{tot}, can be calculated based on using:

$$E_{tot} = K_g\left(E_{on} + E_{off}\right)\frac{V_s}{V_{test}}\frac{I_o(pk)}{I_{test}} \qquad \text{(A10)}$$

Equation (A10) represents V_s as the bus voltage, $I_o(pk)$ as the peak load current and K_g as the correction factor to account for the gate drive impedance. The total switching losses, P_{tot-sw}, of the proposed inverter can found using:

$$P_{tot-sw} = 4f_{sw}\frac{E_{tot}}{\pi} \quad \text{(A11)}$$

Here, f_{sw} denotes the SPWM switching frequency. Evidently, the switching losses in the hard-switching inverter are directly proportional to the switching frequency. Further, from equation (A11) the switching energy is proportional to the voltage across the device during switching, so the losses can be eliminated if the voltage across the device is zero. This kind of switching technique is called soft-switching or zero voltage switching but the added components will result in cost and reliability penalties.

A-4 GATE DRIVE LOSSES

power transistors are voltage-controlled devices and require a gate voltage to establish conduction between collector and emitter. The total gate driver power loss can be derived from the summation of the total power dissipated for the emitter ($P_{emitter}$), internal circuitry ($P_{emitter}$) and the output (P_{output}) of the power transistor driver IC:

$$P_{gate-driver(tot)} = P_{output} + P_{emitter} + P_{internal} \quad \text{(A12)}$$

power transistor total gate capacitance, C_{gate}, is the total gate charge Q_{gate} divided by the gate drive supply voltage V_{GE}:

$$C_{gate} = \frac{Q_{gate}}{V_{GE}} \quad \text{(A13)}$$

This means that the charging and discharging of the power transistor gate is equivalent to the charging and discharging a capacitor. Hence the power dissipated for the output of the power transistor driver IC can be defined by:

$$P_{output} = C_{gate} {V_{GE}}^2 f_{sw} \quad \text{(A14)}$$

Where, f_{sw} is the switching frequency. The power dissipated in the power transistor driver emitter can be derived from the diode forward current $I_{F,}$ maximum diode duty cycle D and diode forward voltage V_F:

$$P_{emitter} = I_F V_F D \quad \text{(A15)}$$

Finally, the power dissipated in the power transistor driver internal circuitry depends on I_{CC}, the collector current, and the collector to emitter voltage $(V_{CC} - V_{EE})$. Note the collector to emitter voltage can be any value between a minimum of -0.5V and a maximum of the device's peak forward rating:

$$P_{internal} = I_{CC}(V_{CC} - V_{EE}) \quad \text{(A16)}$$