UNIVERSITY OF CALGARY

Static Synchronous Parallel Compensation of Var Flow in Power Distribution Systems

By

ZHIQIANG LIU

A THESIS

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ABSTRACT

Excessive var flow can cause extra energy loss and/or significant voltage drop, and is a matter of concern for power system operators and engineers. Var flow control in transmission and distribution systems can be of immense benefit to electric power utilities in regard to performance. Static power electronic controllers are now making a major impact on var compensation in power systems through applications in transmission, distribution and small generation.

Discussed in this dissertation is use of a solid-state device, Insulated Gate Bipolar Transistor – IGBT, to build a current regulated inverter. This inverter is used in developing, what is referred here as a Static State Parallel Compensator, SSPC, for use in power distribution systems and other applications.

There are four important features of this dissertation: (a) A Static Synchronous Parallel compensator that employs a current regulated inverter to inject a current orthogonal to the associated phase voltage is presented. This results in reducing the current from the source power supply. (b) The current regulated inverter is built using a high switching frequency power device: IGBT. (c) The SSPC eliminates the large capacitors and inductors that are necessary for traditional static compensators. (d) Hysteresis-type control is used to regulate the inverter output, which eliminates the need for a large filter inductor. Therefore, the size and cost of the SSPC are smaller than that of a realization employing GTO devices operating at a lower switching frequency.

The SSPC has been simulated and the results are presented in this dissertation. It can be concluded from the results that the magnitude and phase angle of a compensation current can be dynamically adjusted according to load change and technical requirements. The total harmonic distortion of the compensation current is less than 5%, thus meeting industrial requirements.

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LIST OF SYMBOLS AND NOMENCLATURE

BJT	Bipolar junction transistor
BRT	Base resistance thyristor
CSTBT	Carrier stored trench-gate bipolar transistor
DFT	Discrete Fourier transform
EST	Emitter switched thyristor
F_-	Negative sequence network Fourier transform
F_+	Positive sequence network Fourier transform
F_0	Zero sequence network Fourier transform
FACTS	Flexible ac transmission system
FCT	Field controlled thyristor
GTO	Gate turn-off thyristor
i_c	Compensation current in continuous time
$i_c(n)$	Compensation current in discrete-time
i_e	Current error
IEGT	Injection enhanced gate transistor
i_f	Feedback current
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate commutated thyristor
i_l	Load current
i_{ref}	Reference current
MBGT	MOS and bipolar gate thyristor
MOSFET	Metal-oxygen-semiconductor field effect transistor
MTO	MOSFET controlled thyristor
P	Real power
PWM	Pulse width modulation
q_B	Compensation coefficient
Q	Reactive power

Q_{com}	Reactive power for compensation
SCR	Silicon controlled rectifier
SIT	Static induction transistor
SSPC	Static synchronous parallel compensator
SSSC	Static synchronous series compensator
STATCOM	Advanced static var compensator
SVC	Static var compensator
T	Non-zero positive integer corresponding to the sample period;
TCR	Thyristor controlled reactor
TCSC	Thyristor controlled series compensator
THD	Total harmonic distortion
T_S	Sample period
TSC	Thyristor switched capacitor
UPFC	Unified power flow controller
var	Volt-amp reactive
v_c	Control voltage
v_l	Load voltage
v_t	Triangular carrier voltage
$\overline{V}_r$	Per unit receiving end voltage
$\overline{V}_s$	Per unit sending end voltage
X_{el}	Effective reactance
X_q	Compensating reactance
ΔP	Power loss
δr	Phase angle of receiving end voltage source
δs	Phase angle of sending end voltage source
φ	Phase angle from zero crossing of a waveform
μ	Power factor demand factor
ψ_l	Phase angle difference of load current and associated phase voltage

CHAPTER 1
INTRODUCTION

1.1 Reactive Volt-Amp Compensation

Most commercial and industrial loads are inductive in nature and thus current lags the associated voltage. Therefore, the volt-amps drawn from the utility are larger than the real power in watts. Only the component of the current that is in phase with the associated voltage provides useful work. The out of phase component increases the total current that the utility must supply. So a premium may be charged to a customer with a power factor that is below a value fixed by the electric utility (usually 0.7). Utilities actually charge their large customers for the kVA and kW hours using a two part tariff as compensation for having low power factor. Thus customers have an economic interest in improving the power factor of their facilities. The trend has been to improve the power factor to between 0.9 and 0.95 or even better as the cost of electricity has risen in recent years.

The overall power factor of a customer's internal electrical system is brought closer to unity by adding capacitance across the line at various points in the customer's internal electrical distribution system. If the system is compact the capacitance may be near the service points. Larger systems may require power factor correction for each major bus. In the event that the system is capacitive (a rare occurrence), inductance would be added across the line for power factor correction [1].

Automatic equipment is available to sense the power factor of a system and switch more or less capacitance across the line as the load changes in nature. The automatic systems must be chosen with care because many will try to over correct the power factor when a significant part of the load is solid-state motor drives, possibly causing the system voltage to go to excessive levels [1]

In the past, the power factor might not have been corrected to unity for one of two main reasons. The cost of correcting the power factor to unity as opposed to a more modest

correction between 0.90 and 0.95 may be much higher, and the return on investment for the optimal correction may be too small to justify. For example, consider a 10 MW load at 0.8 power factor ($\cos\varphi_1$) lag. To correct power factor of this load to unity ($\cos\varphi = 1.0$), the reactive power for compensation, Q_{com}, *is*

$$Q_{com} = P(\tan\varphi_1 - \tan\varphi) = P \times q_B \qquad (1\text{-}1)$$

where

P is real power,

φ_1 is phase angle difference between voltage and current before compensation,

φ is phase angle difference between voltage and current after compensation,

q_B is compensation coefficient.

In this case $q_B = 0.75$ (corresponding to $\cos\varphi = 1$), thus

$$Q_{com} = P(\tan\varphi_1 - \tan\varphi) = P \times q_B = 7.5\ Mvar$$

for a 60 Hz, 4kV system, the associated capacitor C = 1244 μF, which is very large [2].

The second reason is that a correction to a unity power factor under one set of operating conditions may result in a leading power factor under different load conditions. A leading power factor could result in an excessive line voltage increase in many systems. To operate well at unity power factor, such systems will need automated equipment to control the volt-amp reactive, var, [3] compensation as the load changes [1].

The power factor correction is accomplished using var compensators. Therefore, var compensation will be discussed in this dissertation, instead of power factor correction.

Historically, var compensators have been developed in three phases:

- Staged capacitor compensation.
- Dynamically controlled compensator, e.g., Thyristor Controlled Series Compensator, TCSC [4][5], Static Var Compensator, SVC [5][6][7], Unified Power Flow Controller, UPFC [8] [9], Advanced Static Var Compensator, STATCOM [10][11].
- Solid-state device compensators, e.g., Static Synchronous Series Compensator, SSSC [12][13].

TCSC and SVC are popularly used in today's power systems. However, there is a tendency for the SSSC to take the place of TCSC in the future, because of its smaller size, low cost, quick response and reduced maintenance [14].

The var compensation devices mentioned above fall in the categories of parallel and series connection. A brief description of SVC, TCSC and SSSC and their relative merits is given below.

1.2 Static Var Compensator

Figure 1.1 shows the typical method of static var compensation. The leading reactive current necessary for var compensation is actually supplied by connecting capacitor banks across the ac lines. Before the development of thyristors, this was done using electromechanical circuit breakers. With the advent of thyristors, bidirectional ac switches using thyristors were developed for connecting and disconnecting the capacitor banks. A capacitor bank connected in this way is called a Thyristor Switched Capacitor (TSC). The problem to be faced when connecting the capacitor to the high voltage lines is the large inrush current that will flow at the moment of contact if there is a large instantaneous voltage differential between the line and the capacitor [15].

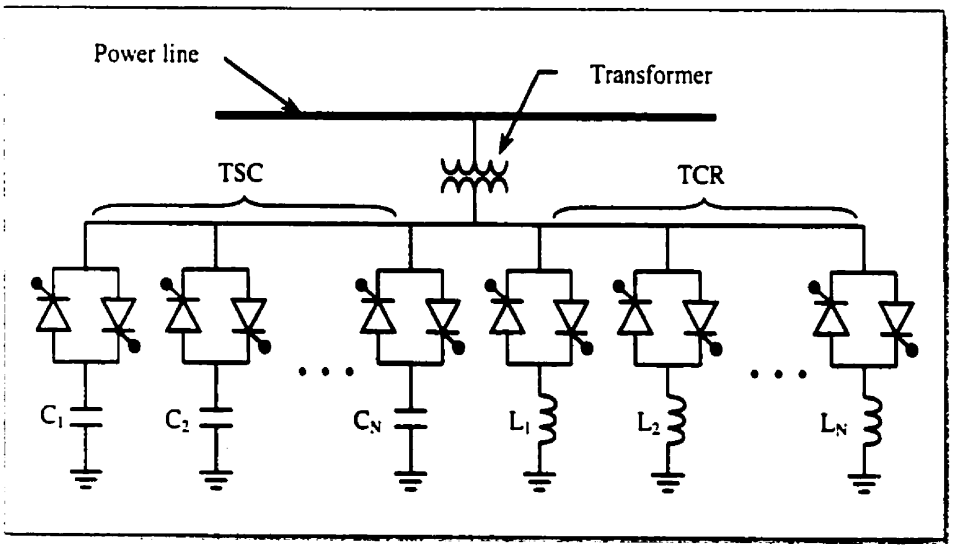


Figure 1.1. Static var compensation scheme using TSC and TCR

It is relatively easy to overcome this difficulty, because the TSC uses static thyristor switches. The switches can be gated at any desired instant in an ac cycle by means of a switching controller that senses the voltage differential and gates the thyristor at the correct instant in the ac cycle when the voltage differential is within permissible limits.

If only TSCs are employed for var compensation, the leading vars to be introduced can only be adjusted in steps, because only discrete capacitors can be switched at a time. For precise adjustments of vars, as dictated by the system requirements, a continually variable feature is desirable. This is achieved as illustrated in the scheme in Fig. 1.1 by having a Thyristor Controlled Reactor (TCR) in parallel with the capacitor bank. If the lagging reactive vars corresponding to the maximum current drawn by the TCR are equal to the leading vars of the capacitor, the two will cancel and the net vars will be zero. From this point, the lagging vars of the TCR can be progressively decreased by phase control, thereby increasing the net leading vars. After reaching the maximum, further increase can be made by switching in another capacitor bank. In this manner, the TSCs provide vars in steps, while the TCR provides the continuous adjustment between steps. This scheme, called the Static Var Compensator, enables precise and fast automatic adjustment of the vars by means of closed loop control. Also, in a practical high voltage system the TSCs and TCRs may be connected to the secondary side of a transformer. In this way, the maximum voltage requirements of the thyristors and the capacitors can be lowered [15].

An SVC is an improvement over the original power factor controller and is popularly used in power systems because it can regulate the power factor dynamically rather than statically, which makes full use of the controller and improves the operation of the power system [15].

1.3 Thyristor Controlled Series Compensator

To demonstrate the operating principle of the TCSC, a practical installation is used as an example. A TCSC controller has been installed at BPA's C.J.Slatt substation on the Slatt-Buckley 500 kV line in Northern Oregon. Figure 1.2 shows an elementary one-line

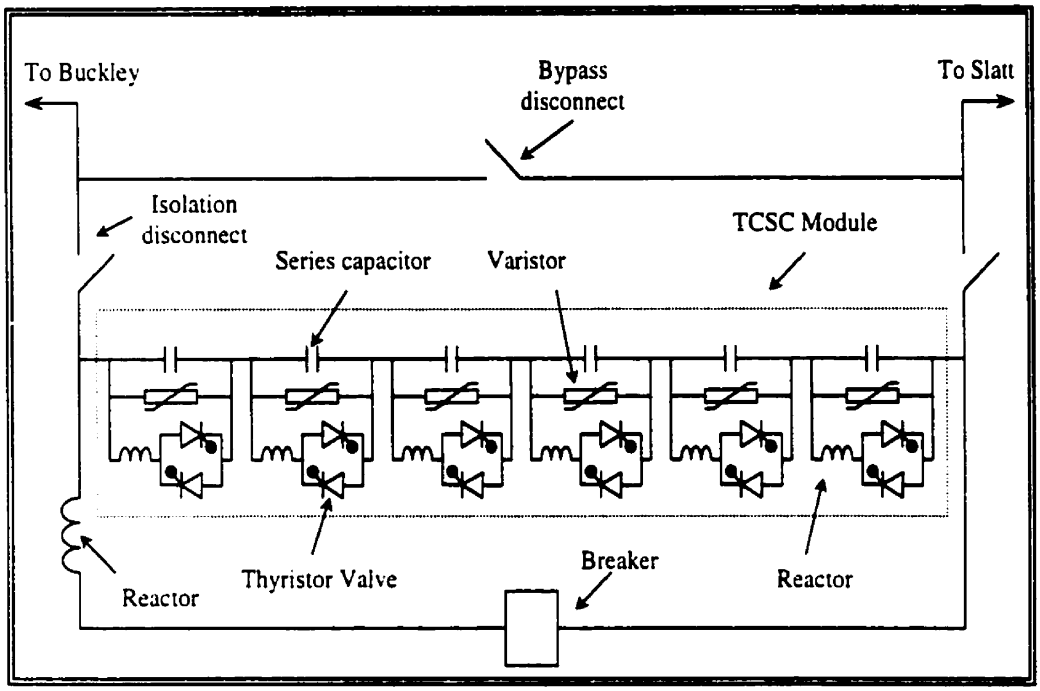


Figure 1.2. One-line diagram of thyristor controled series compensator

diagram of the Slatt-TCSC [16]. It is comprised of six identical TCSC modules connected in series. Each module consists of a capacitor, a bi-directional thyristor valve (with its associated reactor), and a varistor. A bypass breaker (with its associated reactor) is connected across the entire device for use in operational and protective functions. Also, three disconnect switches are used to bypass and isolate the TCSC from the Slatt-Buckley transmission line [16].

Each module can operate either bypassed or inserted. In addition, when the capacitor is inserted, the thyristor valve can be phase-controlled to vary the effective fundamental-frequency impedance of the capacitor. The basic operating principles are explained below.

While the capacitor is bypassed, the thyristors are gated for full conduction, and the net reactance of the module is slightly inductive because of the reactor in series with the thyristor valve. This is illustrated in Fig. 1.3. Note that some current also flows

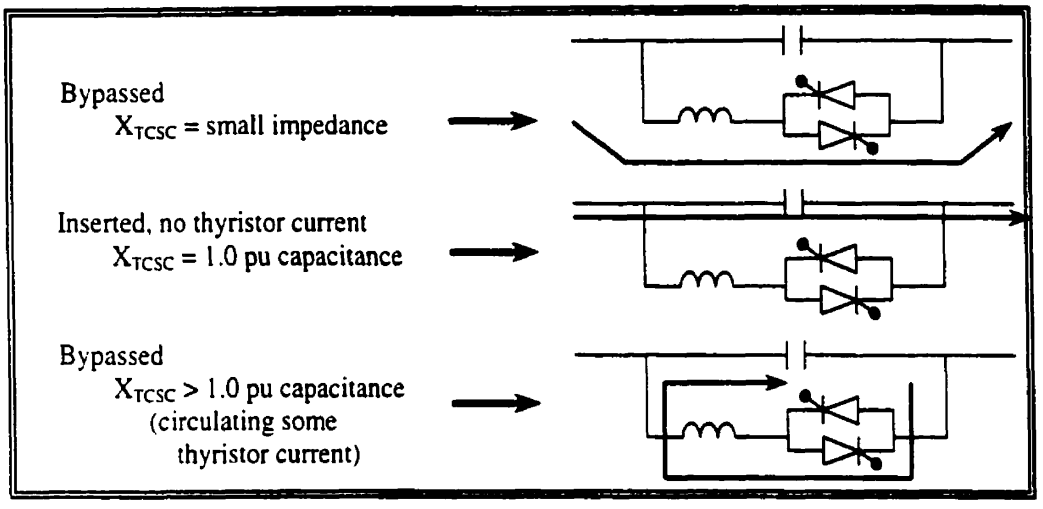


Figure 1.3 Sell out control model sequence of operation

through the capacitor during bypassed operation, but most flows through the thyristor valve and reactor because it is a much lower impedance path.

If the capacitor is inserted by turning off the thyristor valve (that is, blocking all gating signals to the thyristors), the effective capacitance of the module is the same as its ominal value. This mode of operation is essentially the same as for a conventional series capacitor.

While the capacitor is inserted, the thyristors can be gated near the end of each half cycle in a manner that can circulate controlled amount of inductive current through the capacitor, thereby increasing the effective capacitive reactance of the module. This concept referred to as vernier control is also illustrated in Fig. 1.3. In this mode, the inserted reactance can be controlled in a continuously-variable (vernier) manner from a minimum value of the capacitor alone (1.33 ohms) to as much as 4.0 ohms. The upper limit for vernier operation is a function of line current magnitude and time spent at the operating point.

The Slatt TCSC consists of six modules. The operation of all six modules is automatically coordinated from a higher level control system called the common control. All modules receive "ohms" orders from the common level, and these orders establish the operating mode and vernier level for each individual module. The structure of the

transmission networks of power systems leads to several operational challenges which may be helped by appropriate forms of series compensation technology [16].

The characteristics of a TCSC are:

- Hardware design is geared to the maximum voltage that is to be handled.
- Mvar rating of the capacitor bank is proportional to the product of the maximum voltage and the corresponding maximum current.
- Advanced control is required.
- There is an unrestricted number of operations and sequences.
- Accurate setting of the compensation degree is possible.

1.4 Static Synchronous Series Compensator

Electric power flow through an ac transmission line is a function of the line impedance, the magnitudes of the sending-end and receiving-end voltages, and the phase angle between these voltages. By inserting an additional inductive reactance in series with the transmission line and thereby increasing the effective reactance of the transmission line between its two ends, the power flow can be decreased. Also, the power flow can be increased by inserting an additional capacitive reactance in series with the transmission line, thereby decreasing the effective reactance of the transmission line between its two ends [13].

Traditionally, in order to control the power flow of the transmission line, the effective line reactance is controlled using fixed or thyristor-controlled series capacitors or inductors. In 1996, a new var compensator, Static Synchronous Series Compensator (SSSC), was proposed [13]. It is a solid-state voltage source inverter that injects an almost sinusoidal voltage, of variable magnitude, in series with a transmission line. This injected voltage is almost in quadrature with the line current. A small part of the injected voltage, which is in phase with the line current, provides the losses in the inverter. Most of the injected voltage, which is in quadrature with the line current, emulates an inductive or a capacitive reactance in series with the transmission line. This emulated variable reactance, inserted by the injected voltage source, influences the electric power flow in the transmission line [13].

When an SSSC injects an alternating voltage leading the line current, it emulates an inductive reactance in series with the transmission line, which results in the line current decrease as the level of compensation increases. At this point, the SSSC is considered to be operating in an inductive mode. When an SSSC injects an alternating voltage lagging the line current, it emulates a capacitive reactance in series with the transmission line, which results in the line current increase as the level of compensation increases. At this point, the SSSC is considered to be operating in a capacitive mode.

Figure 1.4 shows a single line diagram of a simple transmission line with an inductive reactance, X_L, connecting a sending-end voltage source, $\overline{V}_s$, and a receiving-end voltage source, $\overline{V}_r$, respectively. The real and reactive power (P and Q) flow at the receiving-end voltage source are given by the expressions

$$P = \frac{V_s \cdot V_r}{X_L}\sin(\delta_s - \delta_r) = \frac{V^2}{X_L}\sin\delta \qquad (1\text{-}2)$$

$$Q = \frac{V_s \cdot V_r}{X_L}(1-\cos(\delta_s - \delta_r)) = \frac{V^2}{X_L}(1-\cos\delta) \qquad (1\text{-}3)$$

where V_s and V_r are the magnitudes, δ_s and δ_r are the phase angles of the voltage sources $\overline{V}_s$ and $\overline{V}_r$, respectively. For simplicity, the voltage magnitudes are chosen such that $V_s = V_r = V$ and the difference between the phase angles is $\delta = \delta_s - \delta_r$.

An SSSC, limited by its voltage and current ratings, is capable of emulating a compensating reactance, X_q, (both inductive and capacitive) in series with the transmission line inductive reactance. Therefore, the expressions for power flow are given by the equations:

$$P_q = \frac{V^2}{X_{eff}}\sin\delta = \frac{V^2}{X_L(1-X_q/X_L)}\sin\delta \qquad (1\text{-}4)$$

$$Q_q = \frac{V^2}{X_{eff}}(1-\cos\delta) = \frac{V^2}{X_L(1-X_q/X_L)}(1-\cos\delta) \qquad (1\text{-}5)$$

An example of a simple power transmission system with an SSSC operated both in inductive and in capacitive modes and the related phasor diagrams are shown in Fig. 1.5. The line current decreases from $\bar{I}_{-0\%}$ to $\bar{I}_{-100\%}$, when the inductive reactance compensa-

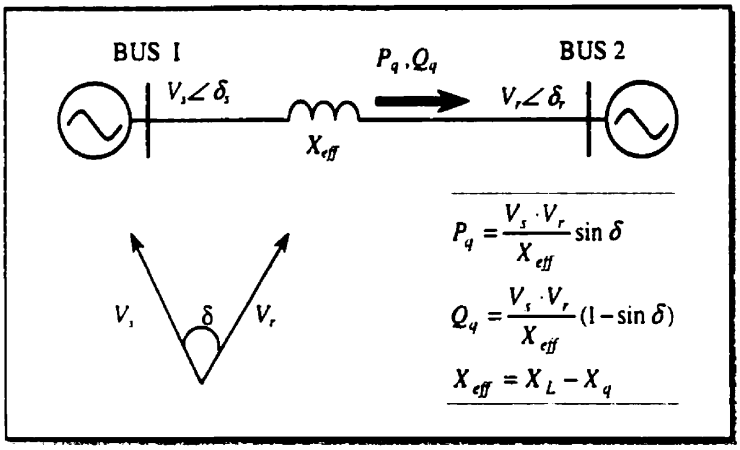


Figure 1.4. Elementary power transmission system

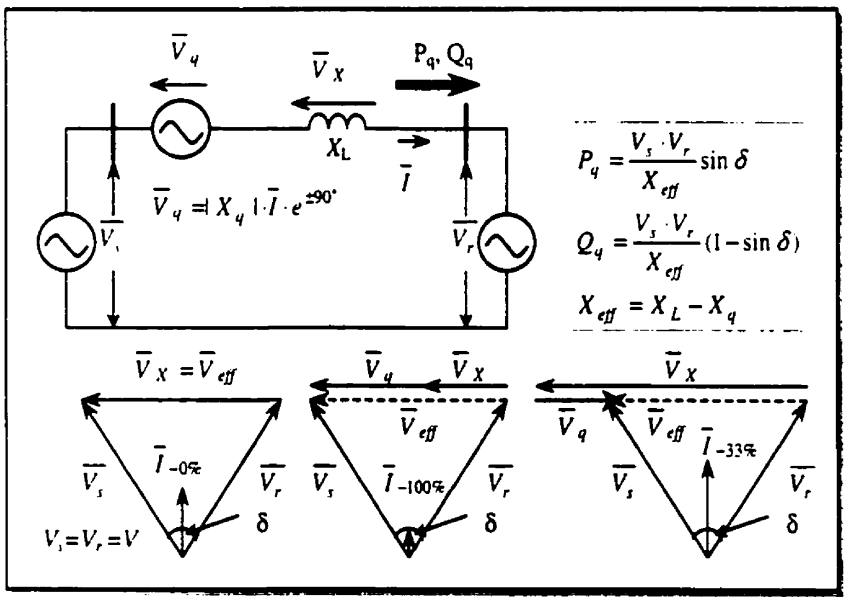


Figure 1.5. Static synchronous series compensator operated in inductive and capacitive modes and the related phasor diagrams

tion. $-X_q / X_L$, increases from 0% to 100%. The line current increases from $\bar{I}_{-0\%}$ to $\bar{I}_{-33\%}$, when the capacitive reactance compensation, X_q / X_L, increases from 0% to 33%.

The expressions for the normalised power flow in the transmission line and the normalized effective reactance, X_{eff}, of the transmission line can be written as:

$$\frac{P_q}{P} = \frac{Q_q}{Q} = \frac{1}{1 - X_q / X_L} \qquad (1\text{-}6)$$

$$\frac{X_{eff}}{X_L} = 1 - \frac{X_q}{X_L} \qquad (1\text{-}7)$$

The effect of X_q on the normalized power flow in the transmission line is shown in Fig. 1.6. When the emulated reactance is inductive, the power flow, P_q, and Q_q, decreases and X_{eff} as $-X_q/X_L$ increases. When the emulated reactance is capacitive, P_q and Q_q increase and X_{eff} decreases as X_q/X_L increases [13].

1.5 Comparative Analysis

SSSC is an advanced approach in var compensation, which has comparatively quick response, smaller size and low cost. It is likely to play an important role in power systems with long transmission lines. The fundamental principle of its application being line reactance, it is not applicable in distribution systems with short lines.

SVC is a good var compensator, which can be employed in either high voltage power systems or distribution systems. Therefore, it is beneficial to the electric companies. It works in union with other Flexible AC Transmission System (FACTS) [17] [18] devices to keep the system operating in stable condition. However, because it is connected to a system in parallel, its compensation property is not as good as that of SSSC, when the line voltage drop is large enough to affect the normal operation. In this case, SVC is not applicable. On the other hand, SVC consists of solid-state devices for regulation and inductors and capacitors for compensation, which results in slower response, larger size and higher cost.

TCSC has the same drawbacks as SVC, that is, it consists of solid-state devices for regulation and inductors and capacitors for compensation, which makes TCSC have slower response, larger size and higher cost.

From the analysis above, these three var flow controllers can not solve the problem in power distribution systems adequately. Therefore, it is necessary to seek a better

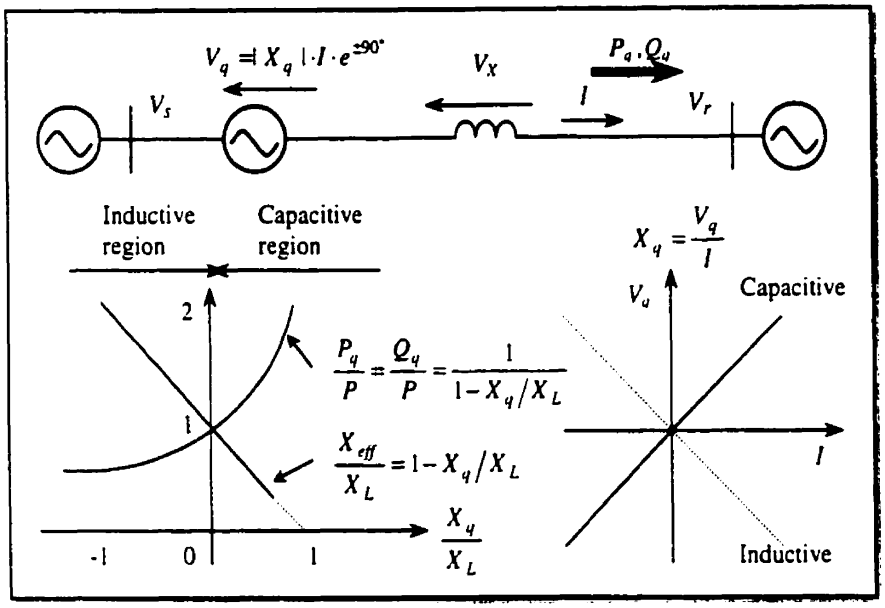


Figure 1.6. Effect of compensating reactance on power flow and effective reactance

approach. Presented in this dissertation is the proposed static synchronous parallel compensator (SSPC) using a current regulated inverter to inject a current orthogonal to the associated phase voltage. The inverter is designed using a high switching frequency power device, the Insulated Gate Bipolar Transistor (IGBT).

1.6 Dissertation Objectives

The objective of this dissertation is to make a contribution to the development of var compensation in distribution systems. For that purpose, the design of the SSPC is studied in this dissertation. The elements to achieve this objective are given below.

Analyse the existing technologies for var compensation, pointing out their advantages and disadvantages along with the respective application domains.

Design and model the proposed static synchronous parallel compenstor, which includes converter design, inverter design and controller design. The converter is used to provide stable, controllable dc power, while the inverter has the ability to inject controllable ac currents to compensate vars in the distribution systems. The function of the inverter is

realised by the controller through the control of the firing signal of the IGBTs so as to control the inverter output according to load change and specification requirement.

To test if the design is reasonable and realisable, simulation studies are performed first. The simulation is divided into three parts. Simulation for a single-phase system compensation is used to verify the feasibility of the proposed approach. Design modifications, if any required, are made at this stage. Simulation for a three-phase system compensation is then used to demonstrate the functions of the SSPC, and test for the correctness of the proposal. Finally, simulation of dynamic compensation presents the system performance.

1.7 Contributions of Dissertation

The main contributions can be summarized as follows:

A new approach, SSPC, for var compensation is presented. The SSPC can provide compensation current with variable magnitude and phase angle according to load change and requirements. This new approach can replace SVC for var compensation in distribution systems, because:

- it deletes the capacitors and inductors for compensation in SVC,
- it possesses flexible compensation ability, and
- it can compensate the power factor to unity without additional devices.

The inverter design deviates from the traditional route. Generally, the voltage source inverter can be used to provide variable ac voltages, and current source can be used to provide variable ac current. In this design, the voltage source inverter is employed and the output is a variable ac current rather than ac voltage. This results in the deletion of a big inductor as a ripple filter.

A high switching frequency power device is used in the design. Compared with Gate Turn-Off Thyristor (GTO) and Integrated Gate Commutated Thyristor (IGCT), the IGBT has remarkable advantages. For example, it can be operated at high frequency. Therefore, it reduces the size of the SSPC, and increases the efficiency of the SSPC.

A good control strategy, hysteresis-type control, is employed in the controller design, which can take full use of the advantage of the IGBT, reduce total harmonics, and total harmonic distortion (THD) in the compensation currents.

1.8 Dissertation Outline

This dissertation consists of 5 chapters. Presented in Chapter 1 is a background of var compensation. Discussed in Chapter 2 is the SSPC component design. Based on the design in Chapter 2, introduced in Chapter 3 is the SSPC system design and the simulation results are given in Chapter 4. Given in Chapter 5 is the conclusions for the design and simulation investigation and future studies.

Compared in Chapter 2 is a set of solid-state devices, from which the IGBT is selected to build the inverter. The inverter has smaller size and higher efficiency than that composed of GTO.

As a dc link of an inverter, a converter must be stable, and its magnitude must be changeable according to load variation, which is discussed in Chapter 2.

The inverter is the most important part in the SSPC. The inverter design is discussed in detail in Chapter 2. The reason why the inverter design is emphasized in this dissertation is its special characteristics and its important role in compensation. Traditionally, voltage source inverter is used to supply variable ac voltages, while current source inverter is employed for outputting variable ac currents. However, a current regulated inverter is required to deliver variable ac currents in an SSPC. Therefore, a unique design procedure has to be developed.

The specially designed inverter needs a special control strategy. Therefore, the associated controller has to be designed, which is also discussed in Chapter 2. The first consideration is to reduce the total harmonic distortion of current, and the second consideration is to output variable current. These requirements can be realised using hysteresis-type control.

The procedure of the SSPC design is quite complicated, because there is no existing rule to follow in this case. After extensive trials and analysis, proper parameters for each device in the system were selected and desired simulation results were obtained for single-phase compensation. Results of these studies are given in Chapter 3.

Although confidence was gained after the simulation for single-phase compensation, new problems appeared with the three-phase case. For example, compensation currents and phase voltages were seriously distorted. Presented in Chapter 3 is the solution for solving these problems and describes the simulation results for three-phase compensation in static condition.

To implement the design for industrial applications, every possible condition must be considered. e.g., balanced or unbalanced system operation, load change from inductive situation to capacitive situation or vice versa. All these simulation results are presented in Chapter 4.

Conclusions for the SSPC design and simulation studies and future studies are given in Chapter 5.

CHAPTER 2

SSPC COMPONENT DESIGN

The function of the static synchronous parallel compensator is to inject a current that is in quadrature with the associated voltage, i.e., the SSPC only delivers reactive power to the load according to the actual load power factor and the desired overall power factor.

A block diagram of the SSPC is shown in Fig. 2.1, where

v_l – load voltage

i_l - load current

i_c – compensation current

It is composed of an inverter, associated filter components, controller and a dc source. The dc source can be a battery or an ac/dc converter. This chapter presents the design of these components and the choice of control strategy.

2.1 Converter Design

In the SSPC design, a dc source is needed to provide power for the inverter. The dc source can be either a battery or an ac/dc converter. The converter design is discussed in this section.

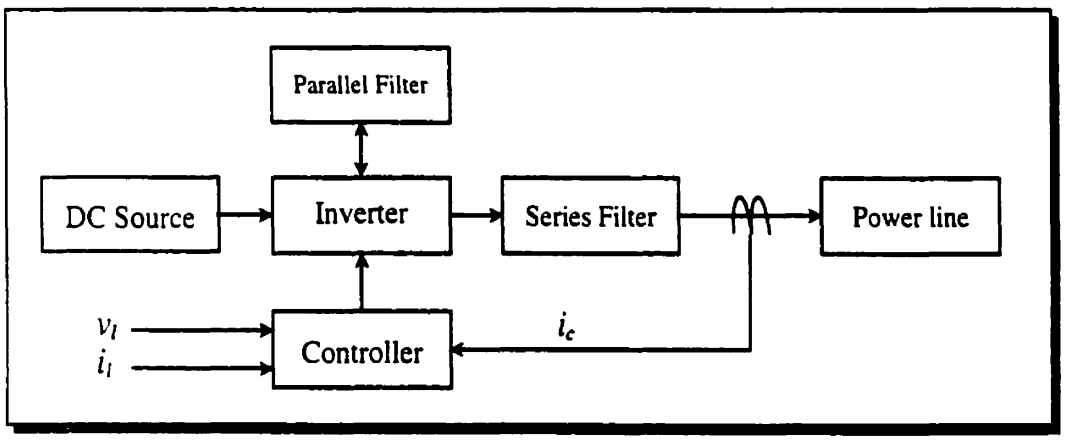


Figure 2.1. Schematic diagram of the SSPC

2.1.1 Thyristor and its connection

The thyristor, also known as the silicon controlled rectifier (SCR), was the first solid-state power semiconductor device to be developed to function as a controlled static switch with large current and voltage capability. It was the advent of the thyristor that began a new era of major developments in static power conversion and control. These developments have made rapid strides in recent years, making "Power Electronics" a recognized technology in its own right. The thyristor has two categories of voltage ratings – the forward blocking and the reverse blocking. These ratings are generally equal.

Current ratings are generally valid only if cooling is provided by the use of suitable heat sinks to keep the device temperature within the specified limit. Average, rms, repetitive peak as well as surge current ratings are usually specified separately, especially for devices with large ratings. Power semiconductor category fuses may be used with each individual thyristor in a converter to provide short-circuit protection to it. The main parameter on the basis of which the fuse is selected is the I^2t rating. To afford protection, the I^2t rating of the fuse must be less than the I^2t rating of the thyristor. Its continuous current rating should match that of the thyristor. The voltage rating of the selected fuse will be based upon the maximum circuit voltage that can occur across it in the event of a fuse blow out [15].

Other major specifications of the thyristor from the power circuit side, which are directly related to its safety, are the *dv/dt* and the *di/dt* ratings. These are expressed in terms of $V/\mu s$ and $A/\mu s$, respectively. A *dv/dt* failure causes an erratic turn ON of the device, and, depending on the circuit conditions, this may result in a short circuit in the system, with the possibility of damage to the device and other components. Exceeding the *di/dt* limit can directly damage the device because of excessive local current concentration in an area of the thyristor pellet [15].

A snubber circuit is invariably used to protect a thyristor from excessive stresses. Fig. 2.2(a) shows the commonly used R-C snubber, where T represents the thyristor. This snubber circuit functions by limiting the over-voltage resulting from the reverse recovery

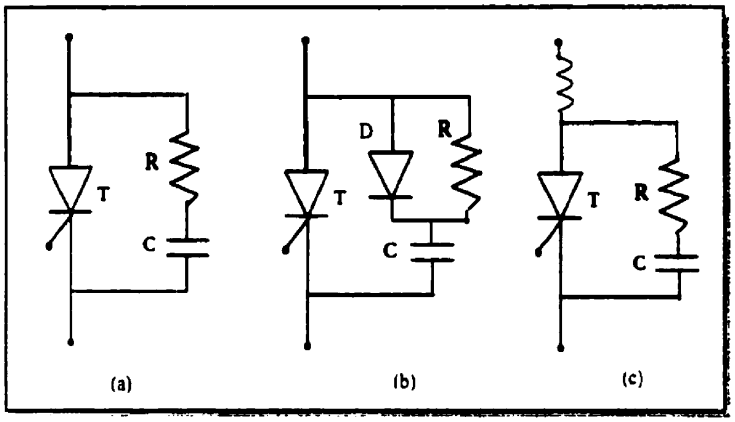


Figure 2.2. Snubber circuit for thyristors

current transient. Also, by suitable choice of values for R and C, it can serve to mitigate the *dv/dt* stress. But the snubber can be made more effective in limiting *dv/dt* by the addition of a diode as shown in Fig. 2.2 (b).

To limit *di/dt*, when circuit conditions are such that there is a danger of exceeding the specification, an inductance may be added as shown in Fig. 2.2(c). This is usually a coil of a few turns, capable of carrying the full thyristor current. In some designs, this coil is wound on a small ferrite ring. This reduces the size of the coil for the same inductance value. Also, the core becomes saturated when the current exceeds its saturating level, and then the effective inductance falls to a low value [15].

2.1.2 Bridge configuration

In the converter design, a popularly used bridge configuration is employed, and a transformer is used with it for the following purposes: (a) to provide electrical isolation between the ac bus and the load circuit. (b) to provide a voltage transformation because the available ac bus voltage is unsuitable to meet the voltage requirement of the load.

Fig. 2.3 shows the bridge configuration for three-phase converters, in which there are two circuit sections. Half of the total number of switching elements constitutes the common cathode section, which is the top in raid in Fig. 2.3. The cathodes of all these elements are tied together at the common cathode terminal labelled K. The common anode section is shown at the bottom raid, where all the anodes are tied together at the common anode

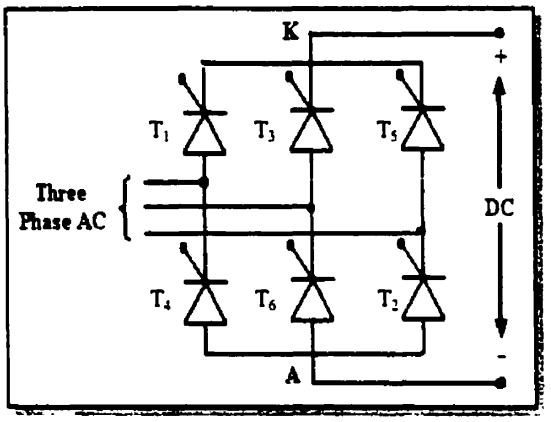


Figure 2.3. Bridge configuration

terminal labelled A. Each "leg" of the bridge, shown vertically, has one device belonging to the common anode section at the bottom and another device belonging to the common cathode section at the top. A bridge will have as many legs as there are ac input lines, each of which is connected to a leg. Bridges with more phases can be built by adding additional legs.

The dc terminals of the bridge are K and A. The common cathode K is the positive voltage terminal in the rectification mode and the negative in the inversion mode. It is always the positive current terminal when the positive current direction is defined as away from the terminal into the external circuit [15].

2.1.3 Gate pulse requirements for the starting of the bridge

The sequence of switching for the three-phase bridge should meet the need that the six thyristors are to be turned ON, one at a time, at 60° intervals. If narrow gate pulses are used for this purpose, the timing of the pulses is as shown in Fig. 2.4 will meet this requirment. In this figure, the top row (a) shows the pulses for the common cathode section according to the labels for the thyristors in Fig. 2.4. The next row (b) shows the pulses for the common anode section. Such a scheme space of pulses, however, will not be sufficient for starting the bridge. The starting difficulty arises because two thyristors, one in the common cathode and the other in the common anode section, must conduct for the dc current to flow. In the gating pulse scheme shown by (a) and (b), only one thyristor

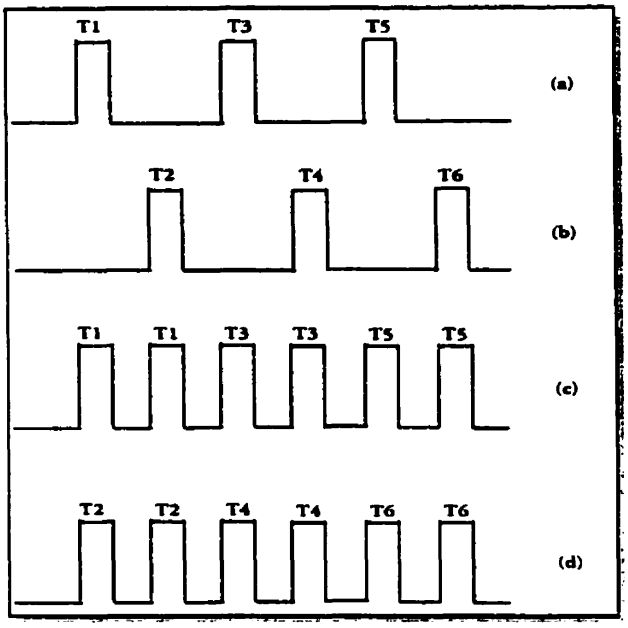


Figure 2.4. Double-pulse gating scheme for three-phase bridges

receives the gating pulse at a time. Therefore, when the first gate pulse arrives at a thyristor, it cannot turn ON, because its partner in the other section has not yet received its gate pulse. When later, after 60°, the partner does receive the gate pulse, its own pulse has disappeared, assuming that the pulse width is less than 60° [15].

There are two solutions to the starting problem. One is to use pulses of long duration, so that a pulse on a thyristor gate does not end before the next pulse arrives on the gate of the thyristor in the other section. The second method is to provide double pulses to each thyristor. The idea is to simultaneously provide a pulse to the conducting partner in the opposite section whenever a pulse is given to any thyristor. This purpose is satisfied by the scheme of pulse sequences shown in Fig. 2.4(c) and (d). Figure 2.4 (c) is for common cathode thyristors and (d) for common anode ones. Every thyristor will be seen to receive two consecutive pulses, the second one timed at 60° from the first. A continuous gating scheme in which each thyristor receives gate drive for the entire duration of its allocated conducting interval will also overcome the starting difficulty. A discontinuous mode of operation can also occur in a bridge. Under such a condition, this type of continuous gate drive is not desirable, because it will also enable each thyristor to come ON as dictated by the circuit conditions after an interruption of current [15].

The double pulse method is the better choice for gate firing according to the above analysis. Therefore, it has been chosen for the converter design.

2.2 Solid-state Device Selection for SSPC Implementation

The main solid-state devices available in the market can be divided into two groups, as shown in Table 2.1. Figure 2.5 shows a direct comparison of the peak blocking voltage and rms current rating between solid-state devices listed in Table 2.1 [19].

In view of the limited potential of MOSFET, BJT and MCT power devices, the only viable power switches for high frequency inverters are those with high blocking voltages and turn-off current capability (namely IGBTs and IGCTs). SCRs are ruled out on the basis of a complex commutation circuit, and high switching losses. The conventional GTO is ruled out on the basis of complex gate circuit and limited switching performance, plus the need for large turn-on and turn-off snubbers. Two GTO type devices (namely IGCT and MTO) and one transistor type (IGBT) are selected as suitable for medium voltage application [19]. However, only the IGBT and the IGCT are discussed here.

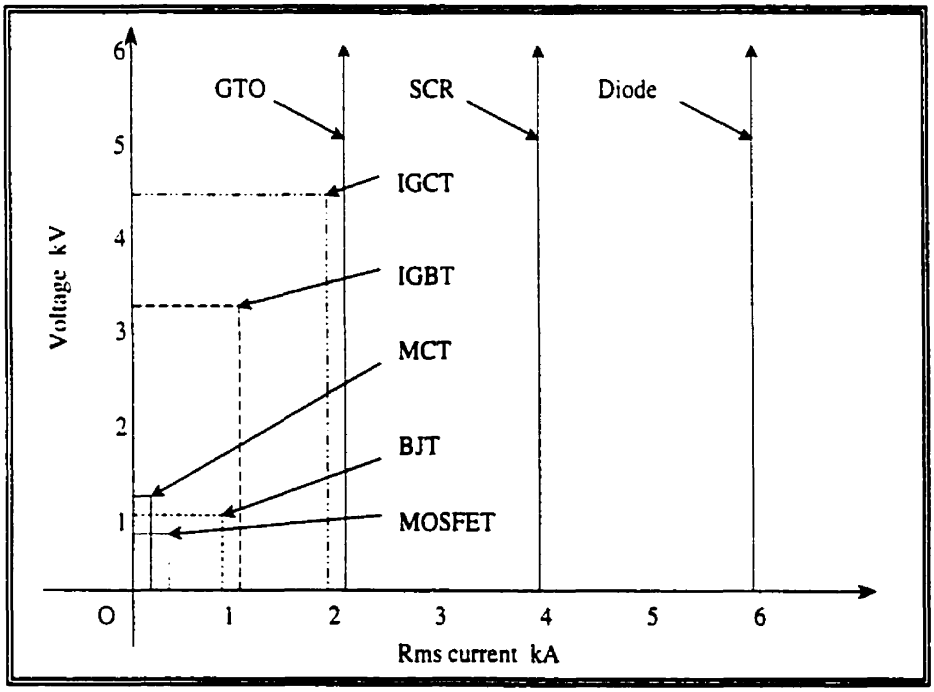


Figure 2.5. Power semiconductor rating comparison

Table 2.1 Self-commutated solid-state devices

GROUP 1: THYRISTORS	GROUP 2: TRANSISTORS
Silicon controlled rectifier (SCR)	Bipolar junction transistor (BJT)
Gate turn off thyristor (GTO)	Darlington transistor
MOSFET controlled thyristor (MCT)	MOSFET
Field controlled thyristor (FCT)	Injection enhanced gate transistor (IEGT)
Emitter switched thyristor (EST)	Carrier stored trench-gate bipolar transistor (CSTBT)
Base resistance thyristor (BRT)	Static induction transistor (SIT)
MOS turn off thyristor (MTO)	Field controlled transistor (FCT)
MOS and bipolar gate thyristor *MBGT)	Insulated gate bipolar transistor (IGBT)
Integrated gate commutated thyristor (IGCT)	

The IGCT is similar to a GTO with three additional features [20] [21] [22]:

- a buffer layer to reduce device thickness and hence reduce losses.
- snubberless capability for fast commutation.
- an integrated antiparallel diode.

The IGBT has the low conduction loss of a BJT and the switching speed of a MOSFET. It is voltage-driven and suitable for snubberless operation. The switching losses are very low in comparison with GTOs. Recent advancement in IGBT technology has resulted in great performance improvements. Higher voltage, more reliable and lower cost IGBT switches are readily available from various sources [20].

Table 2.2 illustrates the main differences between the IGCT and the IGBT. The first is a reverse conducting hard-switched (often termed 'snubberless') IGCT, rated at 5.5kV, 1250A, while the second is a high voltage soft-switched IGBT module, rated at 3.3kV, 1200A. The comparison demonstrates the following:

- The IGBT switching speeds are substantially better than those for the IGCT.
- The IGBT turn-off losses are lower than the IGCT.
- The IGCT has lower turn-on losses than the hard-switched IGBT, but significantly higher losses than the soft-switched IGBT.

The faster switching of the IGBTs enables higher switching frequencies to be used. This has a direct impact on equipment size and quality of waveforms supplied to the output.

A typical switching frequency for the IGCT is 500Hz. This is limited by its gate drive power requirement, di/dt limiting inductor losses and the anti-parallel diode (APD) switching performance. The switching frequency of high-power hard-switched IGBTs is >1kHz. Soft-switched high-voltage IGBTs can switch at a higher rate, typically 3kHz [19].

To implement the hysteresis-type control selected (see section 2.3.3.2), the switching frequency requirement can be determined by a simulation result shown in Fig. 2.6. It can be seen, from Fig. 2.6 (a), that the maximum switching frequency is 1kHz.

Table 2.2 Detailed comparison between IGCT and IGBT

	IGCT	IGBT
Blocking voltage	5.5kV	3.3kV
Peak rated current	1800A	2400A
Rated rms current	1250A	1200A
Max average on state current	800A	1200A
Switching type	Hard-switched	Soft-switched
Turn-on time	<10μs	1μs
Storage time	<3μs	1-3μs
Turn-off time	<10μs	0.3μs
Voltage drop V_{CE}	1.5+0.00083×*I*	1.8+0.0015×*I*
*E_{ON} (μJ/A/V/pulse)	0.17 (hard)	1.53 (hard)
		0.037 (soft)
**E_{OFF} (μJ/A/V/pulse)	1.7 (hard)	1.08 (hard)
		0.611 (soft)

*E_{ON} – turn-on losses
** E_{OFF}– turn-off losses

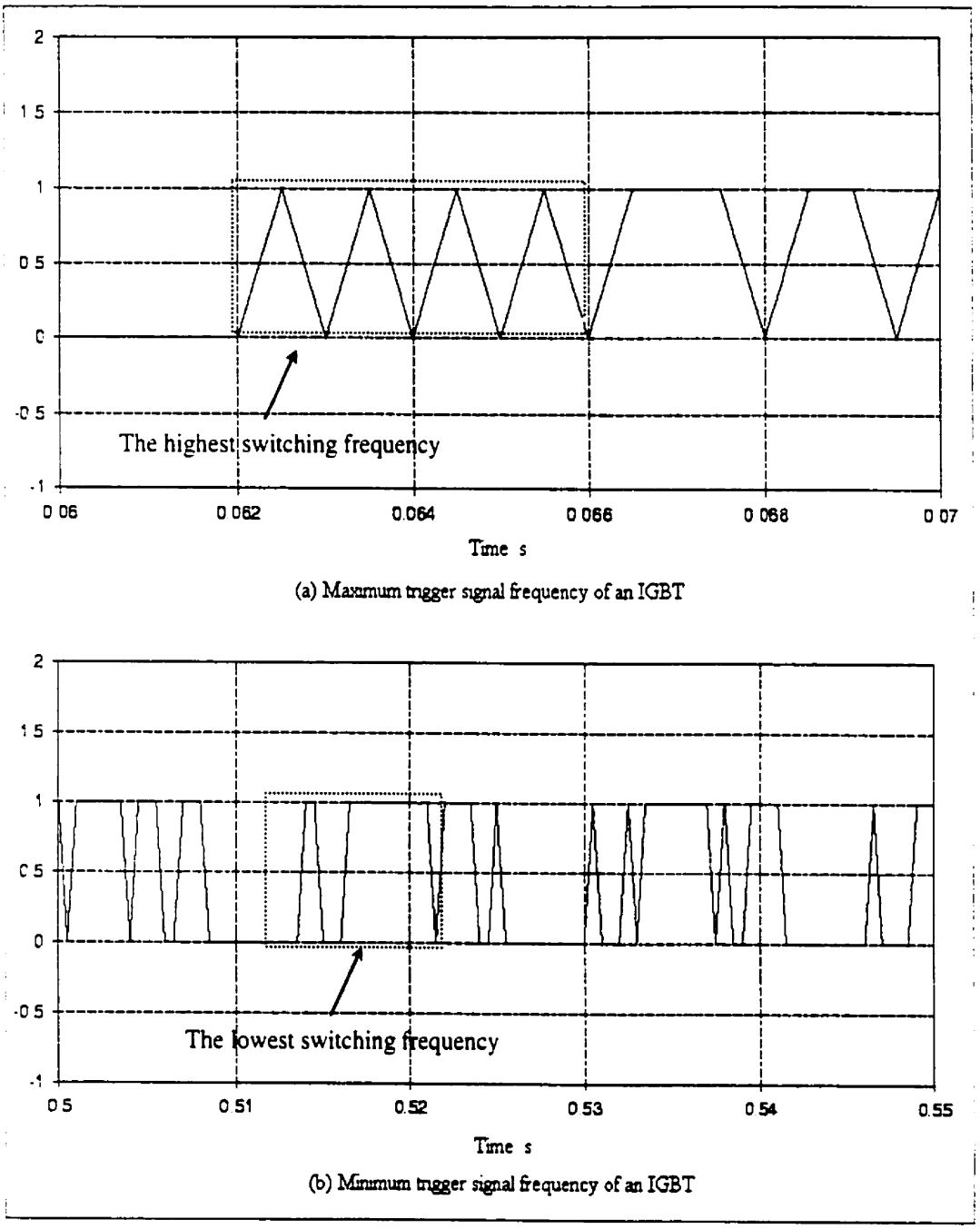


Figure 2.6. Trigger signal waveform

Based upon the above analysis, the IGCT is ruled out because its switching frequency is not high enough for the hysteresis-type control. Therefore, the soft-switched IGBT is the final choice. However, the IGBTs need to be connected in series because of their peak blocking voltage limitation.

2.3 Inverter Design

2.3.1 Categories of inverters

An inverter converts from a dc input into an ac output statically, that is, without any rotating machines or mechanical switches. The power circuit configuration of an inverter consists of semiconductor power devices that function as static switches, that is, the switch without moving contacts. The inverter also has a switching control circuit that provides the necessary pulses to turn ON and OFF each static switching element with the correct timing and sequence. These switches are repetitively operated in such a way that the dc source at the input terminals of the inverter appears as ac at its output terminals [15].

There are several types of inverters. The voltage source inverter, current source inverter, and current regulated inverter are a representative set of examples. The voltage source inverter is the most commonly used type of inverter. The ac that it provides on the output side functions as a voltage source. The input is from a dc voltage source. The input dc voltage may be from the rectified output of an ac power supply, in which case it is called a "dc link" inverter. Alternatively, the input dc may be from an independent source, such as a battery.

The current inverter generally behaves as an adjustable current source on the ac output side. The term "current source inverter" is generally used to describe a force commutated thyristor inverter that has been widely used in practical applications. The dc input to this type of inverter behaves as a current source.

The current regulated category of inverters may have a dc voltage source on the input side, but their switching is controlled in such a way that they behave as a constant current source rather than as a constant voltage source on the output (ac) side. The current source inverter is described first followed by a description of the current regulated type inverter [15].

2.3.2 Current source inverter

On the output side, this type of inverter functions as an ac current source. This type is also a dc link inverter. But, in this case, the dc link functions like a dc current source. A block diagram of the current source inverter is shown in Fig. 2.7 [15].

The dc link is provided by a phase controlled thyristor rectifier bridge. However, the phase control is made to function in such a way that the dc link current is maintained at a constant current level and equal to a reference value provided to the controller. The actual current is sensed by means of a current sensing circuit and compared against the reference current. Any error detected between the reference current and the sensed current is made to operate the phase control circuit in such a way that this error is cancelled. Although it is the dc current that needs to be sensed, the current on the ac side of the rectifier bridge is used as a measure of the dc current as shown by the current sensing circuit on the ac side of the rectifier. It is more convenient to sense the ac side current through current transformers, because they provide electrical isolation. Therefore, in practice, it is usual in current source inverters to use the rectified output of the current transformers as the feedback voltage proportional to the dc current [15].

Figure 2.2 also shows a large inductor in series with the dc link. This is an essential requirement to minimize fluctuations in the dc link current. The reason is that the

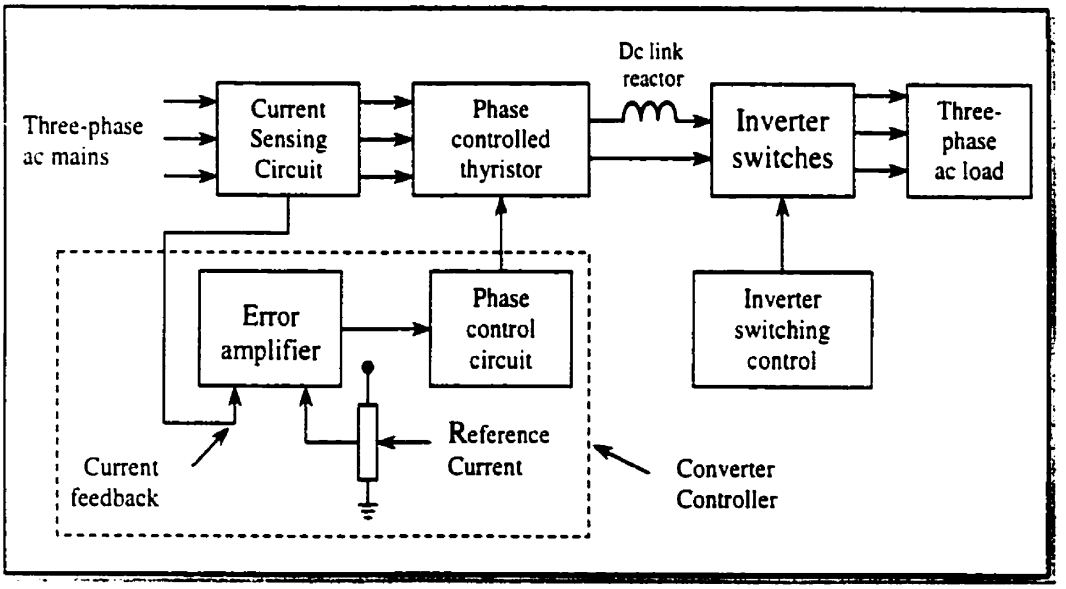


Figure 2.7. Block schematic of a current source inverter structure

switchings in the phase controlled rectifier bridge take place only at discrete intervals, and these intervals are relatively large and are dictated by the frequency of the ac mains. The dc link reactor serves to minimize current variations during the interval between successive switchings (commutations) in the phase controlled thyristor bridge. In this way, the dc link is made to function as a better current source.

The switching elements in the inverter block in Fig. 2.7 only serve to channel the dc link current to the output terminals of the inverter in such a way that the output terminals function as a three-phase current source. This is an adjustable current source, the adjustment being done by changing the reference current input to the phase controlled rectifier bridge [15].

2.3.3 Current regulated inverters

Inverters of this category are becoming increasingly more popular. The input dc is the same as in the conventional voltage source inverters. This could be a dc voltage link provided by a rectifier or an independent dc source such as a battery. The internal switching of the inverter is controlled in such a way that, at the output terminals, it behaves as an ac current source. The waveform of the current required is provided to the switching control circuit as a reference waveform.

2.3.3.1 PWM control

An inverter with pulse width modulation (PWM) control [15] is designed to make the output current conform to a reference value at every instant. In the PWM control, the switching frequency is fixed. The pulse width is determined by comparing the triangular waveform with a control voltage. This may be explained by reference to Fig. 2.8, where

v_t – triangular carrier

v_c – control voltage

i_{ref} – reference current

i_f – actual instantaneous current

Figure 2.8(a) shows one leg of the inverter bridge and one load phase (phase a). The load is shown as a series R-L circuit. The two switches of the inverter leg are labeled S_1, and S_2. Pulse width modulation is implemented by the comparison of a triangular carrier waveform v_t and an adjustable control voltage v_c. The comparator compares these two voltages, and whenever v_c is higher than v_t, the static switch S_1 is kept ON and the switch S_2 OFF. The switching instants correspond to the intersections of the triangular wave and the control voltage, as illustrated in Fig. 2.8 (b). At the instants labeled S_1 in this figure, switch S_1 is turned ON and switch S_2 is turned OFF.

Similarly, at the instants labeled S_2, switch S_2 is turned ON and switch S_1 is turned OFF. When switch S_1 is ON and switch S_2 OFF, a positive pulse will appear at the load terminal A. A negative pulse will appear at the load terminal during the intervals when switch S_2 is ON. As may be seen from Fig. 2.8 (b), for a zero value of the control voltage, the durations of the positive and negative voltage pulses will be equal. For a positive value of the control voltage, the positive pulses will be of longer duration than the negative pulses. Similarly, for a negative value of the control voltage, the negative voltage pulses will be of longer duration than the positive pulses.

To implement current controlled operation of the inverter, a reference current value is provided to the control circuit. This is the signal current labeled i_{ref} in Fig. 2.8 (a). A fast current sensing device senses the actual instantaneous current and feeds this signal back to the controller. This signal current is labeled i_f in the figure. The error detector compares the reference i_{ref} and the feedback signal i_f. Its output is the current error $i_{ref} - i_f$. This error signal is fed into the circuit block labeled "Error amplifier current controller." The output of this error amplifier serves as the control voltage, v_c, for pulse width modulation. The comparator compares the control voltage and the triangular carrier voltage, and implements the switching in the manner indicated in Fig. 2.8 (b). If the current error is positive, that is, if i_{ref} is more than i_f, then switch S_1 will be ON for a larger portion of the switching period, and the positive pulse will be wider than the negative pulse, resulting in a net increase of load current. If the current error is negative,

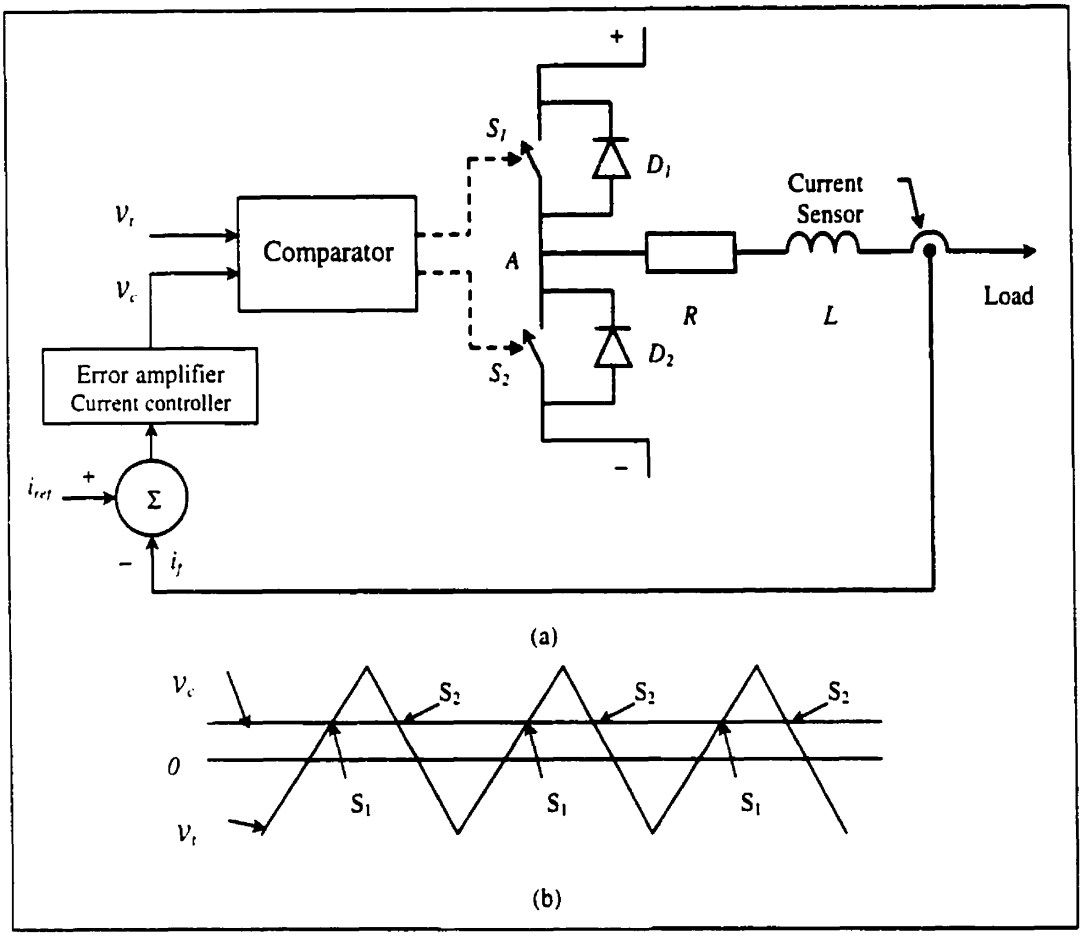


Figure 2.8. Schematic of current regulated inverter with PWM controller

the negative pulse at the load terminal will be of longer duration, resulting in a net decrease of the load current. In this manner, the current controller forces the load current to conform to the reference value. The PWM control has the property that the switching frequency has a fixed value as determined by the frequency of the triangular carrier wave. In a three-phase inverter, the individual phase currents can be controlled independently [15].

2.3.3.2 Hysteresis-type control

The principle of the hysteresis-type control strategy [15] can be described using Fig. 2.9. The required instantaneous value of the current, i_{ref}, is provided as a reference waveform. The actual value of the instantaneous phase current, i_f, is sensed by means of a

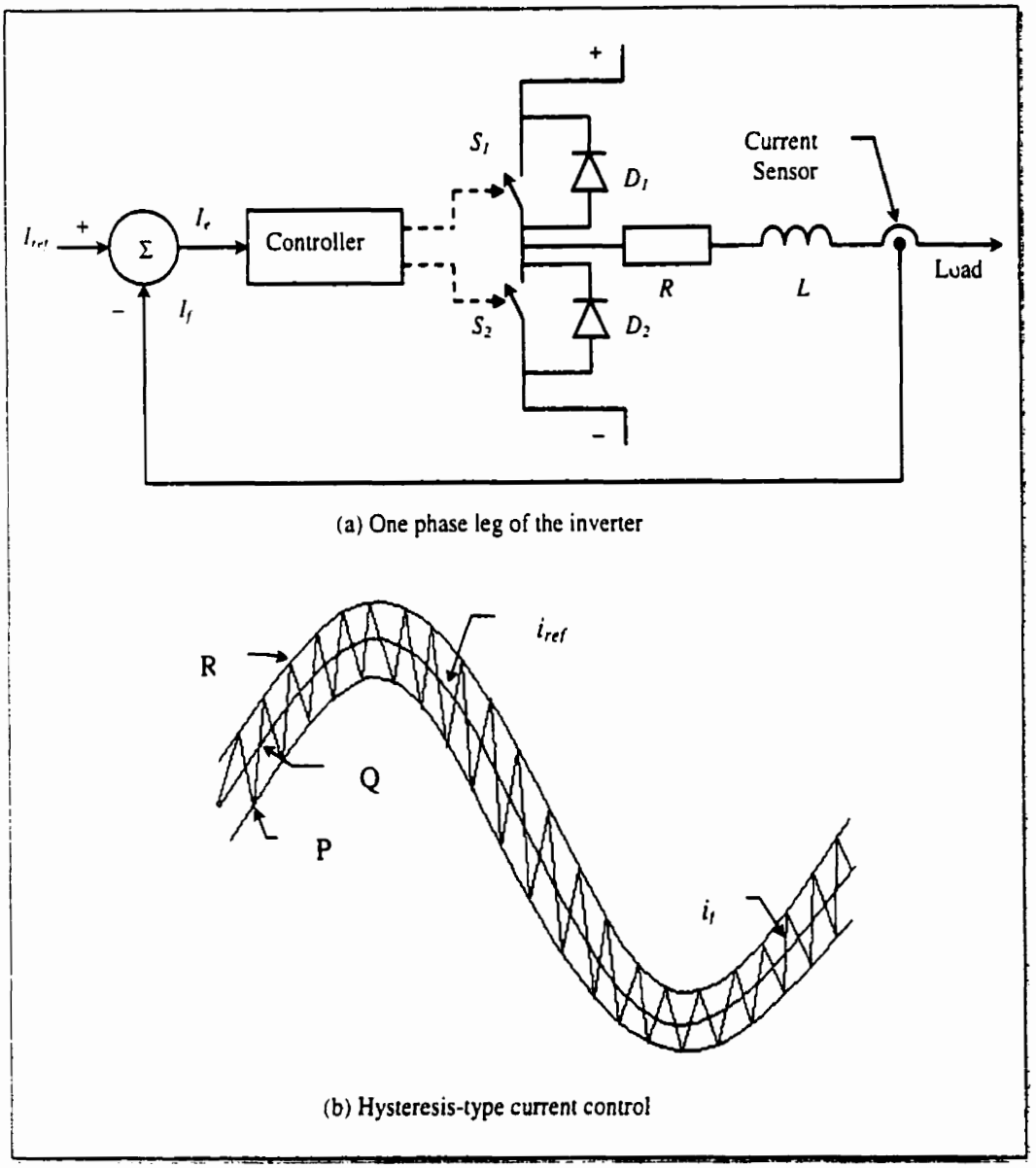


Figure 2.9. Schematic of current regulated inverter with hysteresis-type controller

fast current sensor and fed back to the control circuit. The error detector compares the reference value with the actual value, and the current error, i_e, where $i_e = i_{ref} - i_f$, is fed to the current controller.

If the current at a given instant is given by a point such as P in Fig. 2.9 (b) where the error is positive, that is, the actual current i_f is less than the required value i_{ref}, the current controller will turn OFF the switch labelled S_2 and turn ON the switch labelled S_1. This

will cause the load to be connected to the positive dc rail, and will cause the current to increase. As the current increases, the current error decreases, and becomes zero when the instantaneous current value falls on the reference waveform at the point labelled Q.

The current error then begins to be negative as the current continues to rise. At the instant when the magnitude of the negative error reaches a preset limit, corresponding to the point R, the controller causes the switch S_1 to turn OFF and switch S_2 to turn ON, thereby connecting the output terminal to the negative dc rail. As a result, the current will now start to decrease. The current error will decrease in magnitude, and become zero when the instantaneous current value falls again on the reference waveform. The error will then begin to be more and more positive. As soon as the error magnitude reaches the preset limit, the controller will again operate the switches to increase the current. In this manner, the actual current waveform will be made to follow the serrated shape shown in Fig. 2.9 (b) within an upper and a lower boundary, as sketched in this figure.

2.3.4 Choice of controller strategy

The dc input to the "current source inverter" is to behave as a current source. As shown in Fig. 2.7, it requires a large inductance between the rectifier and the inverter to form a current source. This not only results in an increase in the number of circuit elements, but also its output waveform is not good [15].

The hysteresis-type and the PWM control have a common feature that they can output better voltage and current waveforms. The switching frequency for PWM control is above 1kHz to obtain an output with low THD. The higher the frequency, the better the output. In contrast to the fixed switching frequency for PWM control, the switching frequency for the hysteresis-type control is varied.

One simulation result is shown in Fig. 2.6. It can be seen, from Fig. 2.6 (a), that the highest switching frequency is about 1kHz, while the lowest switching frequency that can be seen from Fig. 2.6 (b) is 200Hz. First, as is discussed in section 2.2, there is energy loss during the switching, which, as a result, increases both the size of auxiliary equipment for cooling and the equipment price. Second, although the switching

frequency for the soft-switched IGBT can be greater than 3kHz, the higher the switching frequency, the more complicated the snubbers. Based upon the above analysis, the hysteresis-type control is better than the PWM control for the SSPC design. Therefore, the hysteresis-type of control has been chosen for the inverter.

In view of the discussions in sections 2.2 and 2.3, the inverter based on IGBTs is designed and is shown in Fig. 2.10, where

T_{xn} – IGBT, x = a, b, c; n = 1, 2, 3, 4

G_{xm} – gate of the IGBT, m = 1, 2

i_{cx} – compensation current which will be discussed in detail in Chapter 3.

2.4 Controller Design

2.4.1 Function of the controller

To implement the hysteresis-type control, a controller has to be designed. The controller collects signals from power line and inverter output, uses this data to do necessary calculations and outputs desired control signals. Its duty is described below:

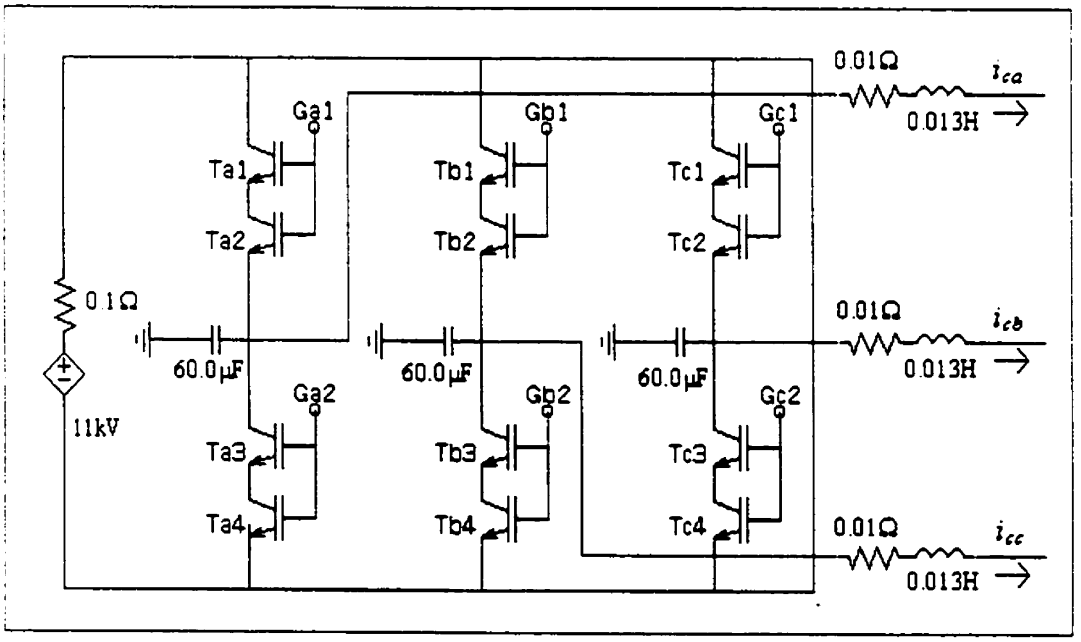


Figure 2.10. Inverter composed of IGBTs

1) Sampling of source current, load voltage, load current and compensation current signals.
2) Discrete Fourier analysis of load current.
3) Reference current synthesis according to the above calculations.
4) Control signal outputs to the IGBTs.

The architecture of the proposed controller is shown in Fig. 2.11, where

$i_{lx}(t)$, $v_{lx}(t)$ – load current and voltage of phase x in continuous-time, x =a, b, c

$i_{cx}(n)$ – compensation current of phase x in discrete-time

I, V – rms value

$i_{ex}(n)$ – error signal of phase x in discrete-time

φ – phase angle from zero crossing of a waveform

ψ_l – phase angle difference of load current and associated phase voltage

μ – power factor demand factor.

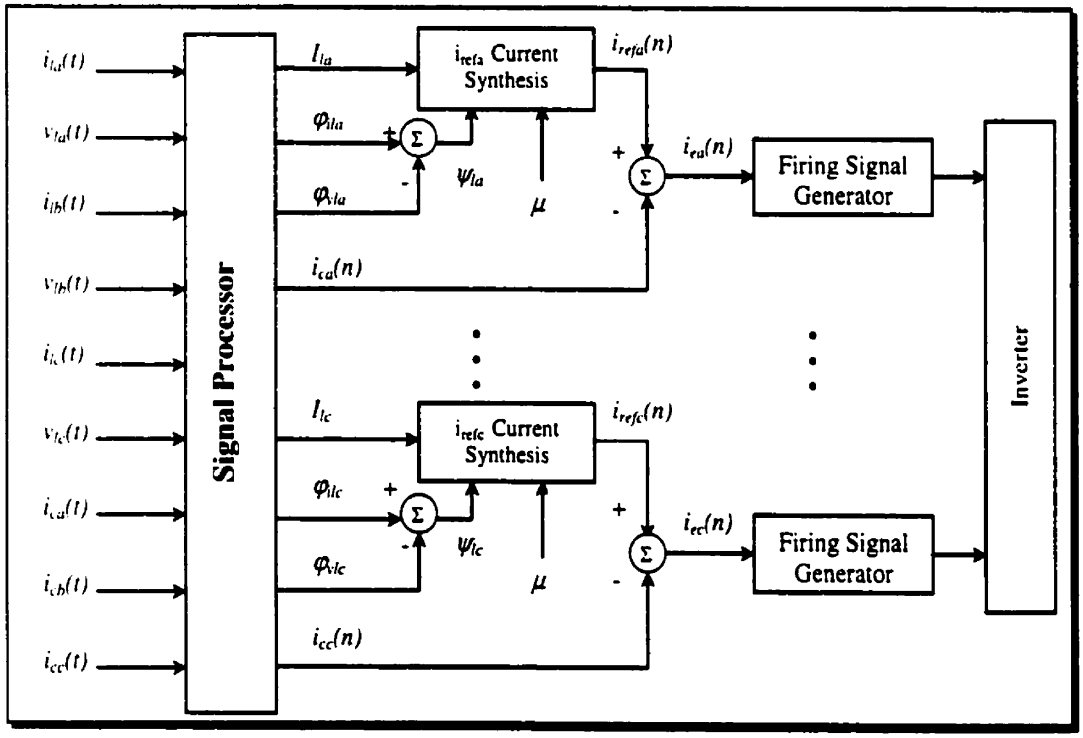


Figure 2.11. Controller structure

The basic function of the controller is described below.

An instantaneous 3-phase set of phase voltages, $v_{lx}(t)$ $(x = a, b, c)$, at the load bus is used to calculate the voltage amplitude, V_{lx}, and reference angle, φ_{vlx}, in the signal processor. An instantaneous 3-phase set of measured load currents, $i_{lx}(t)$, is decomposed into its real (in phase with voltage) or direct component, I_d, and reactive or quadrature components, I_q, and the phase angle, φ_{ilx}, of the load current of each phase is calculated. Then, the phase angle difference, ψ_{lx}, between the phase voltage and the associated load phase current is obtained. In addition, the actual instantaneous 3-phase set of the compensation currents, $i_{cx}(t)$, sensed by the current sensor is converted to discrete-time signals for calculation. According to the acquired information and given power factor demand factor, $\mu = 0.9\sim1.0$, the related reference current, i_{refx}, is determined as:

$$i_{ref} = \mu \cdot i_{lx} \sin \psi_{lx} \qquad (2\text{-}1)$$

The phase angle, φ_{refx}, of the reference current is either $\varphi_{vx}-90°$ corresponding to a capacitive load, or $\varphi_{vx}+90°$ corresponding to an inductive load.

The error module compares the required instantaneous value of the reference current, $i_{refx}(n)$, and the associated compensation current, $i_{cx}(n)$. Then a switching is made in the inverter in such a way that the error, $i_{ex}(n)$, decreases. It is possible to make the compensation current waveform very close to the reference current waveform. Therefore, the SSPC will inject currents that are almost in quadrature with their related phase voltages.

2.4.2 Considerations in Fourier analysis of load current

In signal processing, the main problem is the reference current synthesis. Several methods are available that can be employed, e.g., the cubic spline algorithm, ideal interpolation and the discrete-Fourier transform, DFT.

The cubic spline algorithm is very suitable for curve-fitting [23], but in SSPC operation, it would require an excessive time to reconstruct the original signal.

The ideal interpolation method is a convolution of a discrete-time signal, *x(n)*, with a sinc function [24]:

$$x(t) = \sum_{n=-\infty}^{\infty} x(n) \frac{\sin[\pi(t - nT)/T]}{\pi(t - nT)/T} \qquad (2\text{-}2)$$

where

x(t) – a continuous-time signal;
x(n) – discrete-time representation of x(t) ;
T – sample period;
n – an integer.

Again, this procedure requires excessive computation. Therefore, it is necessary to seek a better real-time signal processing method.

The DFT has the advantage of a shorter processing time than for the above two techniques, which makes it suitable for real-time applications. It is defined as [24]:

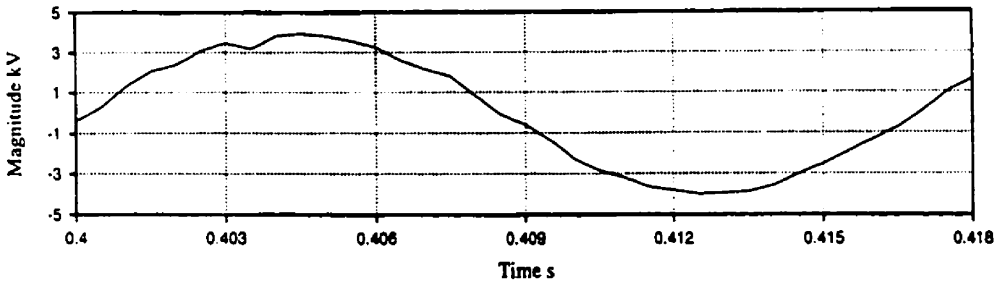
$$X(m) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi mn/N} \qquad (2\text{-}3)$$

where

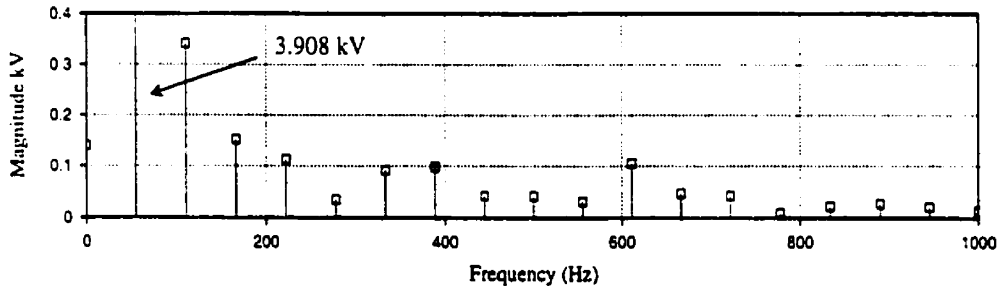
X(m) – discrete Fourier transform of x(n);
m – an index of discrete frequency;
N – data window length;
n – an integer.

To calculate the magnitude of a sinusoidal signal from the acquired information, one only needs to calculate *X(1)* for the current synthesis, because the harmonics in the signal are very small if the inverter is carefully designed.

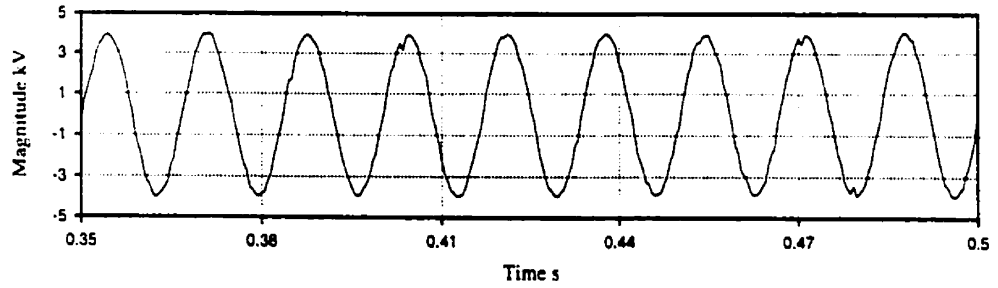
The DFT is used to compute the Fourier coefficients of the sequences of a discrete line current. There must be a whole number of sample intervals in the Fourier analysis period. So, $T_S = T/N$, where T is the period of the sampled signal, T_S is the time between samples and N is the number of samples in the Fourier analysis interval. In contrast, in the Fourier series for continuous-time waveforms, there are only k sinusoid sequences that



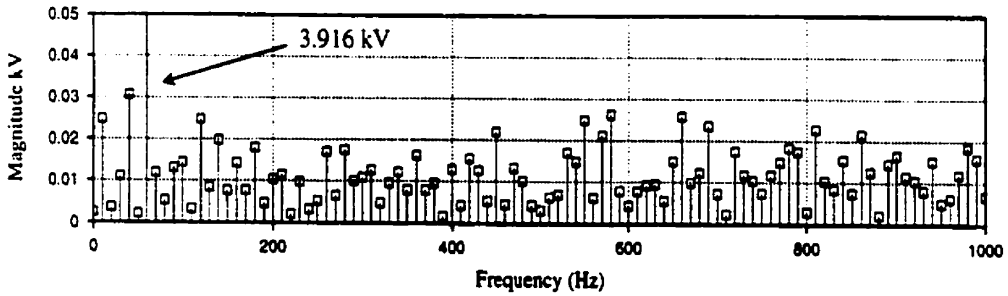
(a) Sample voltage waveform with incorrect T-period



(b) Fourier analysis of (a)



(c) Sample voltage waveform with correct T-period



(d) Fourier analysis of (c)

Figure 2.12. Fourier analysis of a sample waveform

- are T-period, or in other words, are harmonics of the fundamental f = 1/T.
- are distinct at the sample points.

There are three significant sources of error that often corrupt the results computed by a Fourier analysis:

- Incorrect period.
- Interpolation
- Aliasing

Only error caused by incorrect period is discussed here [24].

Fourier analysis inherently assumes that the waveforms are T-periodic, where T is the Fourier analysis interval. Waveforms that are not T-periodic are periodically extended by ignoring everything outside the Fourier analysis interval and replicating the waveform within the interval. If the period of the signal does not match the Fourier analysis interval, a discontinuity is generated. If the signal is not sampled at the T-period, unreasonable harmonics will occur. Figure 2.12 shows the comparison of Fourier analysis with different analysis intervals for the same waveform. The waveforms are shown in Fig. 12 (a) and (c), respectively, while their Fourier analysis results are shown in Fig. 12 (b) and (d), respectively, from which it can be seen that there is much difference between them. The THD in Fig. 12 (b) is 15.66%, while the actual THD of the signal shown in Fig. 12(d) is 4.8061%. The magnitudes of various harmonics are very small compared to that of the fundamental. In order to be able to show the harmonics in Figs.2.12(b) and (d), only the numerical value of the magnitude of the fundamental is given in these figures.

A detailed discussion about Fourier analysis using DFT is carried out in section 3.2.

CHAPTER 3

SSPC DESIGN

Specifications of the three-phase 60 Hz physical system used in the studies are: [1]

Generator G – 20 MVA, 10kV

Transmission line – 50 kV

Transformer T_1 – 20 MVA, 10kV/50kV

Transformer T_2 – 20 MVA, 50kV/5kV

Load – 18 MVA, 5kV

The schematic diagram of a power system is shown in Fig. 3.1. Obviously, the SSPC is of primary concern here.

The SSPC is composed of a dc source, inverter, controller, series filter and parallel filter. Actually, the dc source is a phase-controlled converter that can output adjustable dc voltage. The inverter is a hysteresis-type regulated current source that can provide variable ac current to the load. The controller employs hysteresis-type control. All these component designs have been introduced in Chapter 2. In addition, the series and parallel

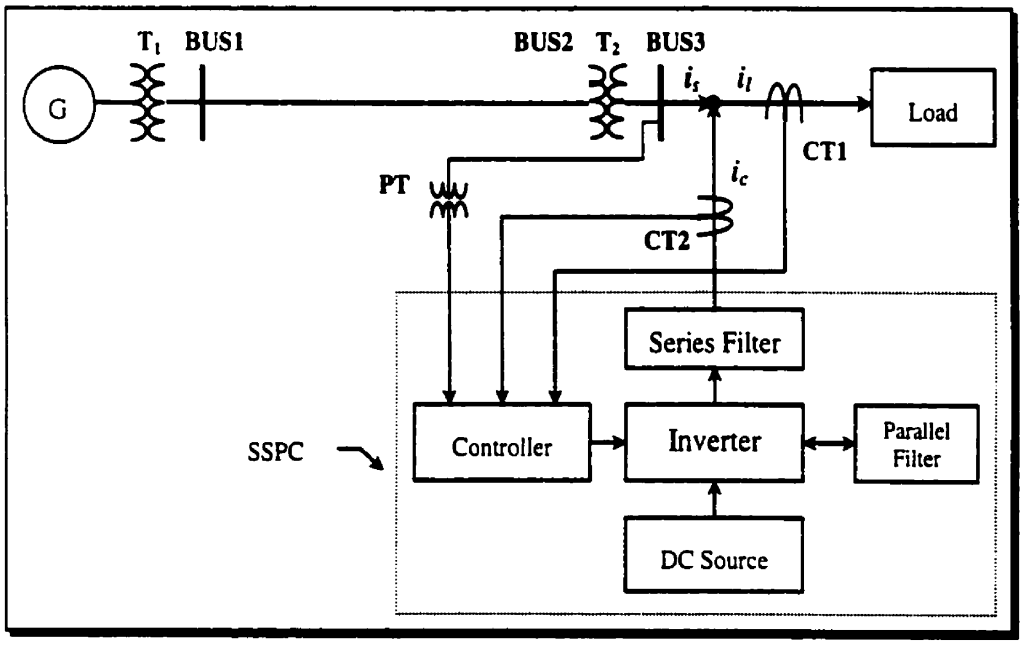


Figure 3.1. Schematic diagram of a power system

filters are employed for smoothing output currents coming from the SSPC and for avoiding distortion of line voltage.

Before introducing the SSPC design, Fourier analysis of the currents and voltages has to be performed and the relative THDs should be calculated, because the analysis and calculation will be used to evaluate the performance of the SSPC.

3.1 Fourier Analysis of the SSPC Outputs

Fourier analysis of SSPC outputs can be proceeded in two parts: single-phase Fourier analysis and three-phase Fourier analysis.

3.1.1 Single-phase Fourier analysis

In the single-phase Fourier analysis, the main issue is to determine the distortion of the waveforms, which can be expressed mathematically by using THD, defined as:

$$THD = \frac{\sqrt{I^2 - I_f^2}}{I} \times 100\ \% \qquad (3\text{-}1)$$

where

I – rms current

I_f – fundamental frequency rms current [15].

As discussed in section 2.4, DFT can be applied only when a waveform is T-periodic and matches Fourier analysis interval. Fortunately, the waveforms coming from SSPC are 60 Hz-based with some harmonics. Therefore, DFT can be used in the analysis.

The procedure of single-phase Fourier analysis can be described as below:

- Using Eq.(2-3) calculate the coefficients for all desired harmonic components.
- Using Eq.(3-1) calculate THD.
- Evaluate the performance of the SSPC according to the THDs obtained

An example of single-phase DFT analysis is shown in Fig.3.2, from which it can be seen that there are harmonics in the magnitude frequency spectra, because the waveform is distorted. Again to be able to show the harmonics, only the numerical value of the magnitude of the fundamental is indicated in the figure.

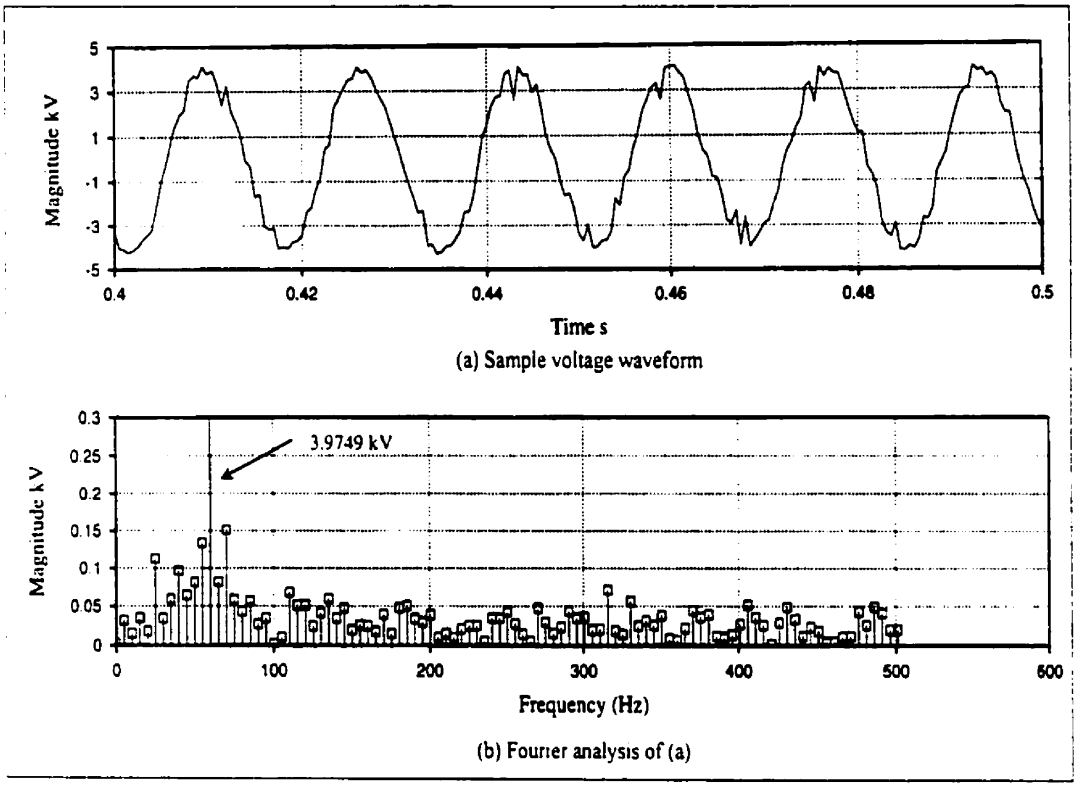


Figure 3.2. Example of single-phase Fourier analysis

3.1.2 Three-phase Fourier analysis [25]

The single-phase Fourier analysis can estimate the THD of the system. However, are the three phases symmetric? If the three-phase signals are not symmetric the system will be more inefficient and have a greater chance of instability. Using three-phase Fourier analysis, it is possible to determine if the three-phase signal is symmetric. The three-phase Fourier analysis is based on the single-phase Fourier analysis. Equation (3-2) shows the relationships between the sequence network Fourier transforms and the single-phase Fourier transforms:

$$
\begin{aligned}
F_+[i] &= \frac{F_a[i] + F_b[i]e^{-j\frac{2\pi}{3}} + F_c[i]e^{j\frac{2\pi}{3}}}{3} \\
F_-[i] &= \frac{F_a[i] + F_b[i]e^{j\frac{2\pi}{3}} + F_c[i]e^{-j\frac{2\pi}{3}}}{3} \\
F_0[i] &= \frac{F_a[i] + F_b[i] + F_c[i]}{3}
\end{aligned}
\qquad (3\text{-}2)
$$

where

$F_+[i]$ – positive sequence network Fourier transform, i = 0, 1, ... M (maximum harmonics considered).

$F_-[i]$ – negative sequence network Fourier transform.

$F_0[i]$ – zero sequence network Fourier transform.

Figure 3.3 shows one of the test results for three-phase Fourier analysis, from which it can be seen that the magnitudes of the negative and zero sequences of three-phase compensation currents are much smaller than that of the positive sequence, because the three-phase signals are symmetric and there is small distortion in the waveforms.

In this test, the THDs are: THD of i_{ca} =2.8645%, THD of i_{cb} =1.3551%, THD of i_{cc} =1.7608%

Another example presented in Fig.3.4 indicates that the system is asymmetric. Although its THDs are very small (THD of i_{ca} = 3.6857%, THD of i_{cb} = 2.8868%, THD of i_{cc} = 3.2187%.), the magnitude spectra of the negative and zero sequence are relatively high. Therefore, it is necessary to justify the property of a system using both single-phase and three-phase Fourier analysis.

3.2 DC Voltage Selection

Recall the description in section 2.3. The principle of hysteresis-type control method is to reduce the difference between the compensation current, i_{cx}, and the reference current, i_{ref}, according to the detected signal. The adjustment of i_{cx} depends on the level of the dc link voltage, the loads connected and the instantanous value of the reference current. On the one hand, the higher the voltage, the faster i_{cx} will be adjusted. On the other hand, if the voltage is not properly fixed, there will be sawteeth in the compensation current and phase voltage, which is shown in Fig. 3.5. Its THD is as high as 30.46%. In this simulation, the dc link voltage is fixed at 15kV, the cause of the distrotion is that the dc link voltage is much higher than the ac line voltage. Therefore, the injected current not only flows to the load, but also flows to the power source, which results in the voltage distortion.

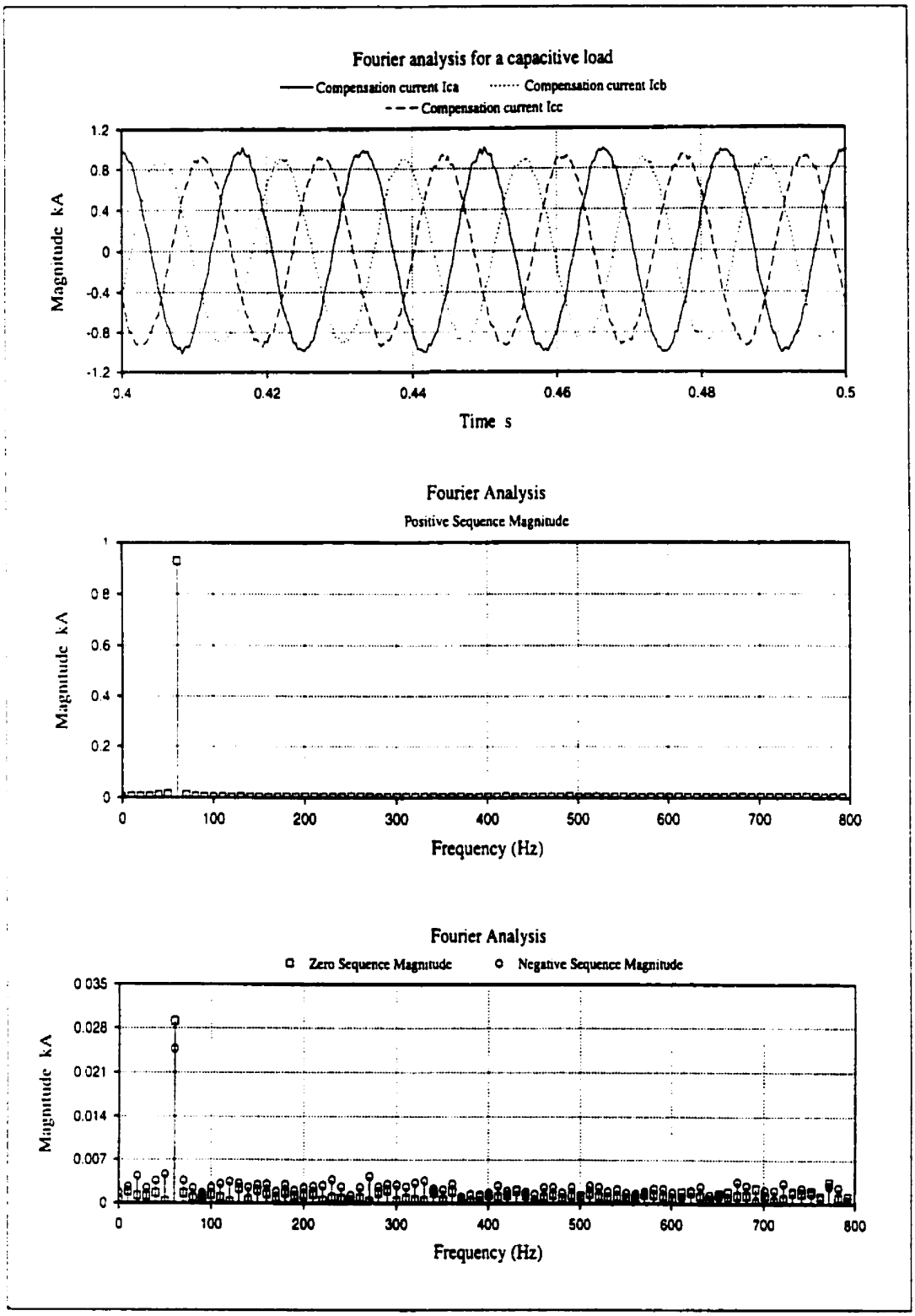
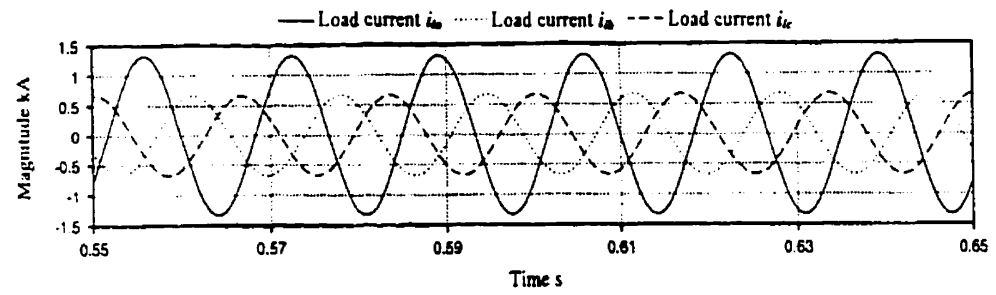
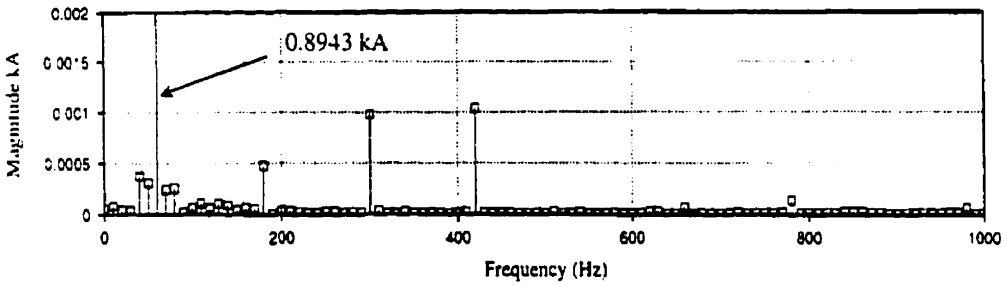


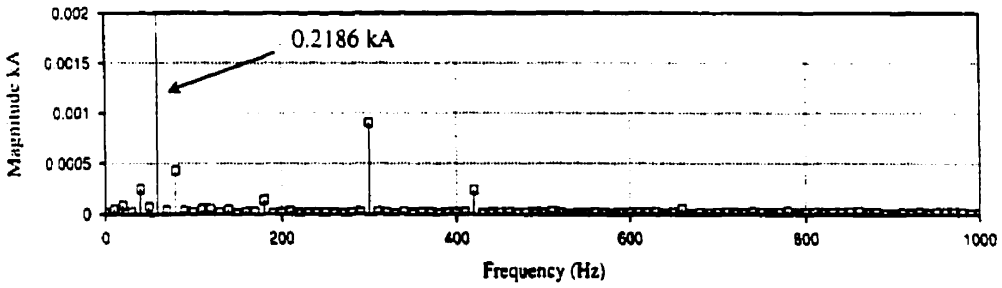
Figure 3.3. Three-phase Fourier analysis



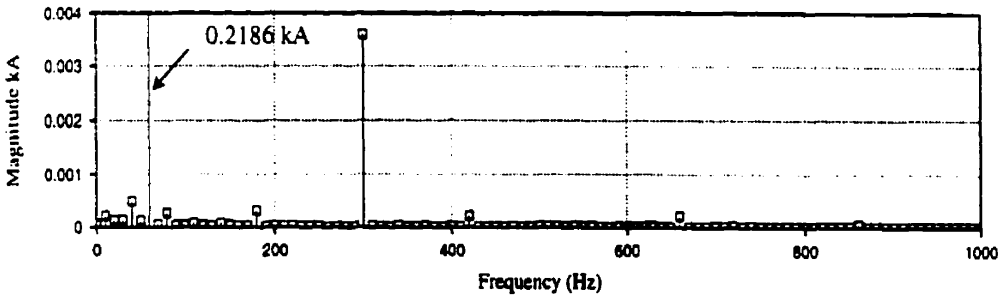
(a) Sample voltage waveform from an unbalanced system



(b) Magnitude spectra of positive sequence



(c) Magnitude spectra of zero sequence



(d) Magnitude spectra of negative sequence

Figure 3.4. Fourier analysis for an asymmetric system

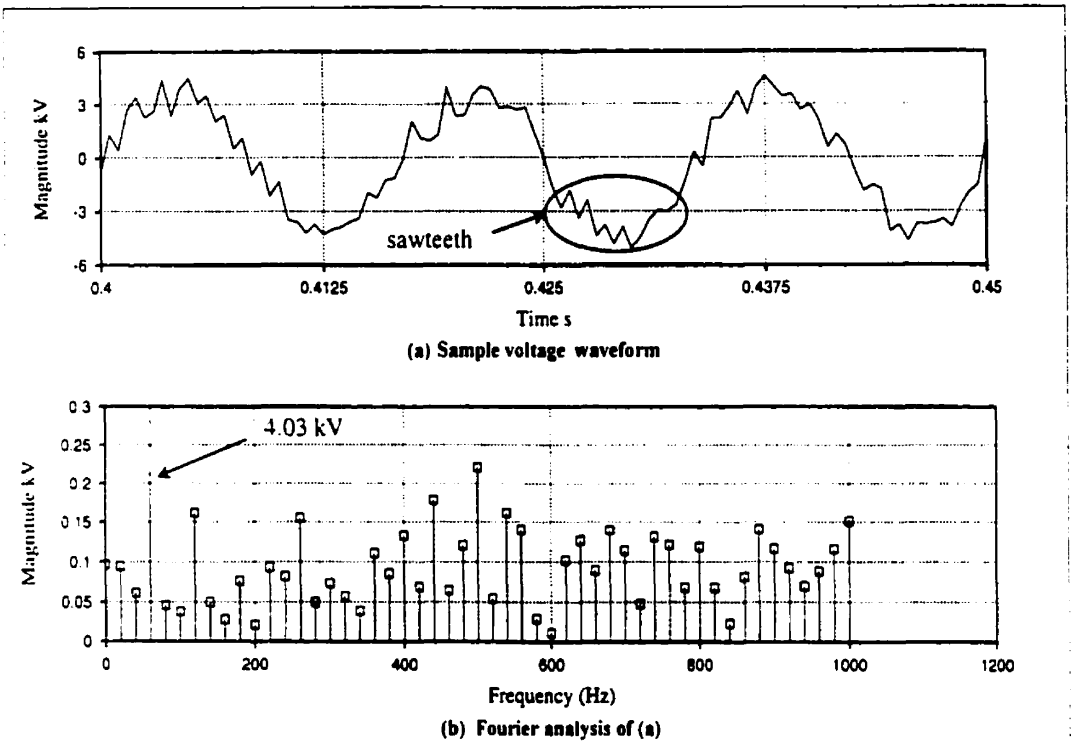


Figure 3.5. Fourier analysis for improper dc voltage setting

The dc voltage selection is determined according to the analysis of the inverter shown in Fig.2.10. As is known, the ac line voltage in the system is 5kV in this system. When the inverter injects the compensation currents to the ac system, the dc voltage must be higher than the ac voltage, which means that the dc voltage, V_{dc}, should be more than 5kV. The second consideration is the voltage distribution. The dc voltage is divided into two parts. One is the positive part that is connected to the switches on the higher rail. The other part is the negative part that is connected to the switches on the lower rail. Therefore, V_{dc} should be double the ac line voltage.

Hundreds of tests have been made to determine the dc voltage suitable for industry application. Tests based on V_{dc} below 10kV indicate that no matter how the inductance for series filter and the capacitance for parallel filter are selected, either the THDs of the currents or the THDs of the voltages are greater than 5%, which is shown in Table 3.1 for V_{dc} = 8kV (Figs.3.6 through 3.9) and Table 3.2 for V_{dc} = 9kV (Figs.3.10 through 3.13).

Table 3.1 Test results for V_{dc} = 8kV

Inductance (H)	Capacitance (μF)	THD of i_{ca}	THD of i_{cb}	THD of i_{cc}	THD of i_{ca}	THD of i_{ca}	THD of i_{ca}
0.006	20	6.4225	7.0251	5.8090	10.275	10.2342	12.2095
	40	6.8935	7.3629	6.4022	9.1513	9.4064	9.9064
	60	7.6948	7.3602	6.8752	9.9921	8.7037	10.0853
	80	7.3458	7.7885	6.4906	7.6430	9.4774	10.0603
	100	7.1712	7.8091	6.7027	9.8173	9.6534	9.1283
0.008	20	6.7937	6.9615	6.1872	8.6357	9.1117	8.7428
	40	7.3480	7.2515	6.5724	7.3103	7.8742	8.2710
	60	7.2188	7.8047	6.9292	6.6293	6.7981	8.3779
	80	7.6465	6.7904	6.1298	7.1866	7.2847	7.6667
	100	9.1102	8.6489	7.5133	8.1422	8.7701	8.9238
0.01	20	6.7540	7.2462	6.7503	10.1138	10.1632	10.2578
	40	7.3309	7.8319	6.7653	8.3645	8.8529	8.3640
	60	8.3318	8.5988	8.1868	7.3902	6.8734	7.6220
	80	9.2459	8.2634	7.9356	6.6517	6.9121	6.1832
	100	8.6169	9.2339	8.1107	7.1548	6.8997	6.8103
0.012	20	7.9996	7.4998	6.5568	7.8522	7.6932	8.4671
	40	8.0254	8.1791	7.0315	7.3891	6.7514	6.6558
	60	8.8836	8.9838	7.8086	7.0842	6.9717	7.5146
	80	9.5597	10.0208	10.2974	6.6359	6.3627	6.3713
	100	9.5778	9.0927	7.2177	7.2840	6.6074	6.2692

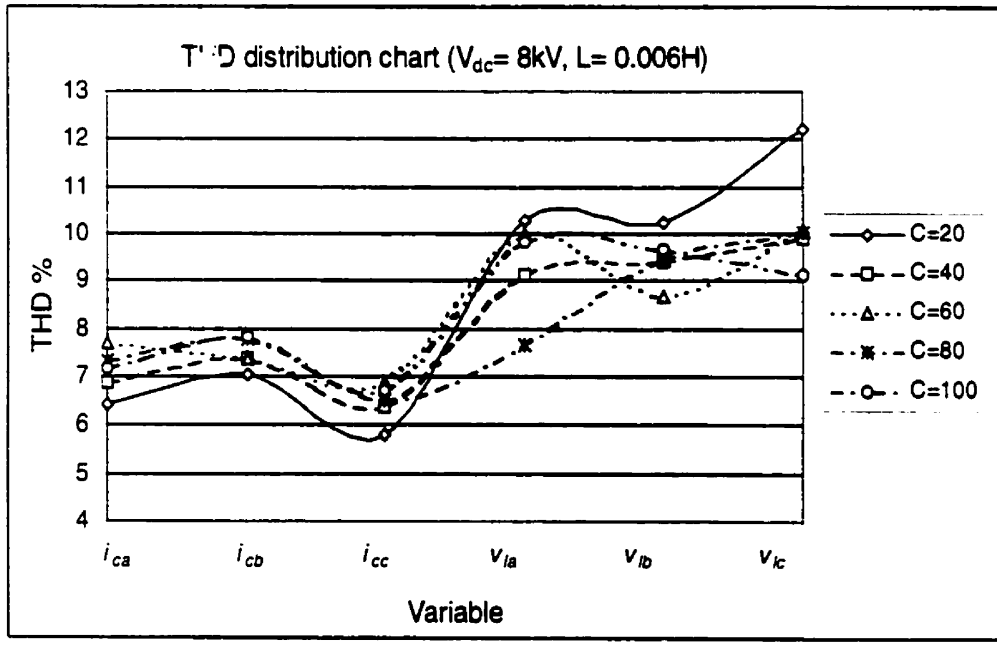


Figure 3.6. THD for test result 1

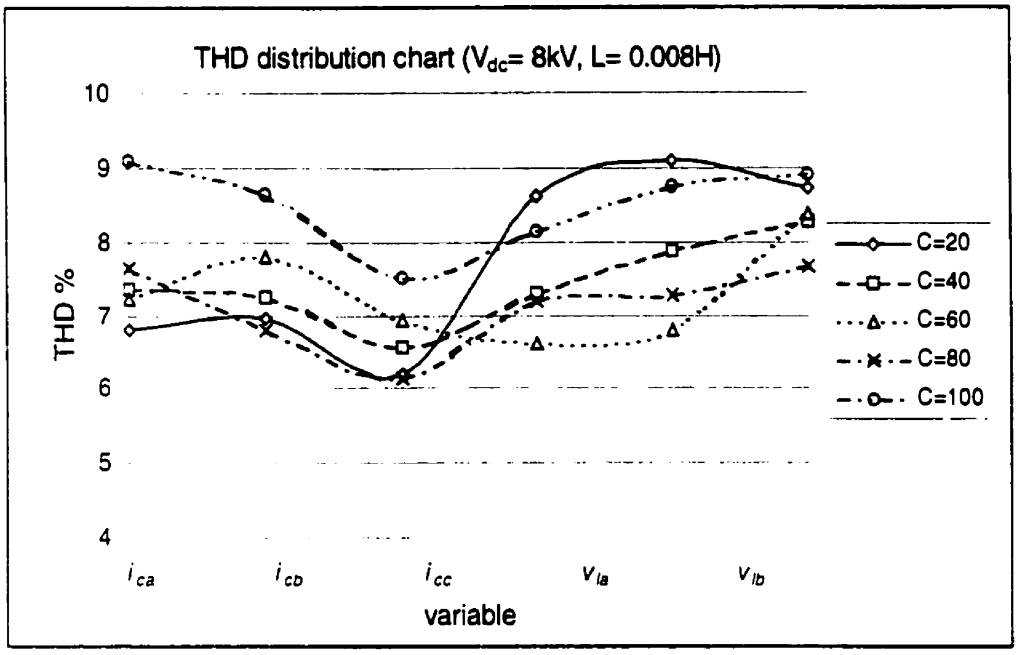


Figure 3.7. THD for test result 2

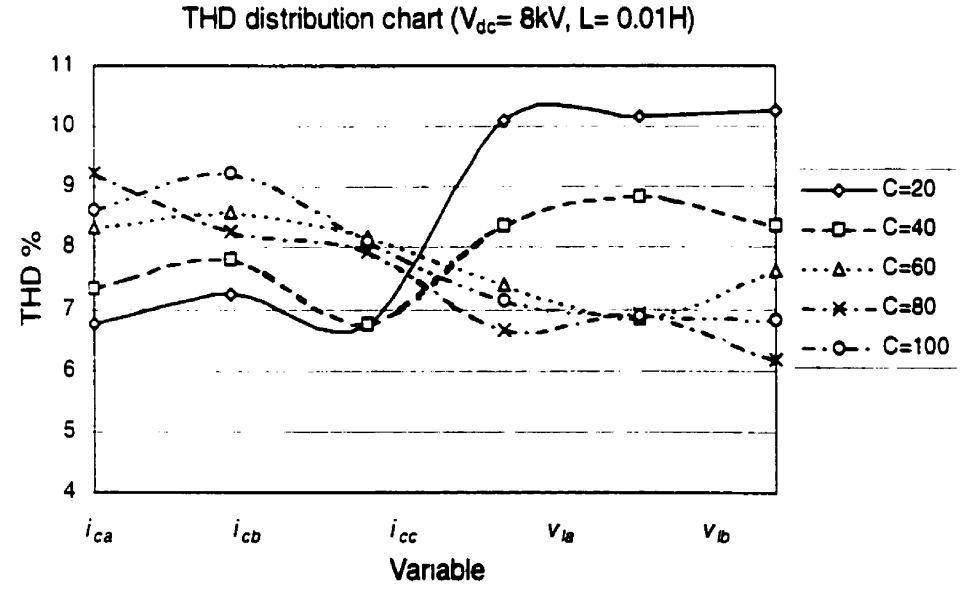


Figure 3.8. THD for test result 3

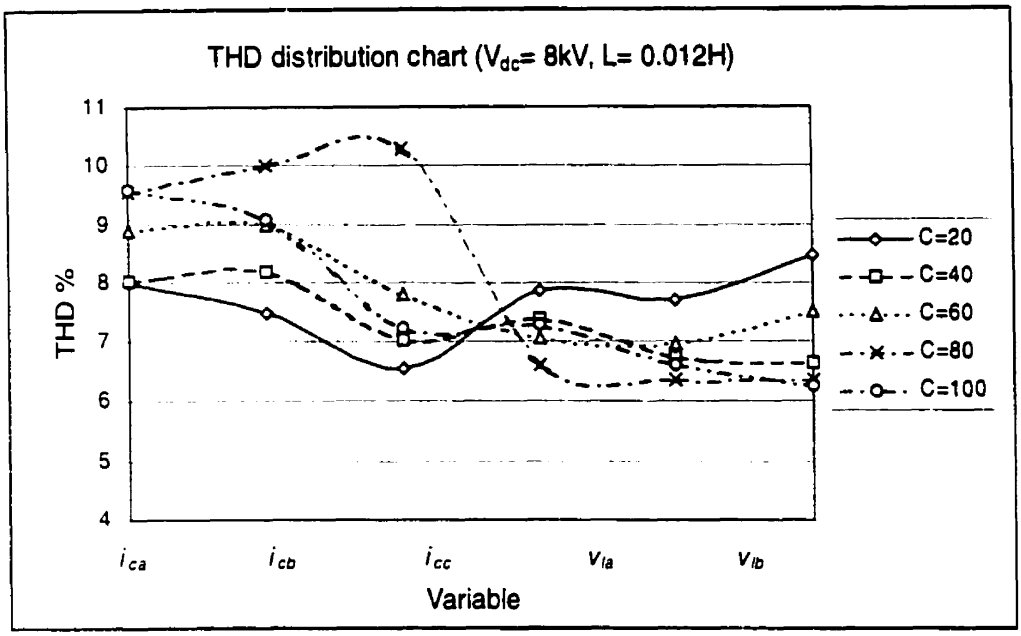


Figure 3.9. THD for test result 4

Table 3.2 Test results for V_{dc} = 9kV

Inductance (H)	Capacitance (μF)	THD of i_{ca}	THD of i_{cb}	THD of i_{ca}	THD of i_{ca}	THD of i_{ca}	THD of i_{ca}
0.007	30	7.1203	6.8655	6.3069	9.7338	9.9757	10.8131
	50	6.6498	6.8638	6.1989	8.9246	10.4689	8.9503
	70	6.9578	7.1448	6.1161	8.7288	8.7019	8.3652
	90	6.855	7.5153	6.2901	8.2968	8.2804	8.4098
	110	7.3313	7.4157	6.5555	9.1525	9.0965	8.851
0.009	30	6.4029	6.7462	6.0957	8.4705	9.8453	9.279
	50	7.3171	6.9467	6.3065	8.1765	7.2901	8.085
	70	7.3509	7.5541	6.556	8.401	7.0294	7.8769
	90	6.7561	7.8139	6.2931	6.0225	8.5016	8.1859
	110	7.8846	7.9609	7.2718	6.464	7.4288	6.0806
0.011	30	4.21393	4.80833	3.0326	5.0991	5.3745	6.7116
	50	5.9989	5.7089	3.8979	4.4423	4.231	5.0981
	70	6.347	6.2197	4.5932	5.3595	5.1491	5.3114
	90	6.4581	6.6692	5.5054	4.6019	4.8521	4.7656
	110	6.7132	6.5759	5.4609	4.8081	4.6415	4.0898
0.013	30	5.3569	5.5465	4.0823	5.0073	5.2639	5.3586
	50	5.5726	6.4786	4.0363	4.5005	4.1896	4.0583
	70	6.3087	7.7488	4.6619	4.7034	4.2831	4.4082
	90	6.8672	8.0179	6.4293	3.4779	3.6692	4.0311
	110	6.6026	7.2392	7.4296	3.6988	4.2127	3.8789

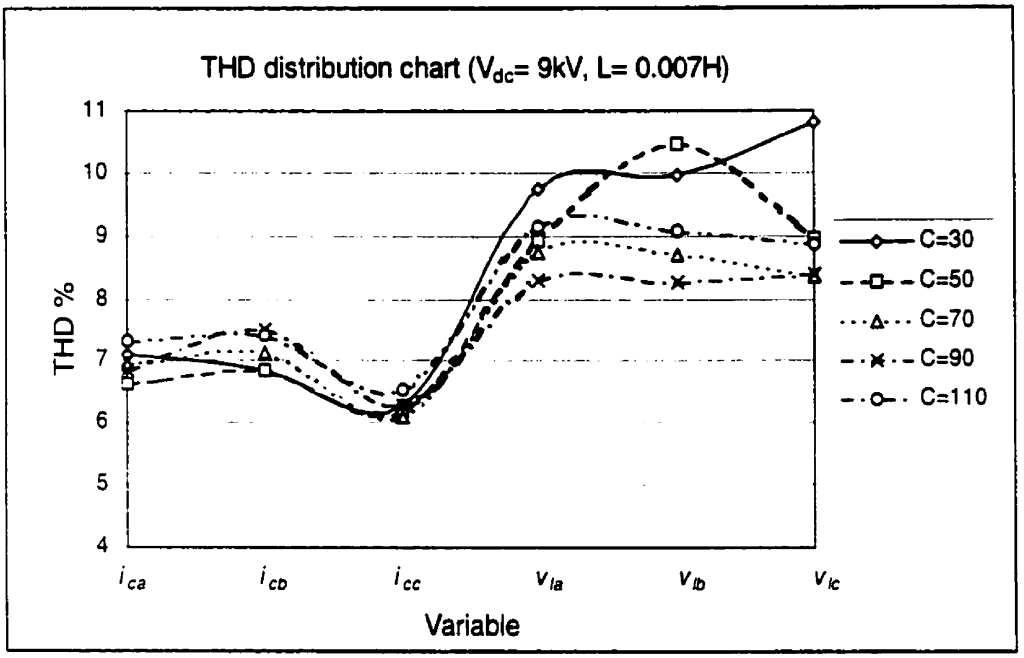


Figure 3.10. THD for test result 5

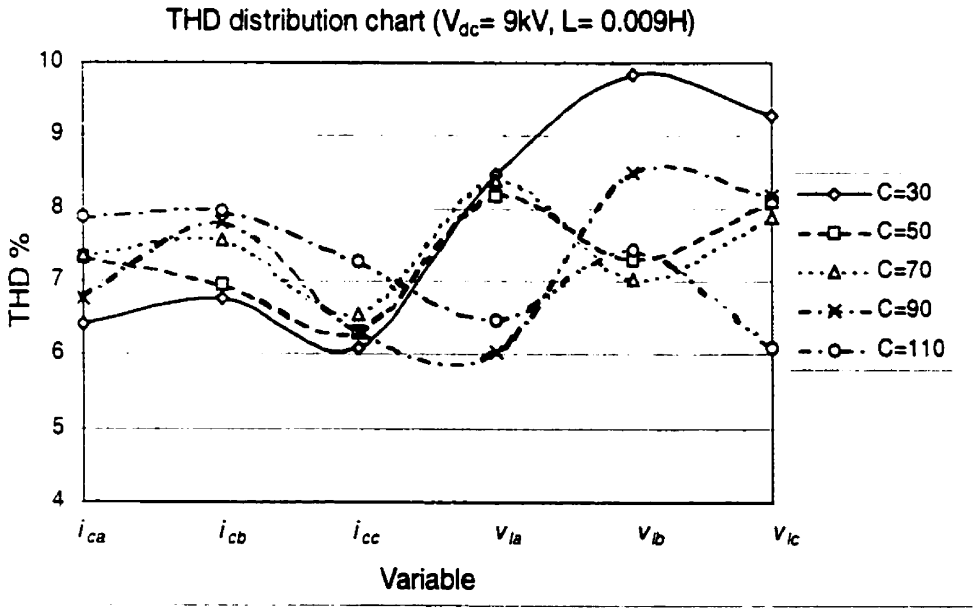


Figure 3.11. THD for test result 6

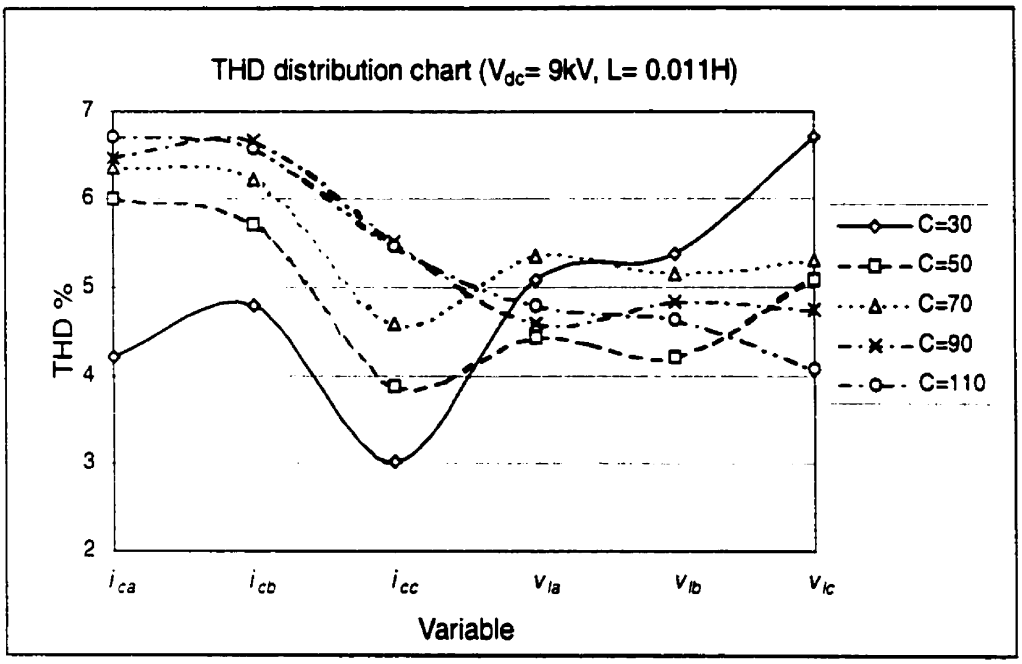


Figure 3.12. THD for test result 7

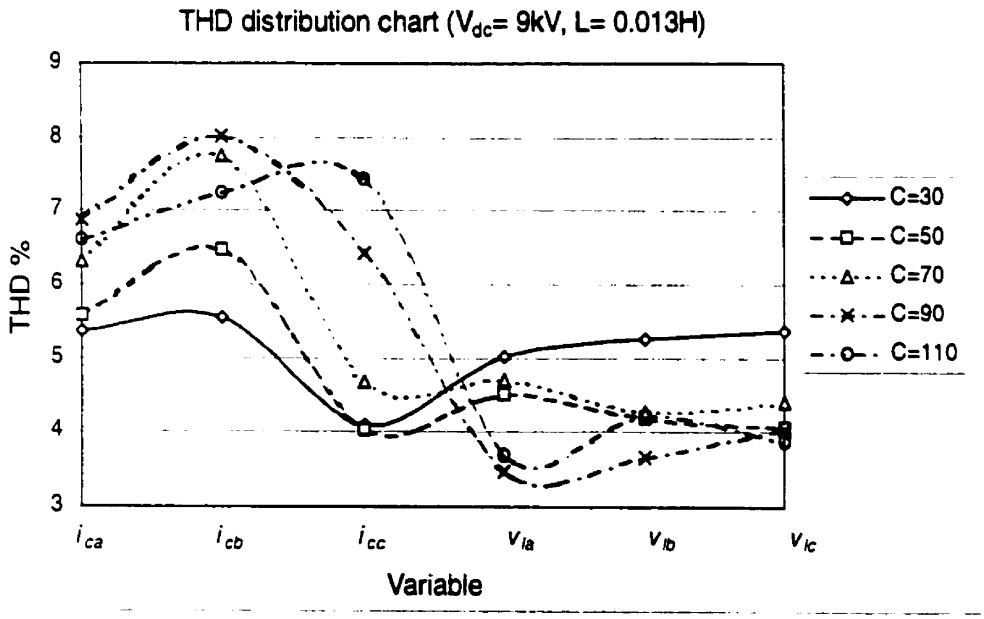


Figure 3.13. THD for test result 8

To minimize this distortion, the dc link voltage was varied between 7kV and 15 kV. The simulation results showed that V_{dc} can be chosen between 10 and 11kV along with the

other parameter adjustments. Of course, if V_{dc} is higher than 11kV, the performance of the inverter is good. But the price is increasing both the dc voltage and the inductance and the capacitance values.

3.3 Parallel Filter Setting

As mentioned above, the switching frequency is relatively high for the hysteresis-type control. As a result, there are high frequency harmonics in the currents and voltages. As is known, the capacitive reactance is the reciprocal of signal frequency. Therefore, a capacitor can filter high frequency signal when connected in paralllel. To smoothen the SSPC outputs, capacitor can be connected in parallel with the SSPC. Moreover, the capacitance has to be selected carefully. Improper setting of the capacitance can not help improve the voltage and current waveforms.

An example of improper parallel setting is shown in Fig.3.14, where

V_{dc} = 10kV

L = 0.012H

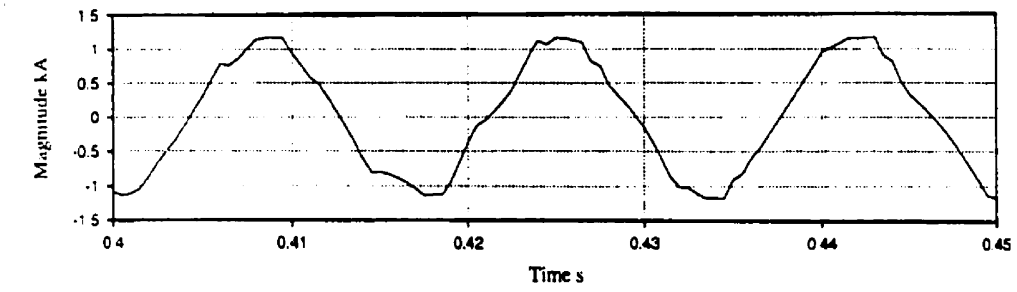
C = 1000μF.

The THD of the voltage is 10.5667%. Obviously, the value exceeds the upper limit for THD requirement.

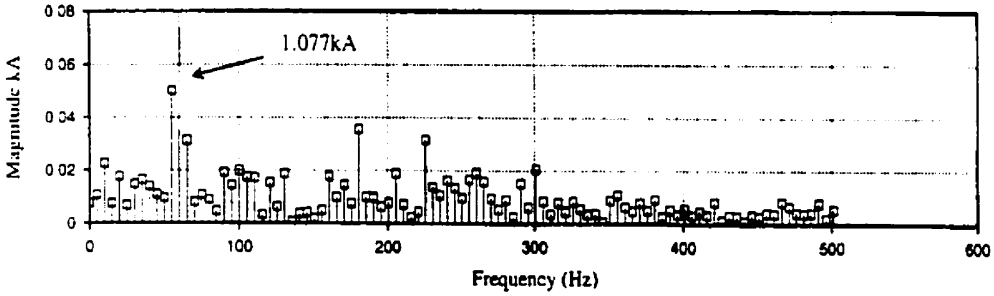
The proper capacitance is determined by changing its value based on the fixed dc voltage and inductance as series filter shown in Tables 3.1 through 3.4 and the corresponding charts. The proper capacitance is varied with V_{dc} and the inductance, e.g., the capacitance for applicable operation is C = 130μF based on L = 0.01H and V_{dc} = 10kV, while another possible selection is C = 60μF based on L = 0.013H and V_{dc} = 11kV.

3.4 Series Filter Setting

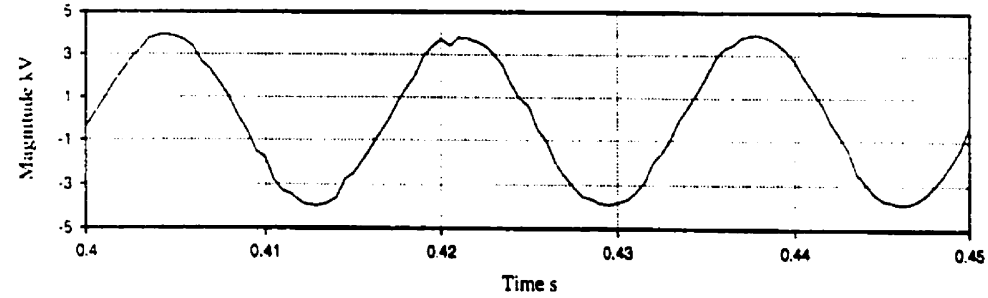
As is known, inductive reactance is proportional to signal frequency. Therefore, an inductor can minimize the high frequency harmonics in the signals when it is connected in series with the system. In addition to the inductor, a resistor has to be put in use as a damper. To smoothen the output waveforms of the SSPC, the inductor and the resistor are



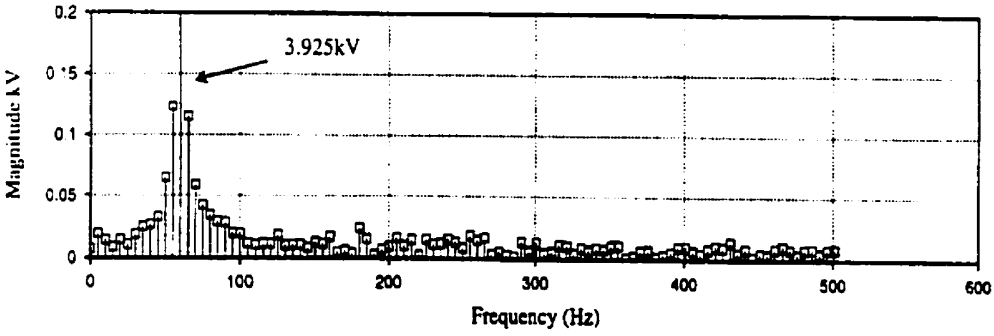
(a) Sample current waveform



(b) Fourier analysis of (a)



(c) Sample voltage waveform



(d) Fourier analysis of (c)

Figure 3.14. Fourier analysis for improper parallel filter setting

connected in series with the SSPC. Moreover, their parameters must be set appropriately. Improper setting of the inductance can not help improve the voltage and current waveforms.

An example of improper series setting is shown in Fig.3.15, where

V_{dc} = 10kV

L = 0.003H

C = 50μF.

The THD of the voltage is 15.8254%. Obviously, the value exceeds the upper limit for THD requirement.

The proper inductance is determined by changing its value based on the fixed dc voltage and the variation of the capacitance as parallel filter shown in Tables 3.1 to 3.4 and corresponding charts. The inductance is also varied with V_{dc} and the capacitance, e.g., the inductance for applicable operation is L = 0.012H based on C = 50μF and V_{dc} = 10kV, while another possible selection is L = 0.015H based on C = 40μF and V_{dc} = 11kV.

Based on the above design and simulation studies, the outputs of the SSPC are improved after changing the parameters to appropriate settings. One of the results that the THDs for both the currents and the voltages are below 5% is shown in Fig.3.16, which means the performance of the SSPC meets the technical requirements for industry application. In this case, the parameters are

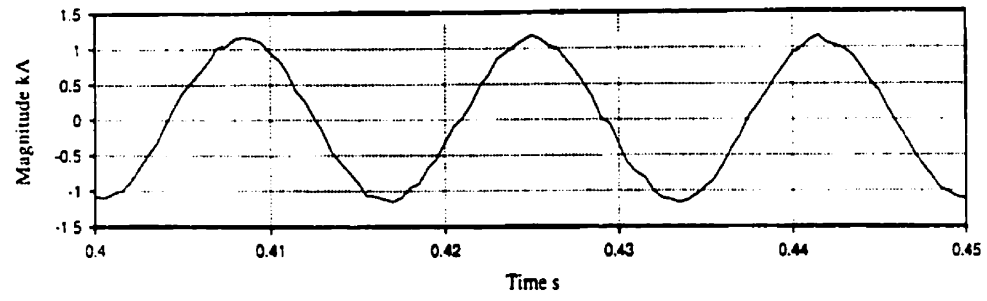
V_{dc} = 11 kV

L = 0.013 H

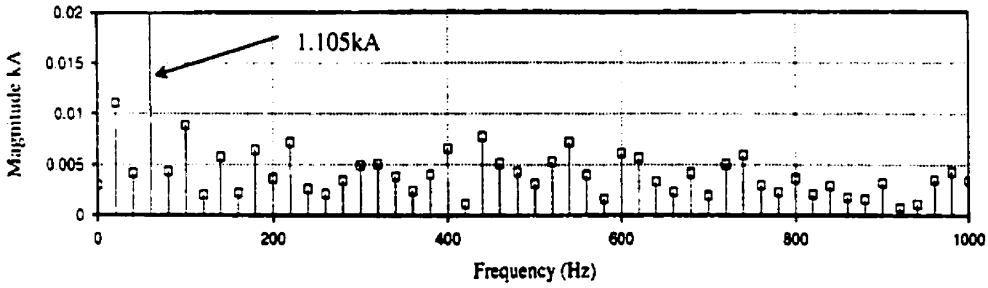
C = 60 μF.

The THDs are listed in Table 3.4.

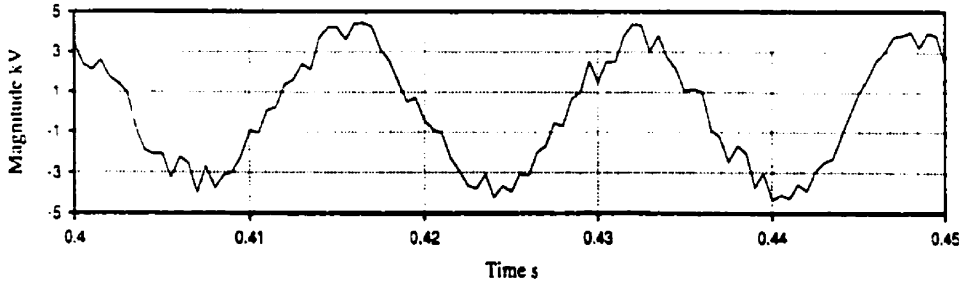
The rest tests are based on V_{dc} = 10kV and 11 kV. Their results are listed in Table 3.3 for V_{dc} = 10kV (Figs.3.17 through 3.20) and Table 3.4 for V_{dc} = 11kV (Figs.3.21 through 3.24). The applicable combinations of the parameters are highlighted using dark rows in Table 3.3 with the relative charts drawn in Figs.3.18 and 3.20 and in Table 3.4 with the corresponding results shown in Figs.3.22 through 3.24.



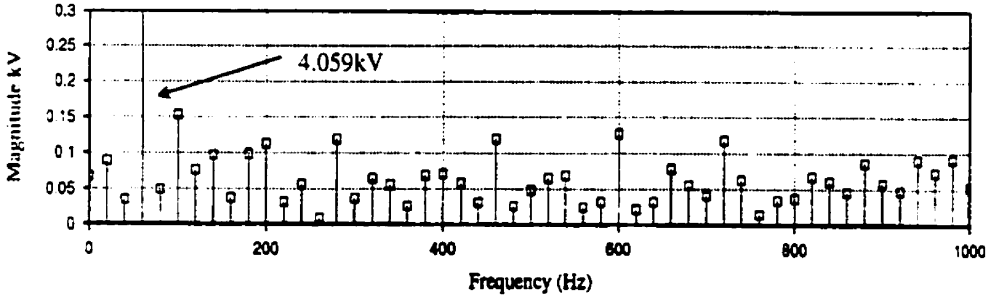
(a) Sample current waveform



(b) Fourier analysis of (a)

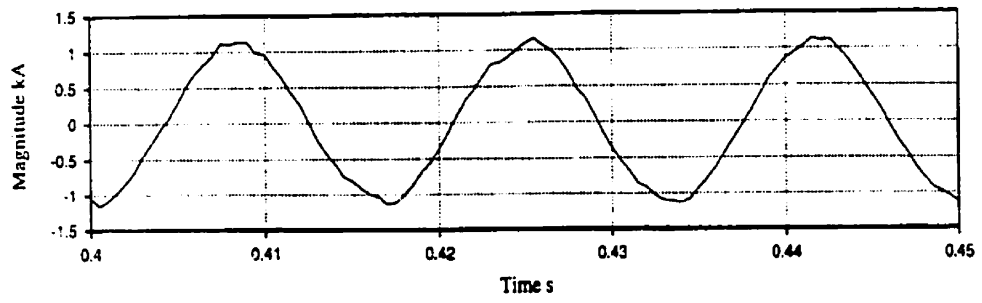


(c) Sample voltage waveform

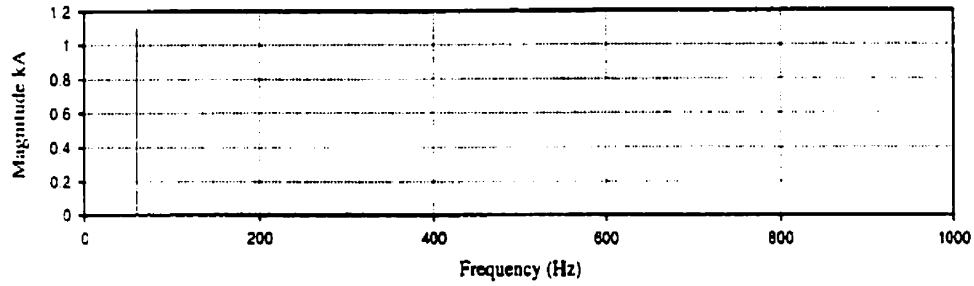


(d) Fourier analysis of (c)

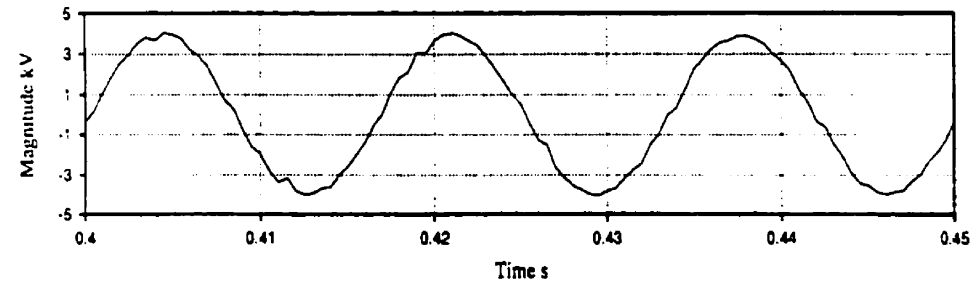
Figure 3.15. Fourier analysis for improper series filter setting



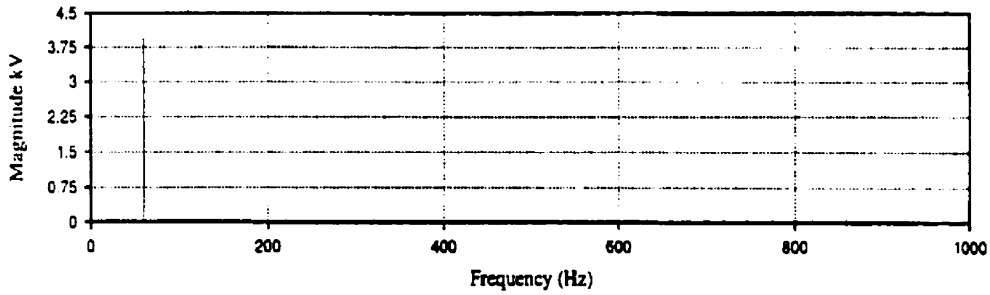
(a) Sample current waveform



(b) Fourier analysis of (a)



(c) Sample voltage waveform



(d) Fourier analysis of (c)

Figure 3.16. Fourier analysis for improved setting

Table 3.3 Test results for V_{dc} = 10kV

Inductance (H)	Capacitance (μF)	THD of i_{ca}	THD of i_{cb}	THD of i_{cc}	THD of i_{ca}	THD of i_{ca}	THD of i_{ca}
0.008	40	3.6239	3.7433	2.6822	7.3951	7.5132	6.8048
	60	3.7434	3.9098	2.7896	5.8107	7.6542	8.0703
	80	3.7017	4.1857	3.1192	6.7598	8.7252	8.3081
	100	4.1784	4.7313	3.3719	5.3043	6.634	6.1583
	120	3.8975	4.3775	3.0665	5.0912	5.9851	5.8875
0.01	40	4.0725	4.1204	2.7298	5.4186	6.1094	6.9132
	60	4.2509	4.3159	2.7401	5.0160	5.2753	5.2414
	80	4.5595	4.1175	3.2482	5.9979	5.9292	6.4589
	100	4.8305	4.4690	3.2235	5.5959	5.2052	5.5652
	120	4.5669	4.5447	3.6688	4.0273	4.2621	4.6097
0.012	40	4.1209	4.5576	3.0410	5.7947	4.8938	5.5068
	60	4.8847	5.3318	3.7293	4.6725	3.8530	5.2199
	80	5.2576	5.4352	4.3193	4.0951	4.8135	5.2335
	100	5.4927	6.5718	5.5452	4.7653	4.4854	5.0841
	120	5.6821	5.9612	4.5432	4.1251	4.7711	4.8248
0.014	40	4.7094	4.6327	3.9391	4.6859	3.7203	4.6074
	60	6.7519	6.0240	4.9553	4.6962	3.6362	3.8456
	80	6.6071	6.8752	5.2458	4.6642	3.3654	4.5199
	100	6.5015	6.5094	5.2986	3.3554	3.4285	3.9995
	120	6.8296	7.5654	5.3597	3.3097	3.8350	3.9539

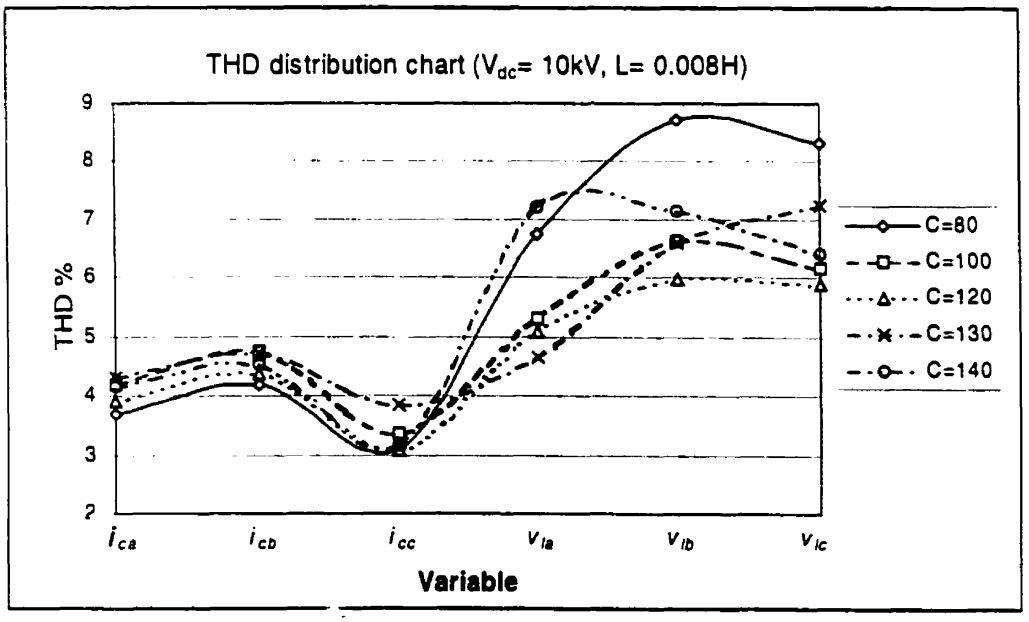


Figure 3.17. THD for test result 9

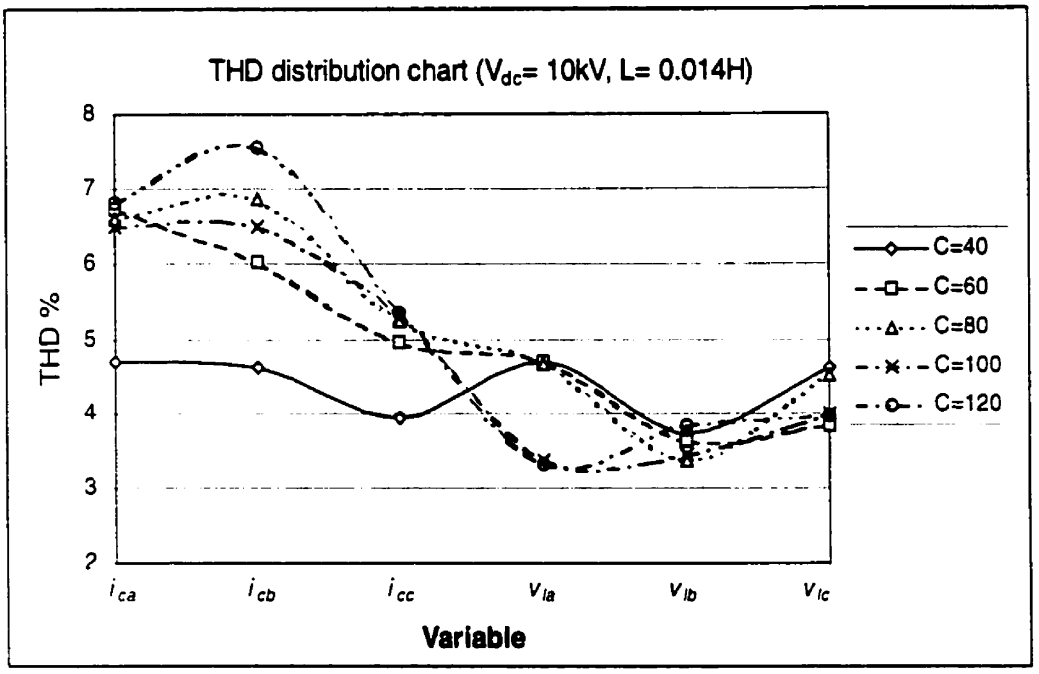


Figure 3.18. THD for test result 10

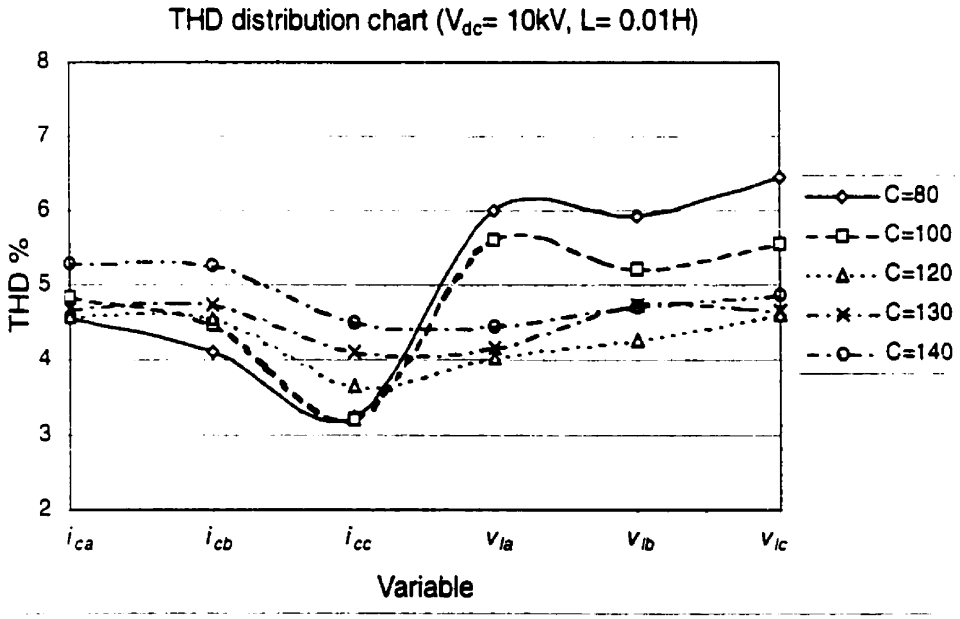


Figure 3.19. THD for test result 11

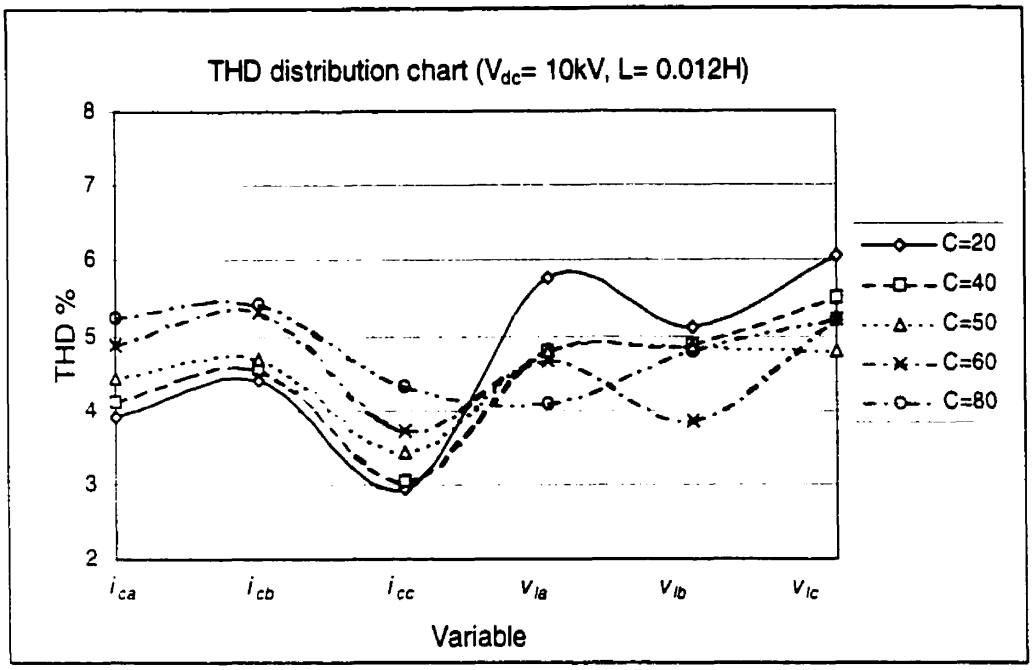


Figure 3.20. THD for test result 12

Table 3.4 Test results for V_{dc} = 11kV

Inductance (H)	Capacitance (μF)	THD of i_{ca}	THD of i_{cb}	THD of i_{ca}	THD of i_{ca}	THD of i_{ca}	THD of i_{ca}
0.009	60	3.6356	4.0791	2.4700	7.1911	7.7113	7.5082
	80	3.7748	4.3637	2.997	6.4523	6.6777	5.9652
	100	3.4773	4.2590	2.7524	7.0683	7.1051	6.1493
	120	4.1712	4.1136	3.4214	6.7690	6.9766	6.9129
	140	3.6914	4.3025	2.9347	5.4095	6.2770	6.6307
0.011	60	3.9207	4.0767	2.7042	5.2839	5.4146	5.9548
	80	4.2351	4.3769	3.0469	4.7278	5.2141	5.1497
	100	4.2601	4.7555	3.2298	3.5140	4.8976	4.5891
	120	4.6802	4.8147	3.4687	4.632	5.9996	5.7766
	140	4.8888	4.8297	3.0368	4.7291	5.6138	6.5216
0.013	60	4.6631	4.3986	3.9459	4.7968	4.6079	4.5320
	80	4.5191	4.8178	3.5965	4.363	4.3794	4.3832
	100	5.1948	5.1615	3.6374	4.3934	5.1165	5.2808
	120	4.7057	5.2415	4.5613	4.2189	3.9701	4.2841
	140	5.9232	5.4090	4.3487	3.6426	3.4085	4.2544
0.015	20	4.2130	4.8109	2.5551	5.2022	5.3125	6.7218
	40	4.5342	4.6049	2.9419	4.7513	4.2869	4.9406
	60	4.8264	5.4019	3.5709	4.2006	4.0432	4.3935
	80	5.5362	6.0956	4.8340	4.2968	4.8033	4.2283
	100	6.4682	5.6377	3.8818	3.3147	4.1511	4.0622

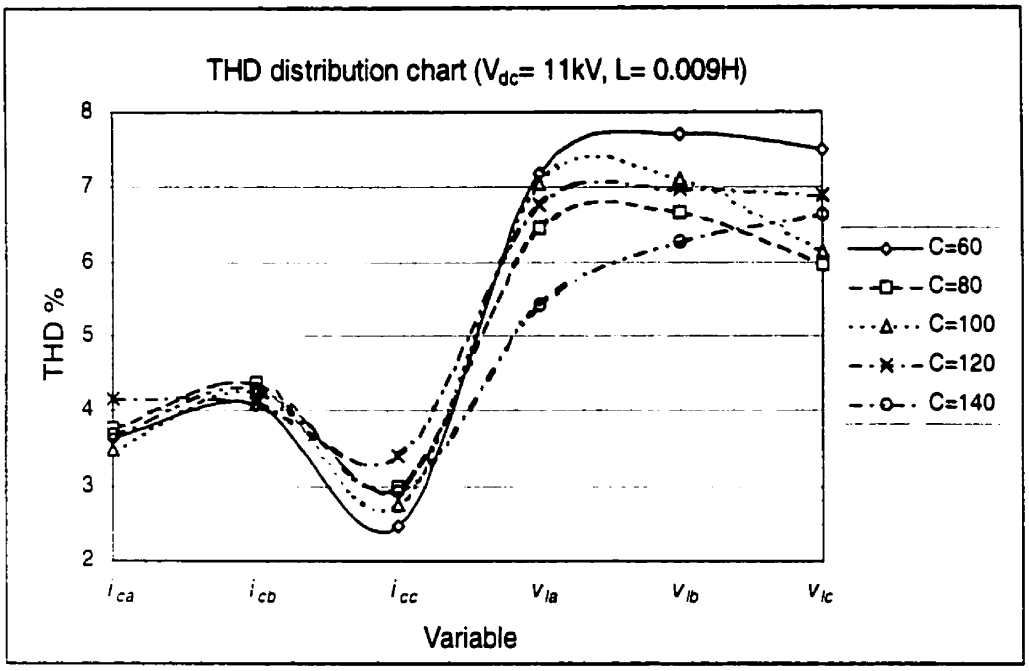


Figure 3.21. THD for test result 13

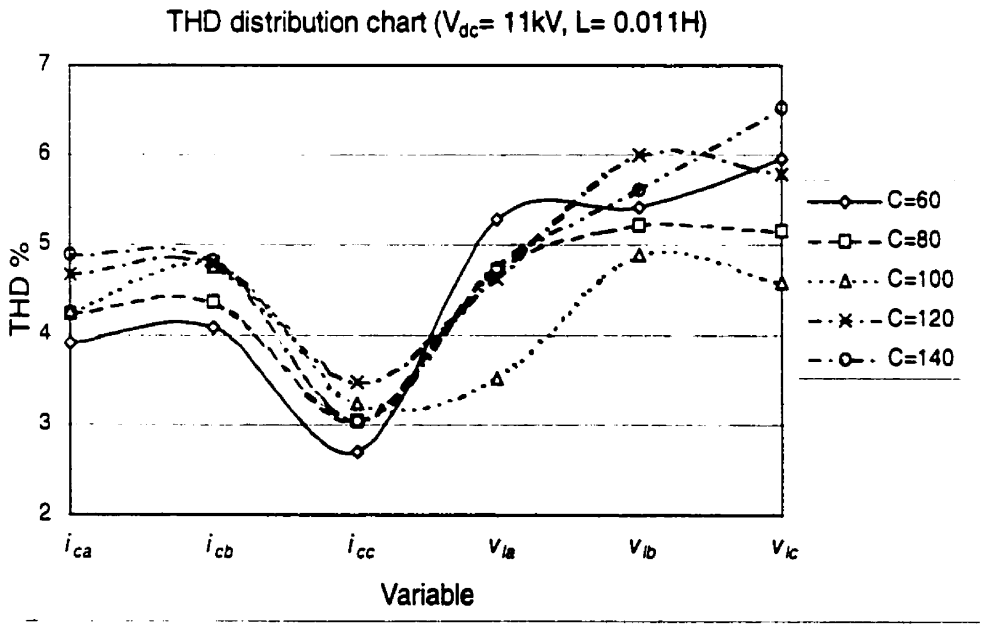


Figure 3.22. THD for test result 14

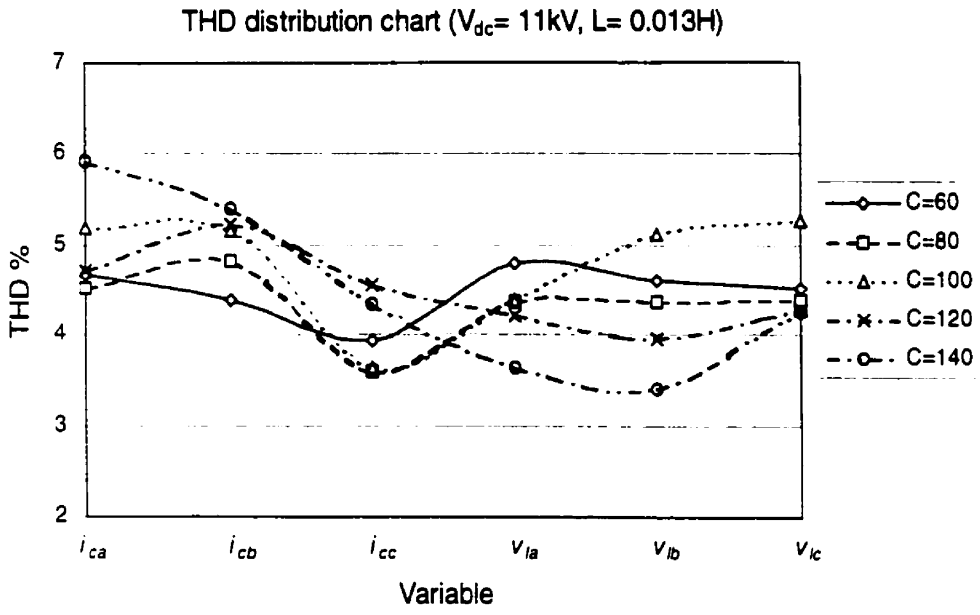


Figure 3.23. THD for test result 15

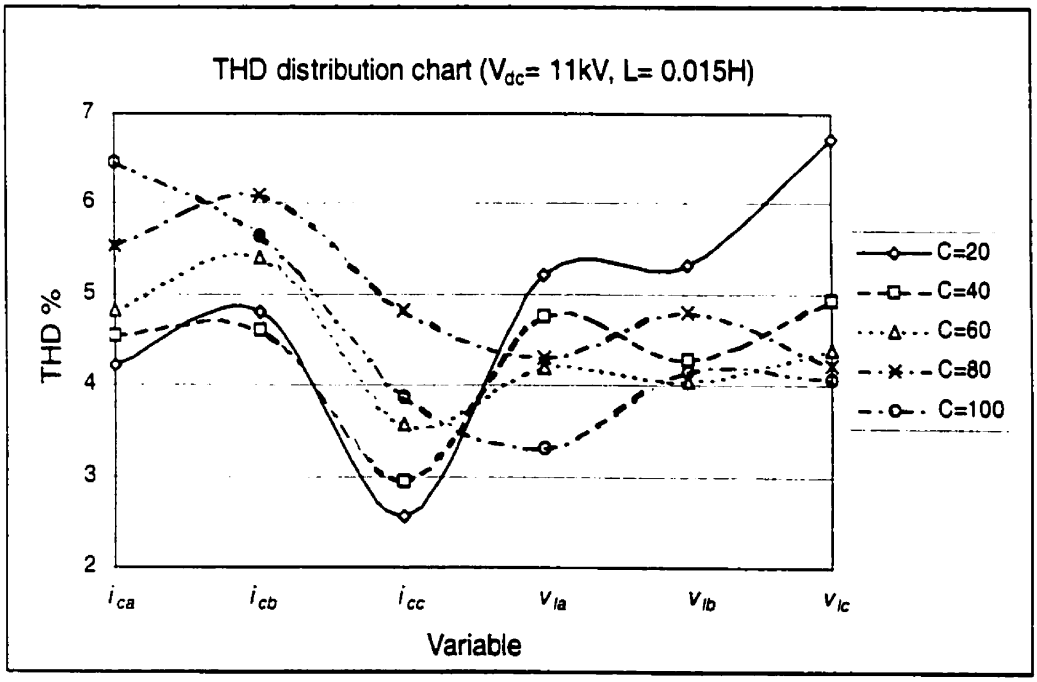


Figure 3.24. THD for test result 16

CHAPTER 4

SSPC SIMULATION STUDIES

A number of studies have been performed on the system shown in Fig. 3.1 and with the specifications described in Chapter 3. Results of these studies are given below.

4.1 Var Compensation for Different Loads

The electrical power distribution system is that portion of the electrical system that connects the individual customer to the power source.

Loads are the reason for the electrical power system. The types of loads are: resistive, such as lighting and heating; inductive, such as motor loads; and capacitive, such as rectifier bridges with capacitor filters. Most electrical system loads are predominantly inductive. The SSPC must be suitable for these loads.

For a system with PF = 0.8 (lagging) before compensation, the relationship among the load current of phase a, i_{la}, source current of phase a, i_{sa}, and load voltage of phase a, v_{la}, is shown in Fig. 4.1. The load current and source current are in phase, and they are lagging the phase voltage. To correct the PF, an SSPC is put in use. The result of this compensation is shown in Fig. 4.2. The simulation results displayed in Figs.4.2 through 4.5 for the four load settings listed in Table 4.1 show that the power factor as viewed from the source can be corrected up to unity under various load conditions.

Table 4.1 Power factor improvement with SSPC

TEST NUMBER	PF BEFORE COMPENSATION	PF AFTER COMPENSATION
1	0.8 (lagging)	0.999 (lagging)
2	0.7 (lagging)	0.998 (lagging)
3	0.8 (leading)	0.999 (lagging)
4	0.7 (leading)	0.999 (lagging)

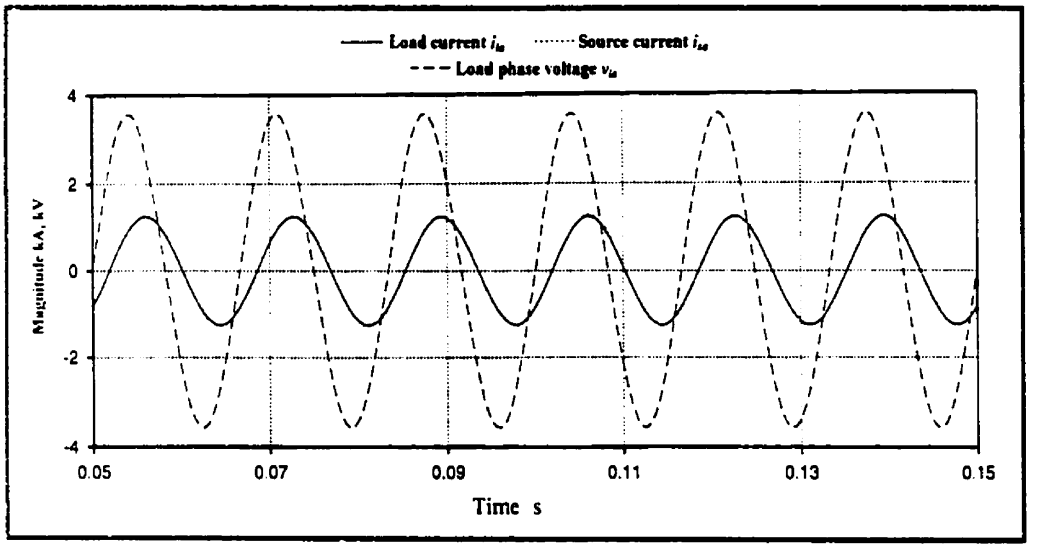


Figure 4.1. Outputs before compensation

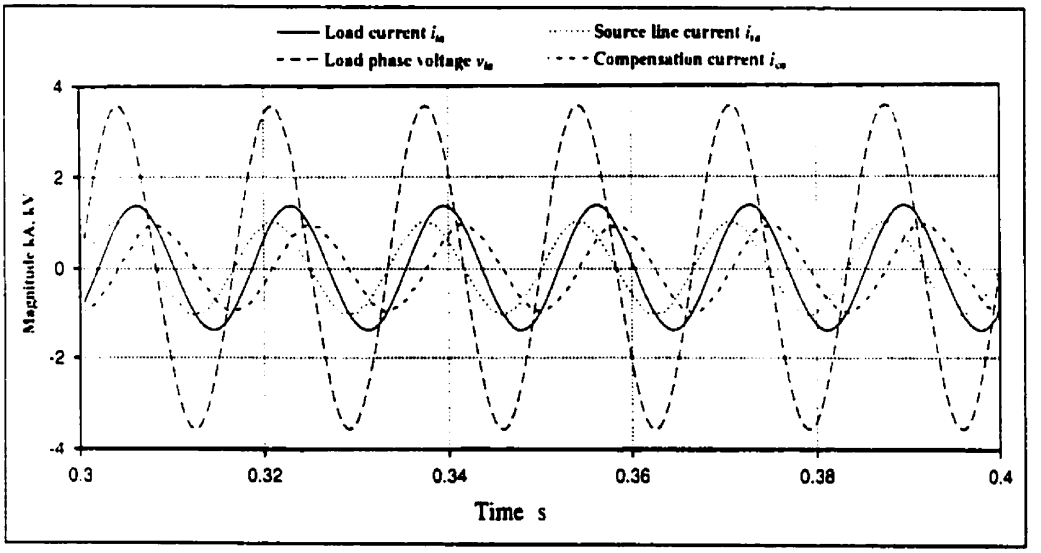


Figure 4.2. Outputs after compensation (Test 1)

4.2 Three-phase Compensation of Unbalanced Load

In practice, it is necessary to compensate the var flow in a system with unbalanced loads. For example, Residential loads are the combined loads of single family dwellings and apartment complexes. Most dwelling units are single-phase although most apartment complexes have three-phase service and the load to each phase is balanced among the apartment units. Obviously it is not possible that all the dwelling units draw current in the same manner. Therefore, the three-phases are not balanced all the time. For this reason,

the SSPC should be able to inject unbalanced compensation currents to the individual phases in the system as shown in Fig. 4.6. The compensation current of phase a, i_{ca}, is greater than that in phases b and c, because the load current of phase a, i_{la}, is greater than that in phases b and c. This technique makes the SSPC more flexible and meets the needs of the customers in distribution systems.

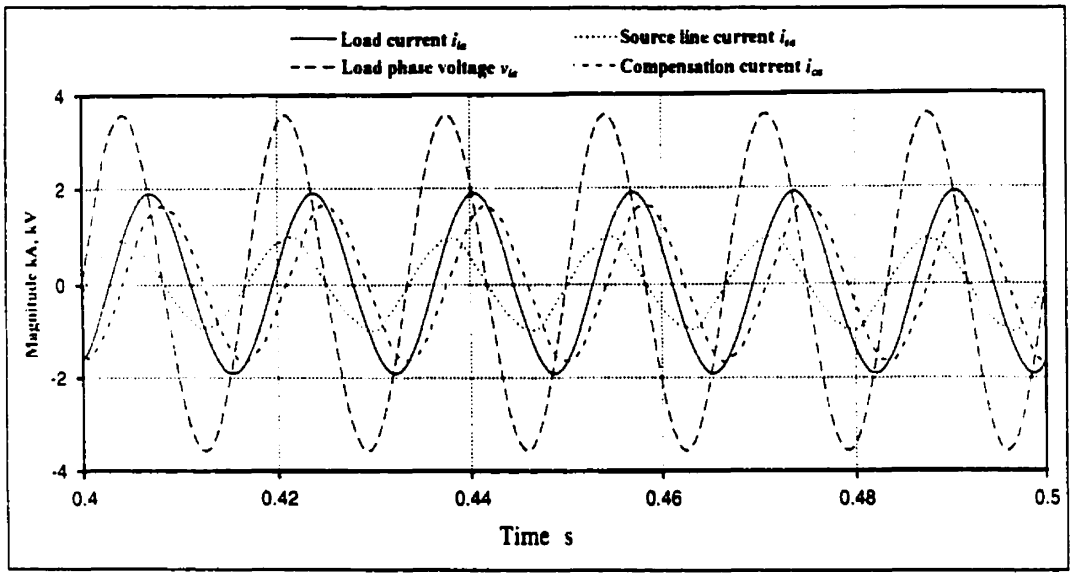


Figure 4.3. Outputs after compensation (Test 2)

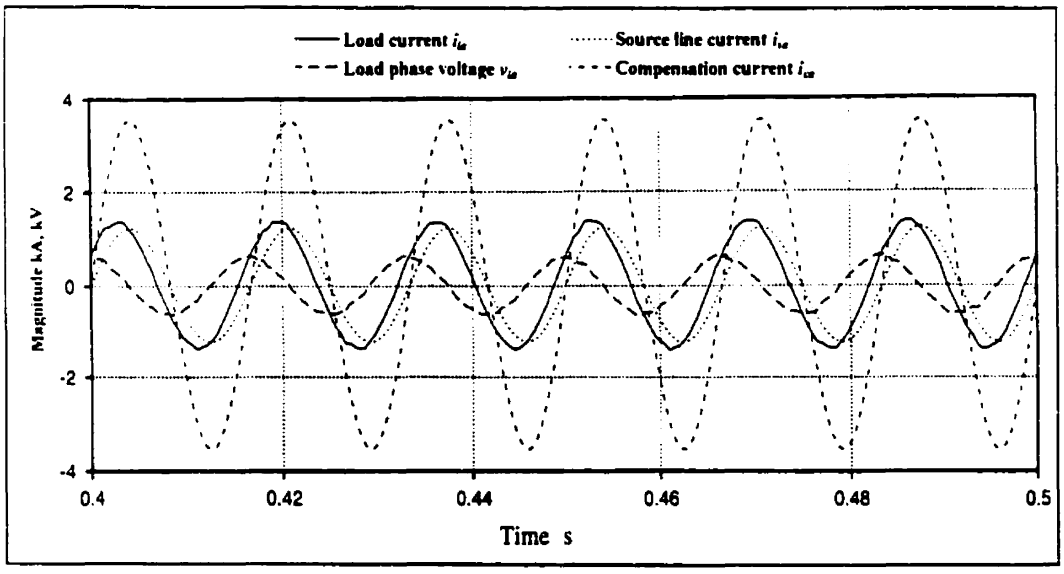


Figure 4.4. Outputs after compensation (Test 3)

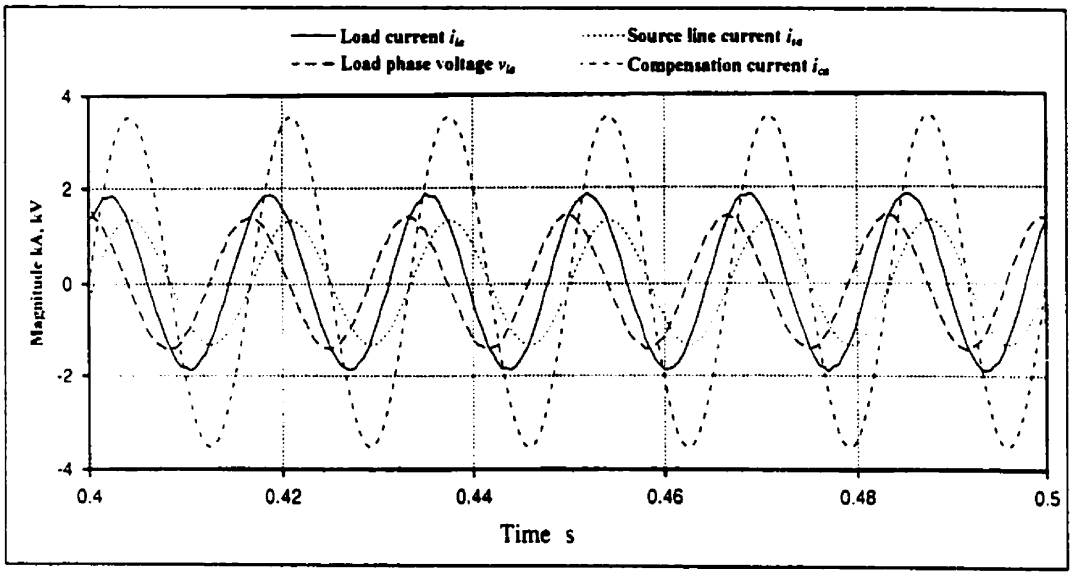


Figure 4.5. Outputs after compensation (Test 4)

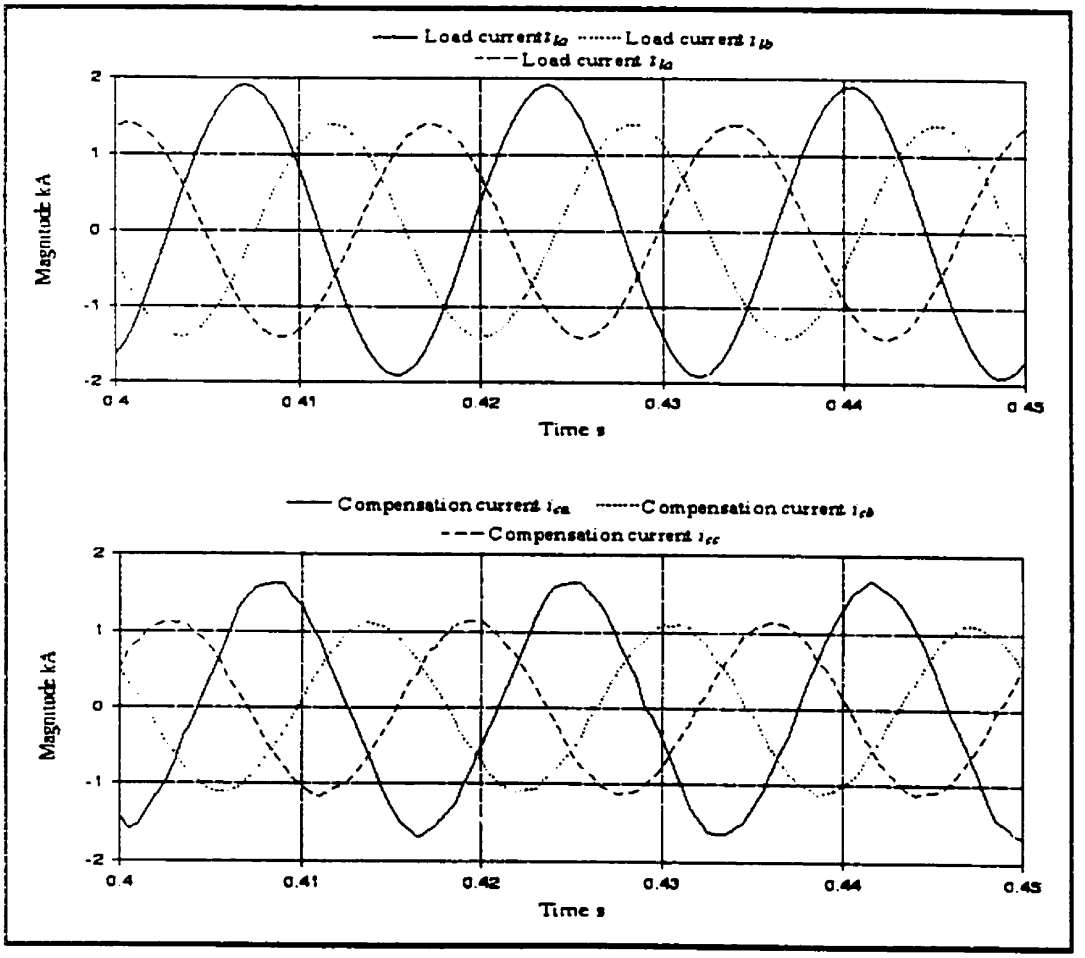


Figure 4.6. Unbalanced load simulation result

4.3 Dynamic Compensation Simulation Results

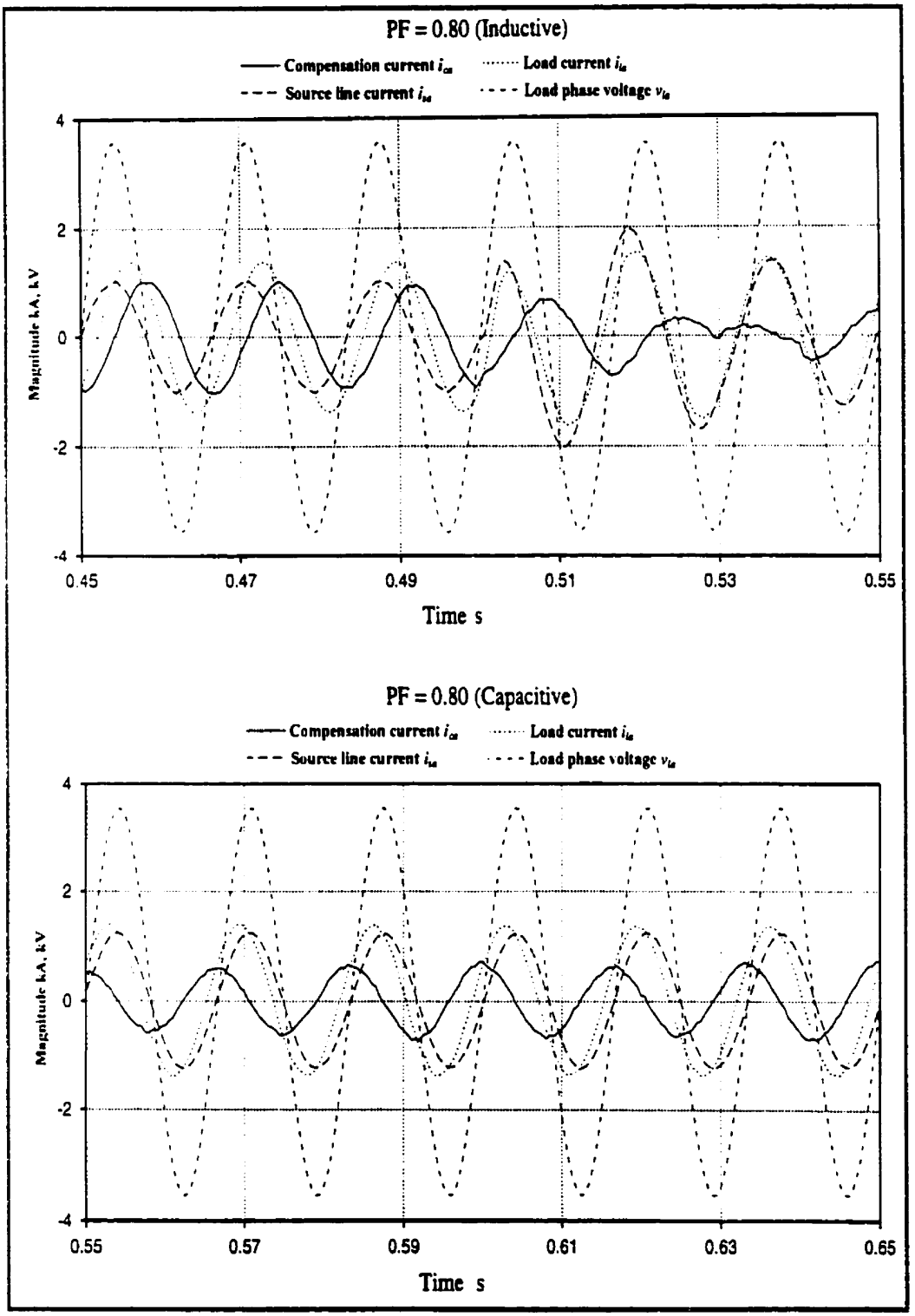


Figure 4.7. Dynamic compensation result

As mentioned in section 1.1, a correction to a unity power factor under one set of operating conditions may result in a leading power factor under different load conditions.

A leading power factor could result in an excessive line voltage increase in many systems (see Appendix B). To operate well at unity power factor, such systems will need automated equipment to control the var compensation as the load changes.

To test dynamic compensation, the system initially had an inductive load. At 0.5s, a capacitive load is switched in and at the same time, the inductive load is disconnected. The system performance is shown in Fig. 4.8. It can be seen that before 0.5s the load current lags the associated voltage, and after 0.5s the load current leads the voltage. However, the source current does not change. It stays almost in phase with the associated voltage, which is achieved by adjusting the compensation current. Moreover, the SSPC can change the compensation currents dynamically, so that "an excessive line voltage increase" can be avoided.

4.4 Analysis

4.4.1 Harmonic distortion

For practical application, the total harmonic distortion must be lower than 5% for the system with the SSPC. To reach this goal, various problems have been tackled at the design stage as described in Chapter 3. For the studies given in section 4.1, Fourier analysis of the 0.8 PF inductive load and 0.8 PF capacitive load has been done using PSCAD [26]. The frequency and phase spectra of the compensation currents and line voltages are shown in Figs.4.9 through 4.11, and the related THDs are listed in Table 4.2, from which it can be seen that the THDs for the waveforms are less than 5%. Therefore, the design can meet the requirement for industry application.

Table 4.2 THD of voltage and current waveforms

FIGURE	THD of phase a	THD of phase b	THD of phase c
4.9	3.6%	4.7%	3.9%
4.10	3.6%	3.1%	3.1%
4.11	1.0%	1.2%	1.1%

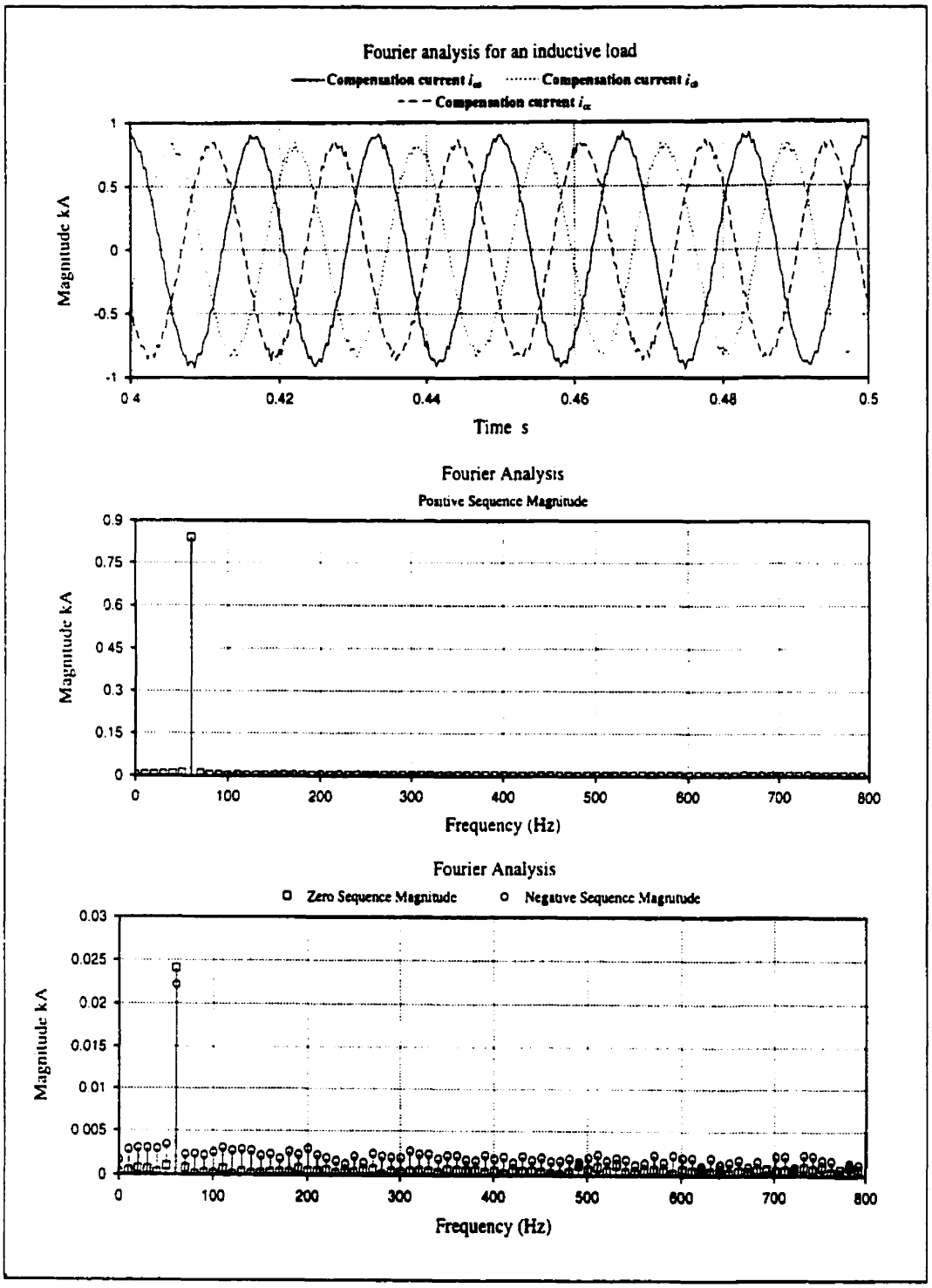


Figure 4.8. Fourier analysis of compensation currents for Test 1

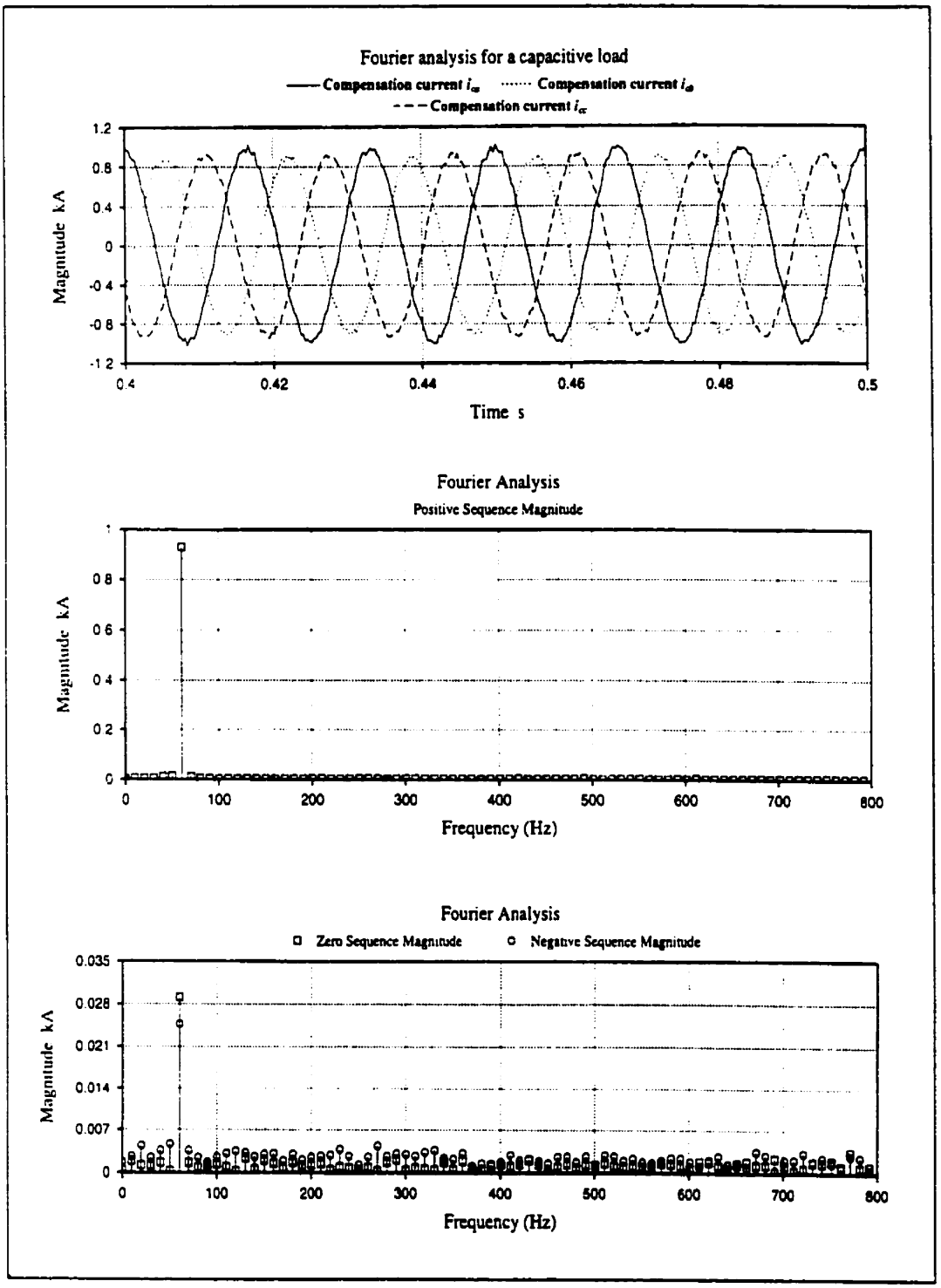


Figure 4.9. Fourier analysis of compensation currents for Test 2

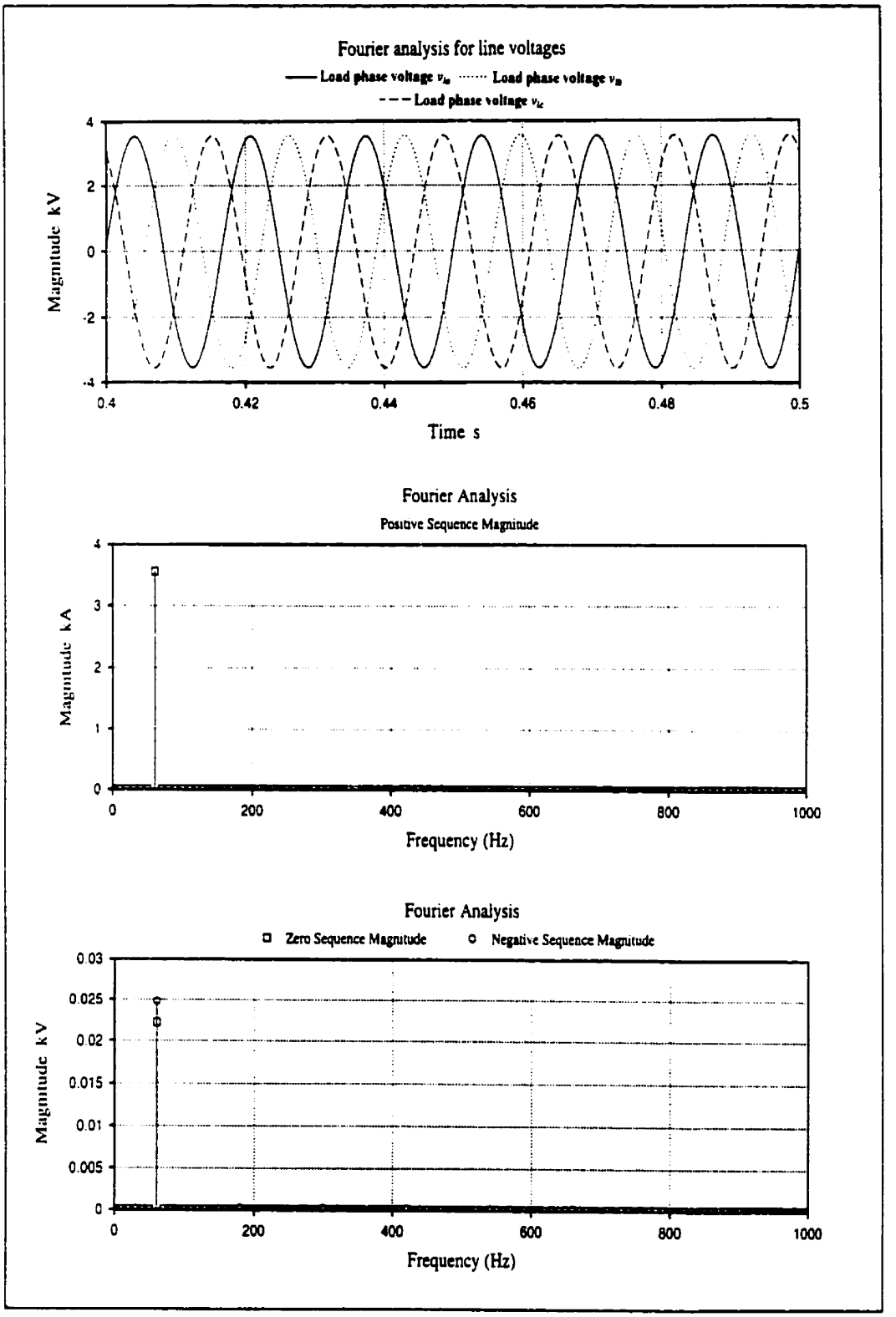


Figure 4.10. Fourier analysis of line voltage for Test 1

CHAPTER 5

CONCLUSIONS AND FUTURE STUDIES

5.1 Conclusions

Excessive var flow can cause extra energy loss and/or significant voltage drop in a power distribution system, and is a matter of concern for power system operators and engineers. Var flow control in transmission and distribution systems can be of immense benefit to electric power utilities in regard to performance. Static power electronic controllers are now making a major impact on var compensation in power systems through applications in transmission, distribution and small generation.

Since the introduction of the FACTS, the power system technology has been moving ahead at an increasing pace. The FACTS is a concept that promotes the use of power electronic controllers to enhance the controllability and usable capacity of ac transmission and covers a large range of advanced equipment for use in power systems. Var compensation devices are one of its main parts. The thyristor controlled series compensator (TCSC), static var compensator (SVC), and static synchronous series compensator (SSSC), are a representative set of devices employed within the FACTS.

The SVC is a good var compensator, which can be employed in either high voltage power systems or distribution systems. Therefore, it is beneficial to the electric companies. However, because it is connected to a system in parallel, its compensation properties are not as good as those of the SSSC, when the line voltage drop is large enough to affect the normal operation. In this case, the SVC is not applicable. Moreover, since the SVC has inductors and capacitors for compensation, the SVC has slower response, larger size and higher cost.

The TCSC has similar drawback to the SVC, that is, it has inductors and capacitors for compensation, therefore, the TCSC has slower response, larger size and higher cost.

The SSSC is an advanced approach in var compensation, as it has quick response, smaller size and a lower capital cost than the SVC or TCSC. It means that it is likely to play an

important role in power systems with long transmission lines. The fundamental principle of its application being line reactance, it is not applicable in distribution systems with short lines.

This dissertation is devoted to the design and development of a static synchronous parallel compensator (SSPC) composed of a current regulated inverter. Contributions have been made to the SSPC design and its simulation investigations.

Devices for building the inverter have been carefully selected. GTO thyristors not only require complex peripheral circuitry to ensure reliable operation but also switch at low frequency. The IGCT is a GTO with improved switching performance, increased gate drive current and lower snubber requirements. Also, its blocking voltage can be as high as 5.5kV. However, its switching frequency is limited to 500Hz by its gate drive power requirement. di/dt limiting inductor losses and the anti-parallel diode switching performance. Therefore, it can not be used for hysteresis-type control. The IGBT has the low conduction loss of a BJT and the switching speed of a MOSFET. It is voltage-driven and suitable for snubberless operation. The switching losses are very low in comparison with GTOs. Recent advancement in IGBT technology has resulted in great performance improvements. Higher voltage, more reliable and lower cost IGBT switches are readily available from various sources, which makes the power device reliable and easy to design into medium-voltage applications. Therefore, the IGBT is recommended for use within the inverter of the SSPC

Several types of inverters are used in practice. Voltage source inverter, current source inverter, and current regulated inverter are a representative set of examples. The voltage source inverter is the most commonly used type of inverter. The input is from a dc voltage source. The ac that it provides on the output side functions as a voltage source, which means that its voltage can be controlled according to technical requirements. In contrast to the voltage source inverter, the current source inverter generally behaves as an adjustable current source on the ac output side. The dc input to this type of inverter behaves as a current source, which is realized using a large inductor.

The current regulated inverters may have a dc voltage source on the input side, but their switching is controlled in such a way that they behave as a constant current source rather than as a constant voltage source on the output (ac) side. The goal of the SSPC is to inject controllable ac currents to compensate var flow in the distribution systems. Therefore, this inverter has been chosen. The inverter is implemented through hysteresis-type control.

The principle of hysteresis-type control is to keep the compensation current as close as possible to its reference current. However, the reference current can be obtained in several ways. The cubic spline algorithm, ideal interpolation and the discrete-Fourier transform to obtain the reference current are compared. Theoretical studies show that the best choice is the DFT method.

One main problem to be tackled in SSPC design is to keep the THD of the compensation current below 5%. Since the compensation currents are generated by high frequency switching, both a series filter and a parallel filter are used to keep both the line voltage and the line current distortion below acceptable level.

To test if the design is reasonable and realizable, simulation studies are performed. The simulation is divided into three parts. Simulation for a single-phase system compensation is used to verify the feasibility of the proposed approach. Design modifications, if any required, are made at this stage. Simulation for a three-phase system compensation is then used to demonstrate the functions of the SSPC, and to verify validity of the proposal. Finally, simulations indicate that dynamic performance is very good.

The main contributions of this dissertation can be summarized as follows:

- A new approach, the SSPC, for var compensation is presented. The SSPC can provide compensation current with variable magnitude and phase angle according to load changes and technical requirement. This new approach can replace the SVC for var compensation in distribution systems, because:

  (a) it deletes the capacitors and inductors for compensation in the SVC, (b) it possesses flexible compensation ability, and (c) it can compensate the power factor

to unity without additional devices.

- The inverter design deviates from the traditional route. In this design, the current regulated inverter is employed and the output is a variable ac current rather than ac voltage. This results in the deletion of a large inductor as a ripple filter.

- A high switching frequency power device is used in the design. Compared with the GTO and IGCT, the IGBT has the primary advantages that it can be operated at high frequency, therefore, reducing the size of the SSPC, and increasing the efficiency of the SSPC.

- A good control strategy, hysteresis-type control, is employed in the controller design, which can make full use of the advantages of the IGBT, and minimizes the THDs of the compensation currents to less than 5%.

5.2 Future Studies

Although the studies of pure solid-state compensators have been made for only a limited number of years, such devices have improved very quickly. To make the approach presented in the thesis suitable for practical application, further study should be done. The following topics are recommended for future research.

- With the development of solid-state devices, more efficient, higher voltage rating devices are expected to be developed in the future. Therefore, a higher voltage, larger power rating compensator has to be designed to meet the increasing requirement of different applications.

- Other switching methods can be used in gate firing, e.g., PWM control having a duty cycle that varies over one period of the mains. In the investigation of current regulated inverter, despite much effort having been made, the THD is still around 4%. Therefore, the controller with PWM control and selective harmonic elimination should be designed to compare with the hysteresis-type control in the future. In addition, it may be possible to have a more systematic design the series and parallel filter components.

- The dc link voltage plays an important role in the compensation current generation. Improper setting of the voltage will affect the quality of the current, which will result in THD increase. Although the THDs of the currents in the simulation studies are below 5% using fixed dc link voltage, it may be possible to improve this design by changing the dc link voltage dynamically according to the load change.

- At the present stage, only software simulation has been carried out. The parameters of the devices used are taken to be ideal. However, there are hidden problems caused by the conditions in the real world applications. Therefore, hardware simulation must be carried out to solve those hidden problems.

- Laboratory testing can be a useful method to verify the feasibility of a proposal, and save time and money. However, there are special problems in industrial applications. The real world test is the final verification of the proposal.

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APPENDIX A

POWER ENERGY SAVING

The principle of SSPC compensation can be described with reference to Figs. A.1 and A.2. The voltage source represents the power source, while the equivalent current source represents SSPC in Fig. A.1. If a certain capacitive or inductive load is connected to the system, V_S can provide current I_l to the load without the SSPC. However, real power is only provided to the load when the SSPC is added, while the reactive power is provided by the SSPC.

The system shown in Fig. 3.1 is used as an example to show the importance of power factor correction from the energy saving point of view.

The parameters of the system are listed below for convenience:

Generator G – 20 MVA, 10kV
Transmission line – 50 kV
Transformer T_1 – 20 MVA, 10kV/50kV
Transformer T_2 – 20 MVA, 50kV/5kV
Load – 18 MVA, 5kV

Suppose the length of the transmission line between T_1 and T_2 is 80 km, and a Hawk conductor with an 5.48 m (18 feet) equilateral spacing is used; load impedance $Z_L = 2.0 + j1.5\ \Omega$.

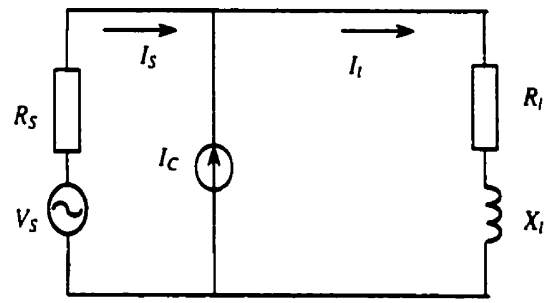

Fig. A 1. One leg equivalent circuit of the system with SSPC

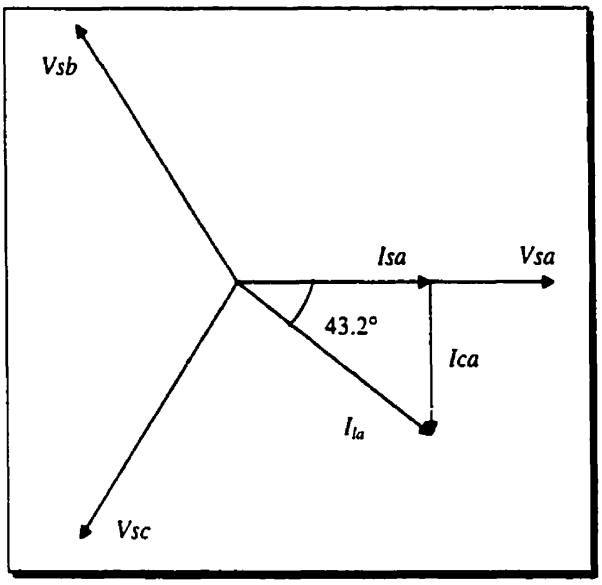

Fig. A 2. Phasor diagram related to Fig. A.1

From the parameter table [26], the related parameters of the transmission line are: $r_l = 0.1325\ \Omega/km$, $x_l = 0.4875\Omega/km$.

To simplify the calculation, ignore the transformer winding resistances and suppose their megnetizing reactances are infinity. Then, the equivalent system circuit can be drawn as in Fig. A.3, where

V_s – secondary voltage of transformer T_1, here $V_s = 50$ kV

I_l – secondary current of transformer T_1

Z_l –line impedance,

Z_L – load impedance,

k – turns ratio of the transformer, here $k = V_1/V_2 = 50kV/5kV = 10$.

The line resistance, reactance and impedance are obtained as follows:

$$R_l = r_l \cdot l = 0.1325 \times 80 = 10.6\ \ \Omega$$

$$X_l = x_l \cdot l = 0.4875 \times 80 = 39\ \ \Omega$$

$$Z_l = R_l + X_l = 10.6 + j39 = 40.42\angle 74.8°$$

In addition, the equivalent load impedance refered to the primary of transformer T_2 can be calculated as:

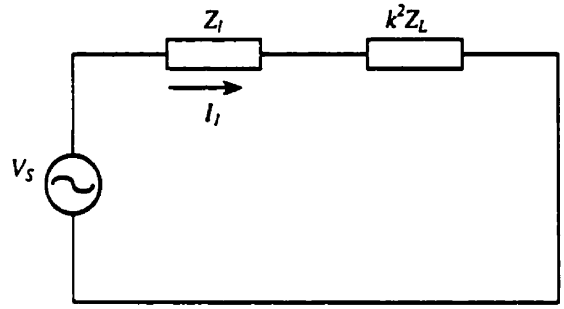

Fig. A 3. Equivalent system circuit for calculation

$$k^2 Z_L = 100 \times (2.0 + j1.5) = 200 + j150 = 250\angle 36.87°$$

The total impedance of the system is:

$$Z = Z_l + Z_L = (10.6 + 200) + j(39 + 150) = 210.6 + j189 = 282.97\angle 41.91°$$

Therefore, the secondary current, I_1, of transformer T_1 can be obtained as:

$$I_1 = \frac{V_S}{\sqrt{3} \cdot Z} = \frac{50 \times 10^3}{\sqrt{3} \times 282.97\angle 41.91°} = 102.2\angle -41.91° \quad A$$

If the power source only provides real power, then the line current is:

$$I_{r1} = I_1 \cos\varphi = 102.2 \times 0.75 = 77 \quad A$$

Therefore, the real power loss can be obtained as:

$$\Delta p = 3 \times (I_1^2 - I_{r1}^2) \cdot R_l = 3 \times (102.2^2 - 77^2) \times 10.6 = 143.4 \quad kW$$

Therefore, a large amount of source current can be reduced by using the SSPC, which can make full use of the generator capacity, save energy wasted in system resistance and benefit customers.

APPENDIX B

EXCCESIVE VOLTAGE RISE

The reason that the voltage at the receiving end rises with a leading power factor is illustrated in Fig. B.1, where

R_S – equivalent secondary resistance,

X_S – equivalent secondary reactance,

R_L – line resistance,

X_L – line reactance,

V_S – secondary voltage of the distribution transformer,

V_R – load voltage.

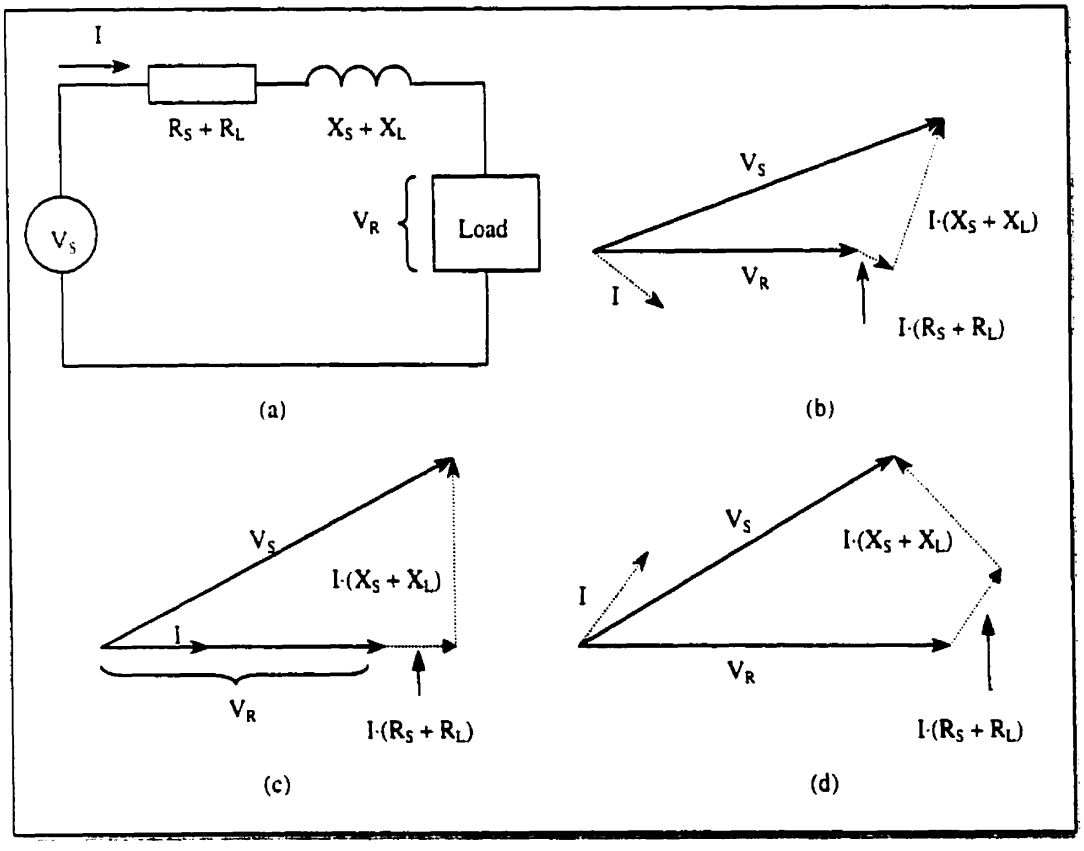

Fig. B 1. Voltage rise with PF < 1 and leading (a) Equivalent circuit of source (b) load PF < 1 and lagging (c) load PF = 1 (d) load PF < 1 and leading

To simplify the analysis, only the secondary winding of a distribution transformer is considered. The secondary resistance and leakage reactance of the transformer, R_S+jX_S, as well as the resistance and reactance, R_L+jX_L, of the line feeding the load are shown in Fig. B.1 (a). Current drawn from the source causes an in phase voltage drop across the resistances and a voltage drop across the reactances that leads the current by 90°, as shown in Fig. B.1 (b). If the source voltage remains constant in magnitude, then as the power factor becomes less lagging and goes into a leading condition, the voltage drops across the reactance and resistance of the transformer secondary and line will rotate the $I\cdot(R_S + R_L)$ phasor as shown in Fig. B.1 (b) and (c). The algebraic sum of the voltages around a closed loop must equal zero so the load voltage will rise, as shown in Fig. B.1 (d).