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A Resonant Synchronous Gate Driver for GaN e-HEMTs

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by

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Abstract

Gallium nitride based enhancement-mode high electron mobility transistors (E-HEMTs) are allowing power converters achieve power densities and efficiencies beyond what has ever been possible with silicon MOSFETs. As E-HEMTs facilitate converters with higher switching frequencies and as unit efficiencies rise, so does the emphasis on having faster and more efficient gate drivers. The conventional totem pole gate driver dissipates the entire gate charge every switching transition, is highly sensitive to parasitic inductance, and has limited control over switching speed. These issues are even greater with E-HEMTs that are capable of switching in under one nanosecond and have much more sensitive gates than silicon MOSFETs. By its very nature, a current source gate driver has control over the rate of change of gate voltage, facilitating faster transitions with lower hard switching losses, and because it is derived from an inductance it has the potential of recovering charge stored in a gate that would otherwise be dissipated. This thesis will introduce and demonstrate the performance of a novel resonant synchronous gate driver applied to a push-pull Class E amplifier for wireless power transfer.

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Dedication

To my mother, father, and sister

Hala Allam, Abdelfattah Youssef, and Ayah Youssef

If you are happy, I am happy

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List of Symbols

ω	Converter's resonant angular frequency, units rad/s
θ	Phase delay
C_{gd}	FET's drain to gate or Miller capacitance
C_{iss}	FET's input capacitance, or equivalent input capacitance
C_{oss}	FET's output capacitance, or equivalent input capacitance
E	Energy, units J
E_{sw}	Switching energy loss
f	Frequency, units Hz
g	Transconductance, units A/V
i	Current, units A
$i^\star$	Optimal gate current
k	Magnetic coupling coefficient
k_d	Ratio of gate resistance to total drive resistance
L	Inductance, units H
p	Power, units W
Q	Symbol for driver FET or charge, or of quality factor $\omega L/R$, or of constant charge.
q	charge, units C
Q_G	Total equivalent gate charge during the on-state

Q_g Total gate charge during the on-state

Q_{sw} Total gate charge associated with current and voltage transitions

Q_{th} Gate charge at V_{th}

Q_{tr} Gate charge inducted by a drain transient

R Resistance, units Ω

R_D A FET's equivalent off-state resistance

R_g Gate resistance

R_{dr} Drive resistance

R_{ds} Enhanced channel resistance

R_{sink} Total drive resistance connecting gate to the source during the turn-off state.

R_{source} Total drive resistance connecting gate to the supply V_{cc} during the turn-on state.

S Symbol for power FET

t Time, units s

t_{ir} Current rise time

t_{vf} Voltage fall time

v Voltage, units volt

V_{cc} Driver supply voltage

v_{dg} Drain to gate voltage

v_{ds} Drain (to source) voltage

$v_{gs,e}$ External gate voltage, observed on the driver side of the gate resistance and inductance

v_{gs} Gate (to source) voltage

V_{pk} Peak gate voltage

V_{th} FET's gate threshold voltage

List of Abbreviations

AlN	Aluminium nitride
BGA	Ball grid array
BJT	Bipolar junction transistor
DPT	Double pulse test
eFET	Enhancement-mode field effect transistor
E-HEMT	Enhancement-mode high electron mobility transistor
EMI	Electro-magnetic interference
FET	Field effect transistor
GaAs	Gallium arsenide
GaN	Gallium nitride
LGA	Land grid array
MOSFET	Metal oxide surface field effect transistor
PCB	Printed circuit board
PWM	Pulse width modulation
RF	Radio frequency
SiC	Silicon carbide
ZCS	Zero current switching
ZVS	Zero voltage switching
ZVDS	Zero voltage derivative switching

Chapter 1

Introduction

MODERN culture's most ubiquitous technology is the metal oxide field effect transistor or MOSFET. This electronic switch is the primary building block in digital and power devices, and is found in cellphones and laptops, solar inverters and satellites. The power MOSFET has been in commercial production for over forty years and today's state of the art MOSFETs are near the theoretical bound attainable. Incremental, cost-effective improvements in silicon are becoming harder to come by, but gallium nitride is a wide bandgap semiconductor that is rapidly emerging as a substitute. GaN is enabling power converters achieve densities and efficiencies beyond what has been possible with silicon. It is also enhancing the capabilities of today's 5G networks and facilitating the development of new technologies e.g. LiDAR and high power wireless charging [2, 3]. In this Chapter a review of the historical development of the silicon MOSFET, GaN and the high electron mobility transistors or HEMTs is provided. Finally a comparison is made between state of the art silicon MOSFETs and GaN and SiC transistors.

1.1 Historical Context

Silicon became the dominant semiconductor in the second half of the 20th century. Germanium was initially preferred as it has the highest carrier mobility compared to any other elemental semiconductor. Bell Labs lead the research on semiconductors and where William Shockley,

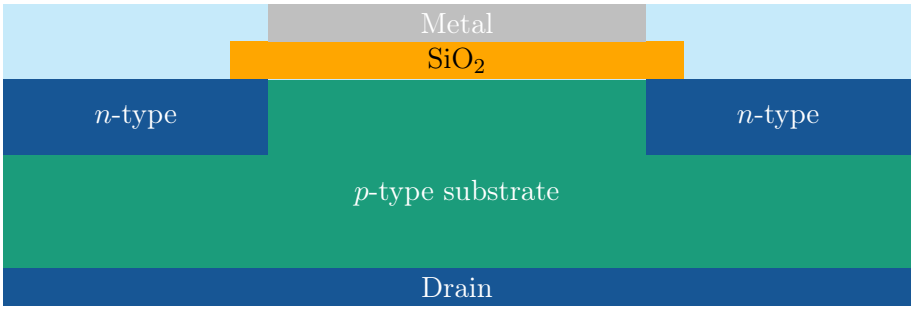


Figure 1.1: Structure of a vertical MOSFET, preferred structure for power applications.

John Bardeen, and Walter Brattain invented the first transistor using germanium in 1947 [4]. In their pure form both silicon and germanium have unstable surfaces which is caused by surface atoms not having complete outer shells. A high surface potential prevents electrical fields from penetrating into the crystal and was the bottleneck in the development of the field effect transistor or FET. The bipolar junction and point contact transistor that Shockley et al. demonstrated in 1947 and 1948 ingenuously avoided the seemingly intractable problem at the surface as the active surfaces are sandwiched between one another [4, 5].

By 1958 a newly hired Egyptian mechanical engineer named Mohammed Atalla capitalized on the advanced fabrication techniques that Bell developed for the diffused bipolar transistor, and solved the surface problem for silicon. He demonstrated the inert properties of its native oxide, silicon dioxide and developed a manufacturing process for the thermal oxidation of silicon where a thin layer of SiO_2 is formed on its surface [4]. SiO_2 proved to be an integral feature of silicon's reliability as a semiconductor as it formed a stable interface with the crystal that was not just electrically insulating, but just as importantly chemically inert with its environment [4]. This was mainly why germanium failed; its oxide was found to be too reactive for reliable performance [5]. Atalla proposed the FET be built from "metal-oxide-silicon" - hence its name - and together with his Korean colleague Dawon Kahng, built the first MOSFET. The MOS revolution as it is known gave rise to the information age and modern power electronics.

1.1.1 Growing GaN

Group III nitrides exhibit intriguing physicochemical properties. Wurtzite GaN is a piezoelectric crystal which gives it a higher elastic stiffness than other compound semiconductors in group III and IV such as GeAs and ZnSe and which makes it more chemically and thermally stable [6, 7]. GaN was first grown on sapphire in 1969 and its band gap energy was discovered to be 3.4eV, three times that of silicon's [6]. Sapphire resisted high temperatures and aggressive reactants used during epitaxy, but contacting crystals with different thermal expansion properties leads to macroscopic defects such as cracks and pits [6].

Much like the bottleneck in the MOSFET, the key to unlocking the power of GaN lied on its surface. Needed techniques in molecular beam epitaxy evolved in the late 1970s allowing for a breakthrough in 1986 where depositing a thin layer of the softer AlN was found to reduce the surface energies between sapphire and GaN [8]. This allowed the reliable seeding of GaN on unmatched substrates free of cracks and with enhanced electrical and luminescent performance. Ideally GaN ought to be grown on a GaN substrate but currently free standing GaN wafers are too expensive compared to the other established substrates until they more readily mass produced which is practically attainable [9]. Commercialization was spurred by the intense development that occurred in the race to produce blue and white LEDs which facilitated its development into RF applications [7, 10].

1.1.2 The High Electron Mobility Transistor

Silicon is unique in that it is the only semiconductor to be fortunate enough to have a highly reliable native oxide that is used together with a n-doped channel to control drain-source conduction. Other semiconductors must resort to other techniques to induce the field effect, and one way in doing so is by creating a heterojunction, which is a junction between different semiconductors - similar to the original bipolar junction transistor - except a BJT is a minority carrier device. Takashi Mimura invented the high electron mobility transistor or HEMT in 1979, intended as a device for microwave applications [12]. Mimura realized that contacting semiconductor with different band gaps causes a discontinuity in conduction and

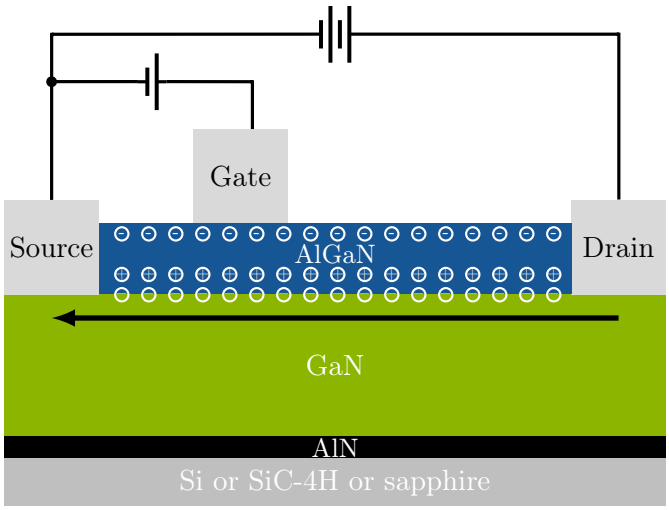


Figure 1.2: Structure of a GaN/AlGaN enhancement-mode high electron mobility transistor or E-HEMT. Applying a positive voltage between gate and source enhances the channel, which can also be done by applying a positive voltage between the drain and gate i.e. negative voltage between drain and source. Adapted from [11].

valence bands at the surface. Band bending occurs because of the difference in band gap energies, and a ultra-low resistance two dimensional conductive electron channel (2deg) is created [13]. The first GaN/AlGaN HEMT was fabricated and characterized, and had the added feature over GaAs/AlGaAs that Mimura used, in that it is naturally polarized and does not require doping [14]. The polarization between the crystals is caused by both the piezoelectric effect caused by the strained AlGaN as well as the difference in spontaneous polarization between AlGaN and GaN [13]. GaN was proven to have excellent semiconductor properties for next generation high- frequency, power, bandwidth and linearity applications; the former two properties being particularly important for power applications where they operate as on/off switches, and the latter for RF application where they are operate linearly [7]. Table I displays some semiconductor properties for silicon, GaN and silicon carbide, the latter which is another attractive wideband gap semiconductor [15, 16]. SiC has a higher thermal conductivity and melting point which also makes it an excellent choice for power applications. SiC's excellent thermal conductivity is similar to copper's at low temperature, which is three times higher than GaN's. However at temperatures greater than 150K this difference is reduced to only 60-70% [17].

Property	units	GaN	Si	SiC-4H
Band gap energy	eV	3.4	1.12	3.2
Breakdown voltage	MV/cm	3.3	0.3	3.5
Saturated drift velocity	$10^7 \times cm^2/s$	2.5	1	2
Electron mobility	cm^2/Vs	990-2,000	1,500	650
Thermal conductivity	$W/cm \cdot K$	1.3	1.5	3.8

Table I: Primary semiconductor properties of GaN, silicon and silicon carbide. Adapted from [11].

The first GaN HEMT was commercialized by Eudyna Corporation in Japan in 2004 [11]. It was a depletion mode (normally off) device and was grown on a SiC substrate. Other companies joined Eudyna and GaN made an impression in the RF industry. Depletion mode devices however require negative voltage for turn off which is not an attractive property for power switches. In 2009 EPC introduced the first GaN on silicon enhancement-mode (normally on) HEMT or e-HEMT intended as replacements for n-channel MOSFETs, thereby taking advantage of the mature silicon wafer industry that is already developed [11]. Soon after many other countries joined to produce e-HEMTs on silicon for the power industry including GaN Systems based in Ottowa, ON.

1.2 GaN e-HEMT

GaN has a higher band gap energy, breakdown voltage, electron mobility and drift velocity than silicon as shown in Table I. A higher breakdown voltage means that a semiconductor can resist a higher voltage per unit length across it, and so it can be miniaturized for high frequency switching. A higher carrier mobility means it will have lower conduction losses. While it can resist higher temperatures, GaN has a relatively low thermal conductivity that is not facilitated by being grown on a non-native substrate and the small packaging required for high frequency switching. Therefore heat loss management has to be a priority in power applications. Furthermore, being a superior amplifying device means that GaN HEMTs are

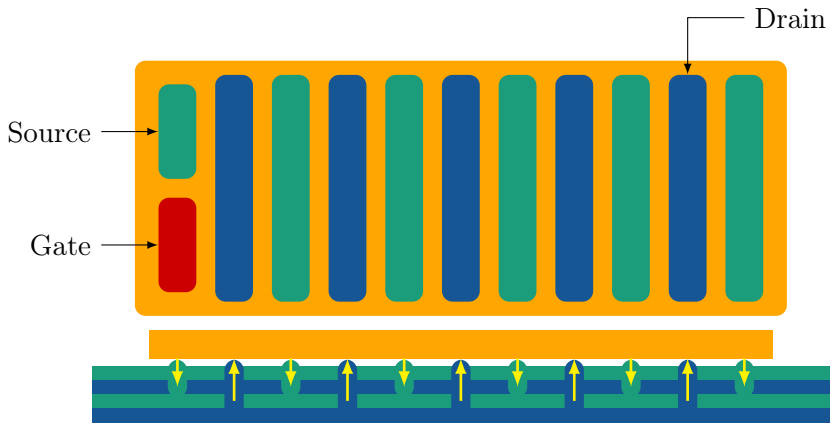


Figure 1.3: LGA package template of GaN E-HEMT by EPC. Alternating the PCB layers between source and drain increases the exposure of reverse currents causing the magnetic fields generated to cancel out while also sinking heat into the PCB.

	[pH]			[mΩ]		
	L_g	L_d	L_s	R_g	R_d	R_s
So-8	2,060	480	830	9.44	0.13	0.96
LFPAK	1,640	100	540	0.73	0.10	0.14
DirectFET	90	440	90	0.22	0.39	0.23
GaN LGA	70	70	80	0.12	0.09	0.10

Table II: Estimates of package inductance at 1MHz [1].

more susceptible to self-sustained oscillation, which is associated with the power density of the device relative to its parasitic tank, including input and output parasitic capacitance and terminal inductance [18]. And so while wide band gap devices show a promising future for enhanced switching performance, their integration must exhibit minimal parasitic inductance and capacitance to tap their properties. Compared to MOSFETs GaN E-HEMTs have:

1. Lower on resistance, which means lower conductance losses.
2. Less package parasitics, allowing for faster transitions and lower switching losses.
3. No reverse recovery charge, enabling efficient and high frequency switching.

1.2.1 Figure of merit and parasitic inductance

A FET is often judged with its figure of merit (FOM) which is a product of on resistance, which reflects its conduction efficiency, and gate charge, which reflects its switching efficiency, given a certain maximum voltage. Figure 1.4 is a plot of some current E-HEMTs together with today's best silicon and silicon carbide MOSFETs. Parasitic inductance exhibited by the packaging and layout of these devices, which can be considerable, is not part of the comparison. Power MOSFETs have a vertical structure to stack a high charge density and breakdown voltage but this comes at the cost of wire bond surface-mount terminals that exhibit parasitic inductance as well as an increased gate charge that curtails high frequency performance [19, 11]. On the other hand HEMTs are lateral devices with a planar structure and so its power density is function of its die area. Such a design is critical for efficient, high frequency operation as the upper bound of frequency performance is inversely proportional to capacitance of a FET [7]. Therefore HEMTs exhibit much less parasitic inductance and capacitance than vertical power devices. Parasitic gate loop inductance is especially concerning for E-HEMTs as there is much small margin between the gate's maximum voltage and the enhancement or turn-on voltage. Drain inductance can be minimized by interleaving source and drain which reduces the system's overall inductance through magnetic self cancellation as shown in Figure 1.3 [20].

1.2.2 E-HEMT characterization

Models, parameters and tools used to describe the behaviour of MOSFETs are used to analyze and describe E-HEMTs and their dynamics [11]. One major difference is that E-HEMTs do not have a body-drain junction that is integral to a power MOSFET's vertical packaging, and which also allows it to conduct in the reverse direction. Having a planar structure avoids the $p-n$ junction and its associated reverse recovery charge which considerably delays transitions from reverse conduction. An E-HEMT can conduct in the reverse conduction in what is called *self commutated reverse conduction*[11] if the gate to drain voltage is sufficiently positive i.e. if drain to source voltage is negative. The source

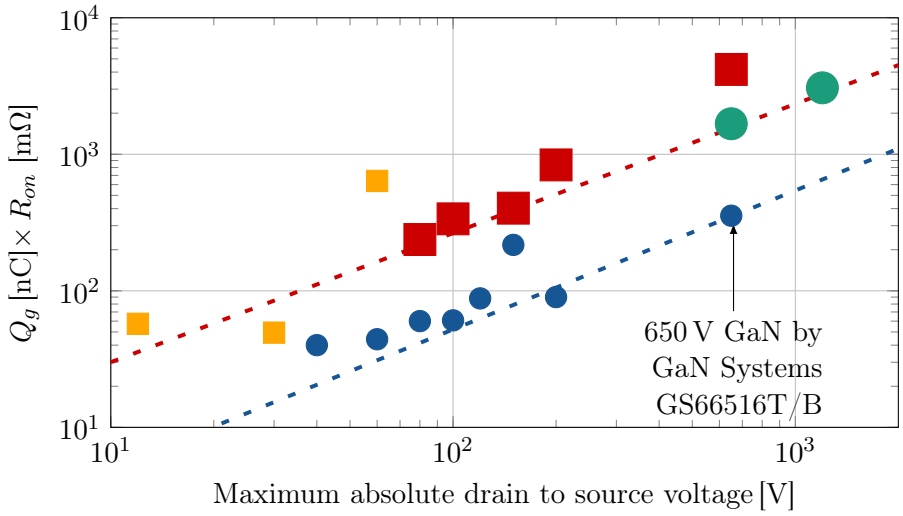


Figure 1.4: FOM of today's state of the art silicon and silicon carbide MOSFETs by Infineon and TI as well as E-HEMTs. Displayed MOSFETs include TI femtofets in yellow which are in LGA packages, Infineon OptiMOS and CoolMOS in red as well as Infineon's SiC IMW120R045 that is in green. LV E-HEMTs by EPC and a 650 V by GaN Systems are in blue. Large dots represent leaded packages while small circles leadless packages (either BGA, LGA or GaN pX®).

to drain voltage is on the order of 2 V and much higher than that of silicon and therefore should be minimized [11]. GaN devices also exhibit both lower parasitic capacitance and inductance, have a lower gate resistance and threshold voltage its on resistance is negatively dependant on temperature [11].

1.3 Driving GaN

Switching GaN's FETs on and off at high frequency requires a power supply capable of sourcing and sinking energy into the gate at high speed; this is the job of a gate driver [21]. Gate drivers including the ones used for high frequency GaN HEMTs typically utilize a totem pole driver which is a half-bridge circuit as shown in figure 1.5. Drivers have a fast response and strong input amplification, and they have leadless and small packages to minimize parasitic inductance. The latter is especially important for E-HEMTs that have a maximum gate voltage margin of less than 1.5 V between the recommended enhancement

voltage. Drivers also have a means for maintaining or regulating gate voltage during the steady state periods, and have low power consumption to minimize heat loss to what is a very tight space. Single-chip monolithic GaN solutions have been commercialized as they allow GaN devices to go beyond the limitations of silicon drivers and PCB and package parasitics as shown and explained in Figure 1.6 [22]. Other features of modern high speed gate drive include:

1. *A Bootstrapped supply* to drive FETs with floating sources. This includes a bootstrap diode or synchronized FET and an external capacitor providing a floating power supply as shown in Figure 1.5. The purpose of the diode is to prevent the capacitor from discharging once the switching node voltage increases, thereby allowing a gate driver to be supplied by a floating voltage source [23, 24].
2. *Level shifter*. The digital input signal is referenced to digital ground, but the FET's gate are referenced to power ground or can be floating as highlighted above. Therefore a gate driver needs to be able to decouple and transform the digital signal input.
3. *Dead time* tuning through local analog circuitry for high precision for synchronous switching, which is the time allocated for when both switches are off before a switching transition is to be completed.

1.3.1 Challenges of the totem pole driver

The conventional totem pole gate driver is made up of two switches, a normally on P-channel MOSFET ('pmos') connected in series with a normally off N-channel MOSFET ('nmos'), with the FET's gate connected in between them, and a voltage source connected between the sources of the switches as shown in Figure 1.5. The pmos and nmos gates are typically tied together and connected to a digital interface that includes a level shifter and an further amplification circuitry to cycle power to their gates. The gate driver receives a digital input from a high impedance source which switches the driver's pmos and nmos in a complimentary fashion. When the logic input is high, the pmos is off and the nmos is on, which connects the gate to its source thereby discharging it, which turns off the FET. When the input is

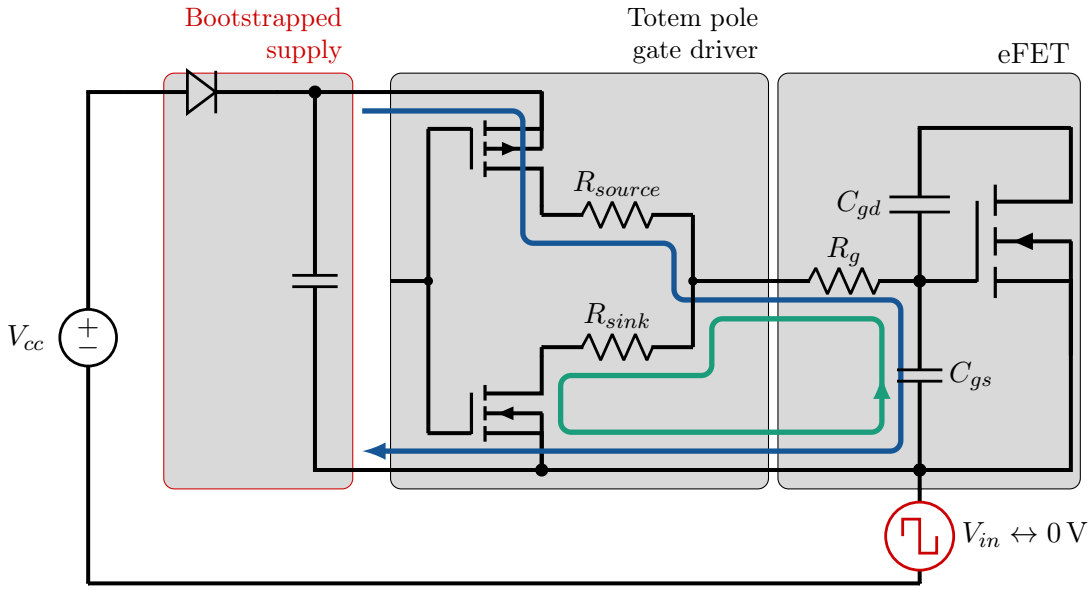
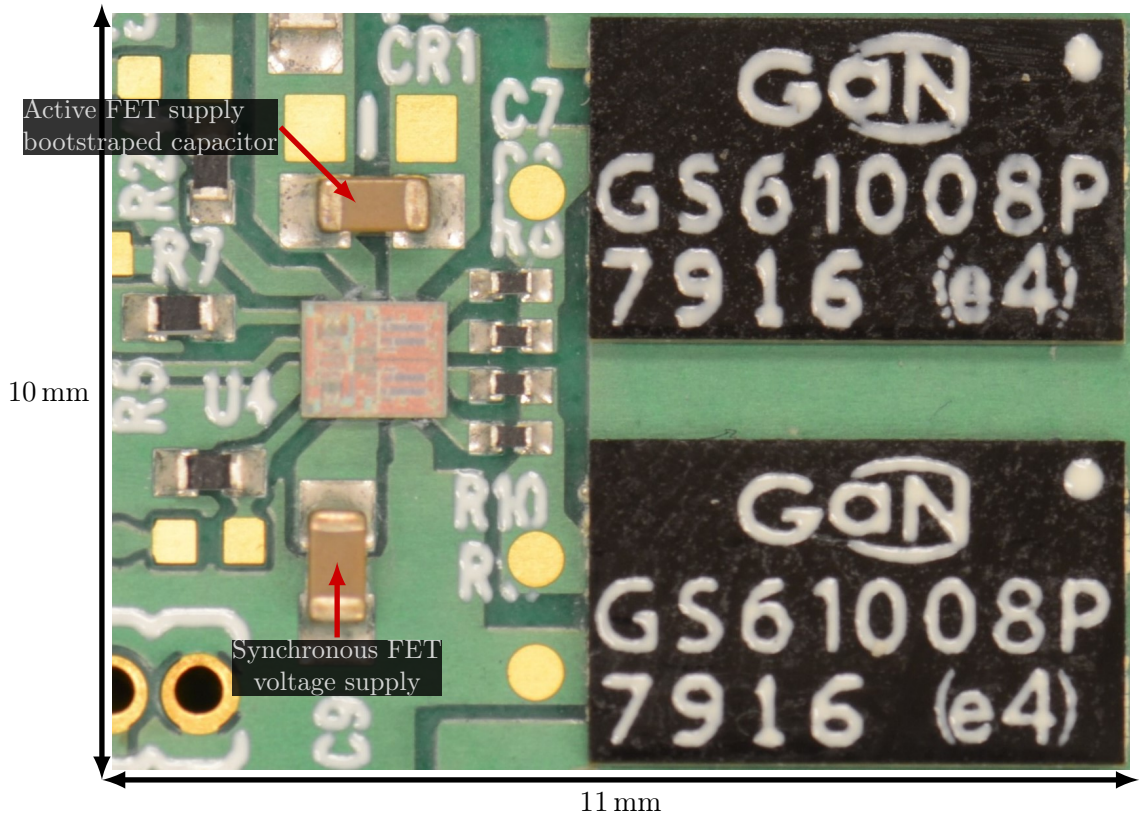


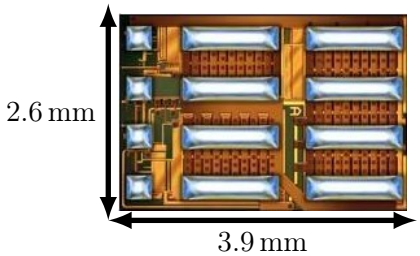
Figure 1.5: A totem pole gate driver source is made up of a half-bridge and can have separate pull-up and pull-down resistors which are also referred to as sourcing and sinking resistors, respectively. These resistors are used to dampen gate ringing as well as to curtail voltage slew rates to suppress gate voltage rise in complimentary switches. A bootstrapped supply can be used to operate the switch with a floating source.

low, the pmos turns on which exposes the gate to V_{cc}, which charges the gate and enhances FET's the channel. Thus the totem pole's output is a square wave with the gate ideally trailing in a first order fashion as per its time constant. Examples of commercial multi-MHz gate drivers for E-HEMT half-bridges are shown in Figure 1.6.

While the totem pole driver remains the topology of the fastest gate drivers, it has several challenges that can curtail the performance of high frequency switching, and particularly of wide bandgap devices. [25] concluded that the primary limiting factors of the totem pole drivers are in its drive resistance, transition times and amplitude of supply voltage. The issues listed below discuss the topological challenges of the totem pole driver and do not consider what the semiconductors the driver's FETs are made from: the situation today is such that we are using silicon to drive GaN. Thus there is a limitation to the switching speed that can be properly demonstrated with existing devices, and it might be better to use larger/slower HEMTs for assessing GaN's performance to make a fair judgement. [26] used GaN HEMTs



(a)



(b)

Figure 1.6: Scaled images of two half-bridges. (a) “Two-chip" design including two 100 V 80 A HEMTs GS61008P by GaN Systems being driven by a synchronous half-bridge gate driver PE29101 by Peregrine Semiconductor. (b) The bottom view of an integrated flip chip EPC2152 by EPC containing both a GaN E-HEMT 80 V, 12.5 A half-bridge as well as their GaN-based drivers. A single-chip and monolithic solution minimizes the gate loop circuit inductance and goes beyond the limitations of silicon. Such a driver will experience high efficiencies, faster switching speeds and shorter propagation delays.

in a totem pole configuration to drive SiC MOSFETs with hard switching at high frequency, and the circuit's operating frequency was limited by the silicon digital isolator and driver that were operating on the GaN driver HEMTs. It was shown that ultimately the performance of GaN HEMTs with the totem pole driver in a hard switching half-bridge topology is curtailed by the gate driver's sinking capability [25]. Therefore, monolithic solutions where GaN FETs GaN FETs such as the one in Figure 1.6 are capable of performing more efficiently at high frequency.

1.3.1.1 Limited speed

The totem pole gate driver is a voltage source gate driver in the sense that the switching dynamics are induced by voltage sources, namely the dc input to the driver and the gate's capacitance. The charging and discharging events transitions are nominally of first order and the gate's ideal or minimally attainable time constant is $R_g C_{iss}$, both of which are properties of the FET, not the driver. The driver's FET's also have an on-resistance that contributes to the time constant, and it may have to be increased to dampen ringing caused by parasitic inductance. Therefore high frequency totem pole drivers need to be compact and near the gates they are operating on, but even at their best they have no leverage on accelerating a switching transition.

1.3.1.2 Gate charge is wasted

During charging, resistance in series with a FET's gate dissipates an equal amount of energy to what would accumulate in it. During discharging, the energy that is stored in the gate is dissipated in the series resistance. The total amount of energy lost in charging and discharging the gate of capacitance C_{iss} from a drive supply voltage V_{cc} is referred to as a gating loss and is given by equation 1.1. All switching losses, including gating losses are directly proportional to the switching frequency of the converter.

$$E_g = C_{iss} V_{cc}^2 \tag{1.1}$$

1.3.1.3 Driver Losses

Gating losses make up about only half of the driver's total losses considering the driver's MOSFETs incur their own losses [27]. This include their own gating losses, channel, and conduction losses, as well as shoot-through losses when both switches are momentarily on simultaneously. Note that the lower the driver's turn on and turn off resistance, the higher the shoot through losses are going to be. Driver losses are proportional to frequency, therefore they need to be minimal for efficient high frequency performance.

1.3.1.4 Dead time synchronization

Given the driver operates on a single switch, its operation needs to be synchronized with other complimentary drivers. Tuning needs to be optimal because on one hand having both FETs on at the same time will cause a shoot-through in synchronous topologies, which damage the FET. On the other hand, having both switches, which is an event called dead time, incurs considerable reverse conduction losses. Single and dual output drivers working in a complimentary fashion can be synchronized digitally by a controller, such as in the EPC2152 shown in Figure 1.6(b), while synchronous drivers are equipped with on-chip circuitry that enables for fine on-board tuning of dead time, e.g. PE29101 shown in Figure 1.6(a).

1.3.1.5 Parasitic inductance

PCB loop as well as component packaging exhibit parasitic inductance that presents challenges to voltage source gate drivers particularly in the source path common to both gate and drain currents [28, 29]. Alongside the FET's parasitic capacitance, inductance introduces resonance that can lead to a voltage overshoot, which is especially problematic for power GaN HEMTs given the low maximum voltage its gates can tolerate. This is why all high frequency drivers are fitted in BGA packages and have extremely tight layouts [30, 31, 32]. Having said that parasitic inductance is not so much an inherent challenge of the totem pole drive as it is a problem of a “two chip" design and integrated solutions such as the one shown in Figure 1.6(b), drastically reduce parasitic inductance allowing for operations with higher

frequencies and lower losses.

1.4 About This Thesis

1.4.1 Thesis Contributions

1. A review of the switching dynamics and challenges of GaN E-HEMTs is provided through sub-circuit analyses utilizing static E-HEMTs parameters.
2. An introduction to current source drive dynamics and advantages are provided, including an expression of optimal gate current with respect to minimizing an E-HEMTs loses including both gate and channel losses in hard switching applications.
3. A novel resonant synchronous gate driver used for complimentary switches is introduced. Its simulation in the application of a push-pull Class E inverter is provided to show reliable switching and the capacity of gate energy recovery.
4. A PCB is designed to test the performance of the proposed gate driver to operate push-pull switches of a Class E inverter that is used in the wireless power transfer of power from a solar PV module.

1.4.2 Thesis Organization

- Chapter One provides a historical overview of the development of the MOSFET and the HEMT, and introduces the challenges of driving GaN devices with the conventional totem pole gate driver.
- Chapter Two describes hard switching dynamics and challenges of high speed switching of E-HEMTs. It also introduces current source gate drives, their advantages and a provides review of some of them.
- Chapter Three introduces and analyzes the operation of the novel resonant synchronous gate driver.
- Chapter Four evaluates the performance of the driver through simulation and optimizes its performance in the application of a push-pull Class E amplifier.

Our interests lie on the dangerous edge of things

The honest thief

The tender murderer

The superstitious atheist

–Robert Browning

Chapter 2

Literature Review

The totem pole push-pull topology remains the primary choice for driving GaN devices. Since the 1990s research began on developing gate drives that incorporate a gate's parasitic capacitance into a resonant circuit. Such a configuration has the capacity to recover energy stored in the gate and offers greater control over the rate of change of gate voltage, enabling faster and more efficient switching transitions. Drivers in general need to be energy efficient, and have the capacity of operating with a wide duty cycle range. Furthermore, they need to utilize low inductance values to be able to be integrated effectively with minimal parasitics. In this Chapter an overview of the latest research into current source gate drivers is provided. First, analyses of an E-HEMT's switching dynamics and losses are provided.

2.1 Switching Dynamics

Switching converters transform electrical power by manipulating power flow through inductors and capacitors using active semiconductor devices. The half-bridge topology, which is used in the totem pole driver, is also used in many switching converters including the buck converter, which is shown in Figure 2.1. During the on-state, the inductor is being charged and load is being supplied by the input voltage source through the active FET, and during

the off-state, the magnetic energy stored in the inductor continues to supply the load through the synchronous FET. Switching of the input current at high frequency leads to an averaging effect through the inductor such that the output has an average dc voltage magnitude that is proportional to the duty cycle of the high-side switch. Therefore, a buck converter is a step-down DC-DC converter.

A FET incurs conduction losses as well as switching losses when transitioning between steady states as illustrated in Figure 2.2, and so the higher the circuit's switching frequency, the proportionally greater are the switching losses going to be [21]. A high switching frequency is desirable because it reduces the required size of reactive components and therefore allows converters to have lower conduction losses, higher power densities, and faster responses to disturbances [33, 34, 35]. Having fast switching transitions is critical in high frequency applications where a FET's channel voltage and current experience a simultaneous transition as illustrated in Figure 2.1 [36, 37]. Switching losses can be avoided by having current and voltage transitions not occurring simultaneously, or not occurring at all, which is called *soft switching*, and its various waveforms are illustrated in Figure 2.3. This is experienced by the synchronous switch in the buck converter that is turned on following the turn-off of the active FET when the switching node voltage is near zero. Therefore it experiences a zero voltage turn on with much lower switching losses.

The switching behaviour of GaN devices has been extensively studied for a variety of converters [38, 39, 40, 41, 42]. [43] provided a comprehensive overview and analysis of a 650 V 30 A E-HEMT and characterized its performance across a range of voltage, current, and temperature conditions. An equivalent circuit of the active FET and the current flows during a turn-on transition is provided in Figure 2.4. The analysis below will describe the hard switching transitions in a half bridge. It does not consider parasitic inductance which will be covered in subsubsection 1.3.1.5.

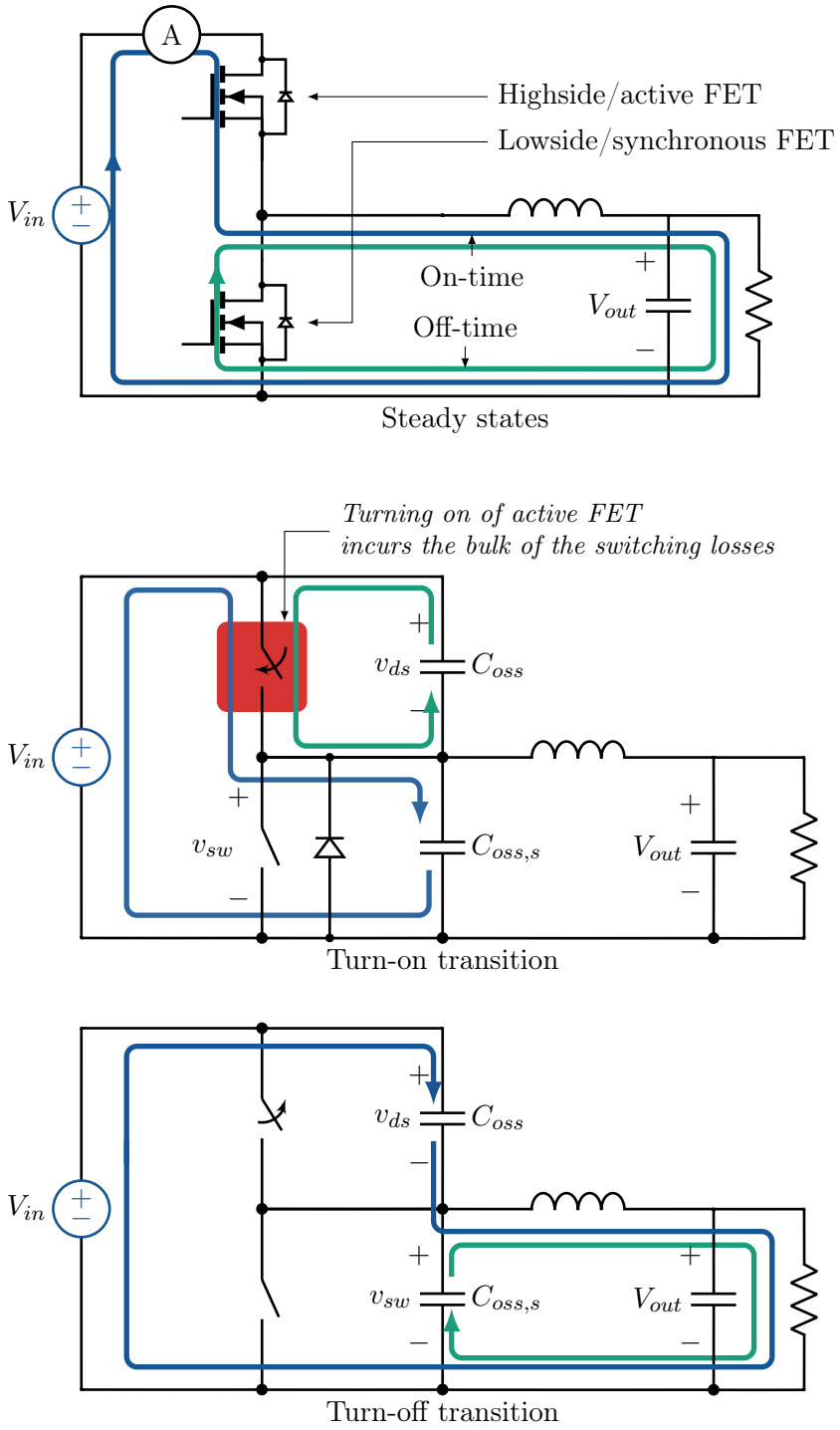


Figure 2.1: Displacement current during hard switching transitions of the high-side FET in a buck circuit or a half-bridge. Before the turn-on transition is a dead-time period when both switches are off and the inductor current is freewheeling in the reverse direction of the rectifying FET, which is represented by the diode.

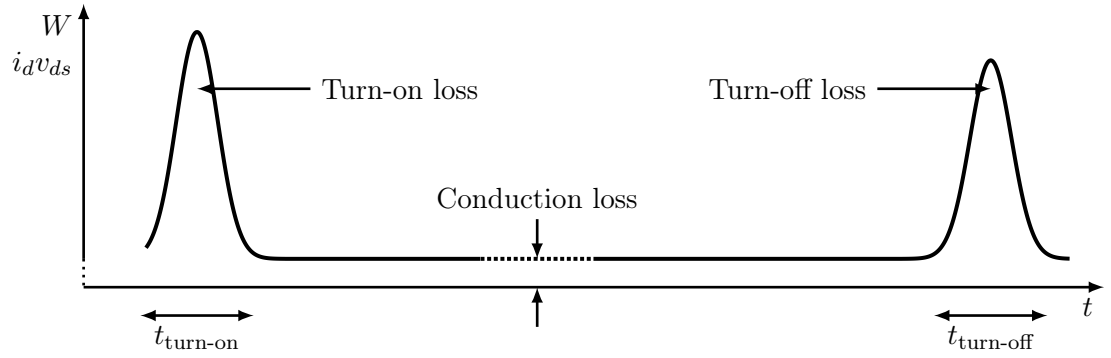


Figure 2.2: Power loss in a FET experiencing hard switching transitions.

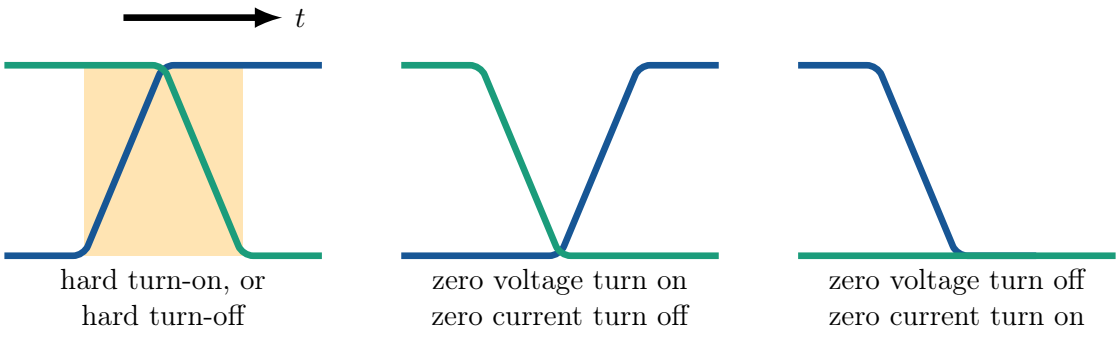


Figure 2.3: Ideal hard switching and soft switching waveforms.

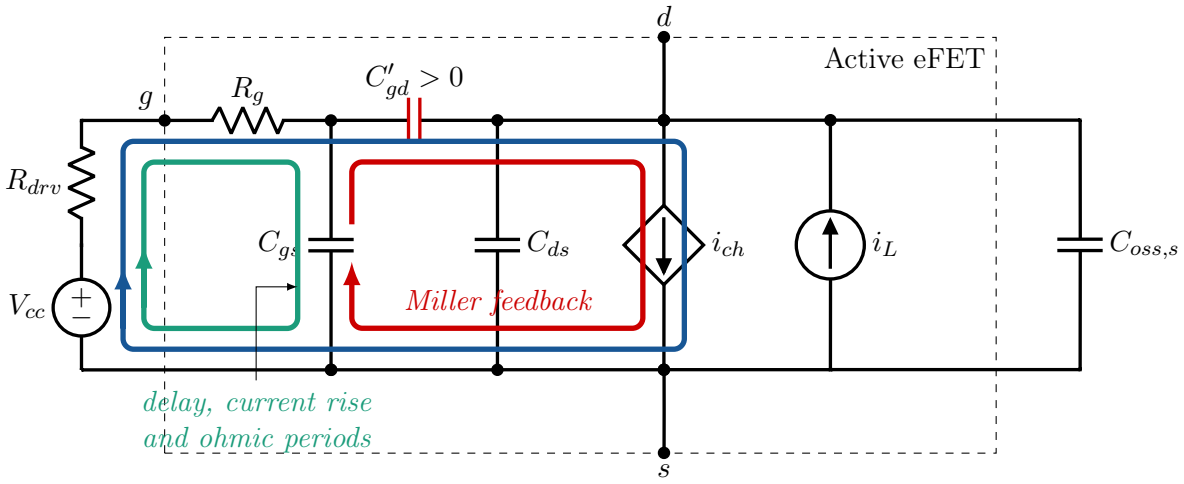


Figure 2.4: Equivalent circuit of an active eFET of a half bridge during a hard switching turn-on transition. On the left of the active eFET is the gate driver and on the right is the output capacitance of the synchronous switch. Adapted from [43].

2.1.1 Time delay

A model of an active eFET in a half-bridge during a hard switching transition is shown in Figure 2.4. In the initial phase of a turn-on transition, the gate voltage is rising but is lower than the FET's threshold voltage. Therefore there are no changes in drain variables in this period, hence its name. Performing a KCL around the gate node in Figure 2.4 and rearranging wrt the rate of change of gate voltage v'_{gs} leads to the expression in equation 2.1, where C_{iss} is the input capacitance of the FET, and R_G is the total series resistance as expressed in equations 2.2 and 2.3, respectively. Because there is change in drain voltage, the rate of change of gate voltage v'_{gs} can be expressed using equation 2.4 and approximated during the delay period as in equation 2.5.

$$(V_{cc} - v_{gs})/R_G = C_{iss}v'_{gs} - C_{gd}v'_{ds} \tag{2.1}$$

$$C_{iss} = C_{gs} + C_{gd} \tag{2.2}$$

$$R_G = R_{dr} + R_g \tag{2.3}$$

$$v'_{gs}|\{v'_{ds} = 0\} = (V_{cc} - v_{gs})/R_G C_{iss} \tag{2.4}$$

$$v'_{gs}|\{v'_{ds} = 0, v_{gs} = 0\} = V_{cc}/R_G C_{iss} \tag{2.5}$$

Therefore the gate voltage has a first order response and can be expressed as in equation 2.6, together with the drain- current and voltage as shown in equations 2.7 and 2.8, respectively. V_D is the source to drain conduction voltage of the synchronous FET during the its off state. This is incurred during the dead-time of a half-bridge when both switches are off, and for GaN E-HEMTs this is approximately 2 V. We can see that the lower the drive resistance, the faster the gate voltage is going to rise. This delay time can be approximated by using

the initial drive current and threshold gate charge as shown in equation 2.9.

$$v_{gs}|\{v'_{ds} = 0\} = V_{cc}\left(1 - \exp\left(-t/R_G C_{iss}\right)\right) \tag{2.6}$$

$$i_{ch} = 0 \tag{2.7}$$

$$v_{ds} = V_{in} - v_{sw}(t) = V_{in} + V_D \tag{2.8}$$

$$t_d \approx R_G Q_{th}/V_{cc} \tag{2.9}$$

2.1.2 Turn-on behaviour

The voltage reaches the threshold voltage V_{th} at which point the FET starting conducting a channel current that is proportional to the FET's transconductance g as shown in equation 2.10, which is assumed to be constant in this analysis. Displacement current of the parasitic capacitance in C_{gd}, C_{oss} and $C_{oss,s}$ begins to flow through the channel as illustrated in Figure 2.4. Gate voltage continues to increase, facilitating a larger channel current thereby allowing for v'_{ds} to continue increasing in magnitude. Now part of the gate current is diverted to C_{gd} to facilitate the voltage transient. Performing a KCL around the drain node in Figure 2.4 yields equation 2.11 [43].

$$i_{ch} = g(v_{gs} - V_{th}) \tag{2.10}$$

$$i_{ch} - i_L = C_{gd}(v'_{ds} - v'_{dg}) - (C_{ds} + C_{ds,s}) \cdot v'_{ds} \tag{2.11}$$

The LHS of equation 2.11 determines the capacity available for the voltage transition, and the RHS terms is the total displacement current required to facilitate the transition. The Miller voltage is the gate voltage that corresponds to the size of the load current not associated with a displacement current as expressed in equation 2.12. Substituting equations 2.12 and 2.10 into 2.11 yields equation 2.13. During the initial part of the voltage transition, the value of $(C_{gd}v_{gs})'$ is relatively small compared to the v'_{ds} term. Ignoring it yields an approximation

for the rate of change of the drain voltage [43]. Substituting equation 2.15 back into 2.13 yields an expression for the rate of change of gate voltage as shown in equation 2.16. During the initial phase of the voltage transition when $v_{gs} = V_m$, the first derivative of the gate voltage is shown in equation 2.17. Setting equation 2.16 to zero yields the plateau voltage where the Miller current is equal to the driver current as shown in equation 2.18. Equation 2.19 suggests the higher the plateau voltage, the faster the drain transient, and equation 2.18 suggests that a higher plateau voltage can be achieved with a higher load current.

$$V_m(i_L) = V_{th} + \frac{i_L}{g} \tag{2.12}$$

$$g(v_{gs} - V_m) = C_{gd}v'_{gs} - v'_{ds} \cdot (C_{oss} + C_{oss,s}) \tag{2.13}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{2.14}$$

$$v'_{ds} \approx \frac{-g(v_{gs} - V_m)}{C_{oss} + C_{oss,s}} \tag{2.15}$$

$$v'_{gs}(v_{gs}) = \frac{V_{cc} - v_{gs}}{R_G C_{iss}} - \left(\frac{C_{gd}/C_{iss}}{C_{oss} + C_{oss,s}}\right) g(v_{gs} - V_m) \tag{2.16}$$

$$v'_{gs}(V_M) = (V_{cc} - V_m)/R_G \cdot C_{iss} \tag{2.17}$$

$$V_P = v_{gs}|\{v'_{gs} = 0\} = \frac{V_{cc} + R_G(C_{gd}/C_{oss}) \cdot g \cdot V_m}{1 + R_G(C_{gd}/C_{oss}) \cdot g} \tag{2.18}$$

$$\min(v'_{ds}) = \frac{-g(V_P - V_m)}{C_{oss} + C_{oss,s}} \tag{2.19}$$

2.1.2.1 Switching losses

There are two sources of energy loss within a FET during a hard switching transition, namely gating losses incurred in the gate resistance and denoted by E_g, and channel losses incurred from the product of channel current and voltage and denoted by E_{ch} as shown in equation 2.20. The energy incurred in shorting all the charge in C_{oss} and charging C_{qoss} is given by equations 2.23 and 2.24, respectively [44]. Equation 3.21 expresses the total switching losses as a function of the drain variables, noting that the energy due to the internal C_{oss} is not

reflected in the drain variables. Equation 2.26 expresses the total switching loss with respect to the load and switching time, which includes the current and voltage transitions.

$$E = E_g + E_{ch} \tag{2.20}$$

$$E_g = C_{iss} V_{cc}^2 / k_d \tag{2.21}$$

$$k_d = R_g / (R_g + R_{dr}) \tag{2.22}$$

$$E_{oss} = \int_0^{V_{in}} C_{ds} v_{ds} \, dv_{ds} \tag{2.23}$$

$$E_{qoss} = \int_0^{V_{in}} (V_{in} - v_{ds}) C_{ds} \, dv_{ds} \tag{2.24}$$

$$E_{ch} = E_{oss} + E_{qoss} + E_{iv} = E_{oss} + \int_0^{t_v} i_d v_{ds} \, dt \tag{2.25}$$

$$E_{iv} \approx I_{load} V_{in} / 2 t_{iv} \tag{2.26}$$

2.1.3 Turn-off behaviour

We can see in Figure 2.1 that the displacement current during a turn-off transition does not flow through the channel, which means that the E-HEMT does not have to remain in the linear region until the voltage transition is complete. Therefore the load current can transition much more rapidly and the voltage transition is dependant on the size of the load, but because of the opposite directions of the load and displacement currents, the parallel channel actually slows down the turn-off transient, thereby causing some IV load losses [43]. Nevertheless the 2deg channel can be rapidly depleted and losses are comparatively much smaller to turn-on transitions if not negligible. We can see in Figure 2.5 that the gate voltage during a turn-off transition has a much smoother first order response.

2.1.4 Double pulse test simulation

A double pulse test circuit is compromised of a half-bridge and an output inductor shorted to ground, and is used to evaluate a FET's or a half-bridge's hard switching performance.

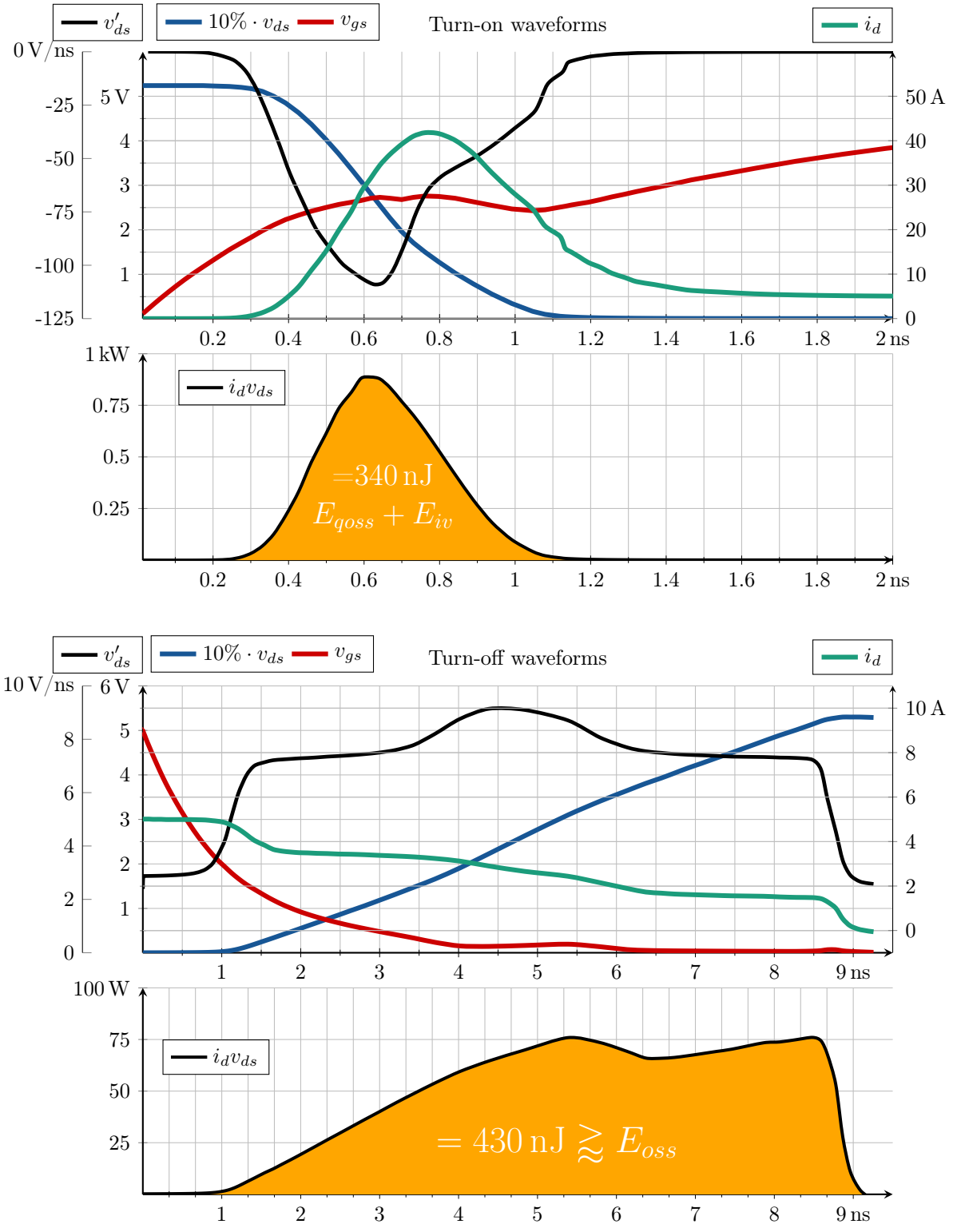


Figure 2.5: Hard switching transition turn-on and turn-off waveforms.

PARAMETER	CONDITIONS	VALUE	UNITS
Transconductance g		30	A/V
Gate resistance R_g		0.4	Ω
Total gate charge Q_g	$v_{ds} = 50\,\text{V}$ $i_d = 11\,\text{A}$	3.2	nC
Gate-to-source charge Q_{gs}		0.9	
Gate-to-drain charge Q_{gd}		0.6	
Threshold charge Q_{th}		0.55	
Output charge Q_{oss}	$v_{ds} = 50\,\text{V}$, $i_d = 0\,\text{A}$	18	
Input capacitance C_{iss}	$v_{ds} = 50\,\text{V}$ $v_{gs} = 0\,\text{V}$	339	pF
Reverse transfer capacitance C_{rss}		3	
Output capacitance C_{oss}		238	
Drain to source resistance	v_{gs}=5 V $I_d = 11\,\text{A}$	13.5	mΩ

Table I: General parameters for E-HEMT EPC2212, a 100 V 75 A E-HEMT by EPC.

Hard switching turn-on and turn-off waveforms of a 50 V, 5 A DPT of E-HEMT EPC2212 are shown in Figure 2.5, and its main parameters are listed in Table I. The driver has a turn-on/turn-off resistance of $R_{source} = R_{sink} = 1.5\,\Omega$.

We can see that gate voltage increases in a first order fashion and plateaus at 3 V, which correlates with the maximum rate of change in drain voltage of -110 V/ns. Afterwards, the current supplied by the driver is insufficient to facilitate the Miller effect and charge is pulled from C_{gs}, causing gate voltage to decrease with a slight slope until the end of the voltage transition. The FET then enters the ohmic region and the on-resistance decreases as the gate voltage continues to increase in a first order fashion as described in equation 2.4. The true gate voltage is behind the gate resistance and therefore can be estimated from the gate node voltage using the gate current as shown in equation 2.27, where $v_{gs,e}$ is the externally measured gate voltage, and v_{gs} is an estimate of the real gate voltage.

$$v_{gs} = v_{gs,e} - R_g i_g \tag{2.27}$$

We note that the drain current measurement includes the displacement current of C_{oss}

whether or not it is flowing in the channel. We also note that during the Miller period, the peak drain current lags the peak change in drain voltage, which the analyses in section 2.1.2 suggests ought to be in-line. However because C_{gd} is growing as voltage is decreasing and has a strong double derivative at low values, it effectively causing a delay in the current response. The Miller voltage is also reflected in the asymmetrical shape in the rate of change of drain voltage. Figure 2.6 illustrates how the driver's turn-on resistance and the size of the load current influence the gate voltage waveform.

2.1.4.1 Turn-on losses

The turn-on energy, is calculated to be 340 nJ. If we assume that the drain voltage decreases linearly for 1 ns, then the IV channel loss can be approximated as the area of a triangle as shown in equation 2.28, which suggests that the channel load losses make up two fifths of the total switching loss. Load channel losses can be minimized with a faster transition.

$$E_{iv,on} \approx \frac{1}{2} \times 50\,\mathrm{V} \times 5\,\mathrm{A} \times 1\,\mathrm{ns} = 125\,\mathrm{nJ} \tag{2.28}$$

2.1.4.2 Turn-off losses

The bulk of the product of drain to source current represents the energy stored in the output capacitance; as opposed to the turn-on transition when the displacement current of the FET wasn't being measured in the first place and the losses associated with C_{oss} were above the measured $i_d v_{ds}$ [45]. We can see that the drain current dips when the voltage begins to increase towards 5 V. We can estimate the turn-off losses using equation 2.29, which suggests that the turn-off load losses are 10 times lower than the turn-on losses.

$$E_{iv,off} \approx \frac{1}{2} \times 5\,\mathrm{V} \times 5\,\mathrm{A} \times 1\,\mathrm{ns} = 12.5\,\mathrm{nJ} \tag{2.29}$$

2.1.5 Estimating current rise and voltage fall times

The switching transition incurs channel losses associated with the load during the current and voltage transitions. This loss is influenced by how long the switching transition takes and is therefore relevant to optimising gate drive parameters.

Voltage remains constant during the current rise, and the load loss incurred during the current transition is given by equation 2.30. Assume that v'_{ds} is constant, we can estimate the load loses as in equation 2.31. Both these equations rely on a constant rate of change in gate voltage i.e. $v''_{gs} = 0$. The duration of the current transition is inversely proportional to the transconductance as shown in equation 2.32. Taking a derivative of equation 2.15 and then doing a double integral results in the approximation for the duration of the voltage transition in equation 2.33. The total losses can be approximated as being directly proportional to the input variables and switching time as expressed in equation 2.34.

$$E_{Li} = I_L V_{in} t_i / 2 \tag{2.30}$$

$$E_{Lv} = I_L V_{in} t_v / 2 \tag{2.31}$$

$$t_i = I_L / g v'_{gs} \tag{2.32}$$

$$t_v = \sqrt{4 Q_{oss} / g v'_{gs}} \tag{2.33}$$

$$E_L = I_L V_{in} (t_i + t_v) / 2 \tag{2.34}$$

2.1.6 Drain transients

E-HEMTs have lower turn-on gate thresholds and parasitic gate capacitance than MOSFETs making them more susceptible to drain voltage transients as shown in Figure 2.7 [42, 46]. Drain voltage is subject to a circuit's operation and is especially challenging in hard switching

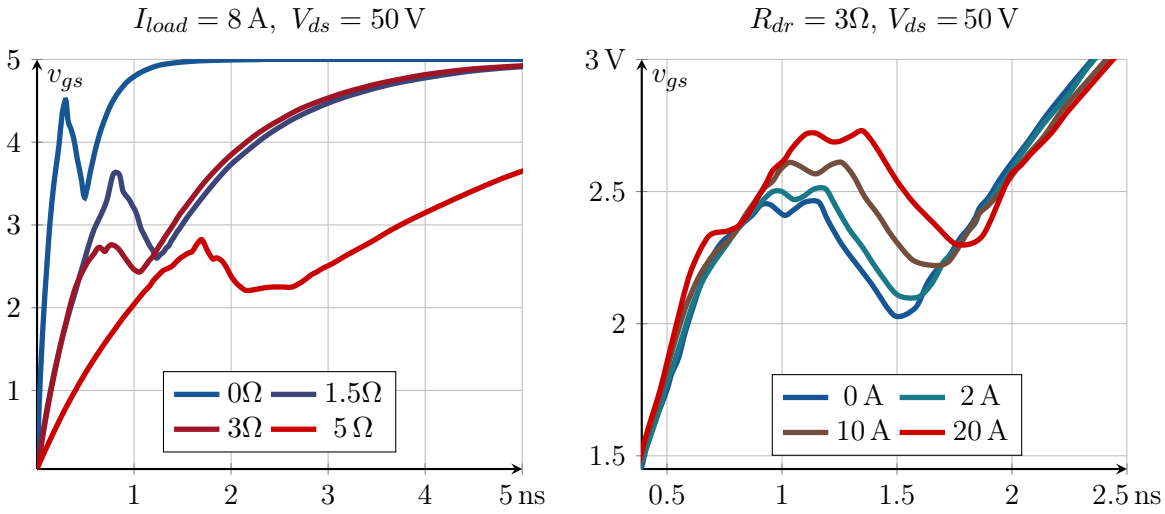


Figure 2.6: Impact of driver's resistance and load current on gate voltage during a hard switching turn-on.

application that experience fast voltage transition, which while reduces switching loss, induce a greater amount of charge in a rectifying FET as shown, risking shoot-through which has detrimental consequences. Soft switching applications can also experience drain transients that are typically accompanied by much greater resonating voltages such as in Class E power amplifier. Drain (to source) transients impress a current in the drain to gate capacitance – referred to in datasheets as a reverse transfer capacitance C_{rss} – which is shorted to the source through the gate to source capacitance C_{gs}. We will first model the impact on a drain transient on a source that is not connected to ground.

2.1.6.1 Transients on an un-sourced gate

Without a path to the source, drain charge will accumulate in the gate as expressed in equation 2.35. Substituting this current back into the definition of gate to source capacitance

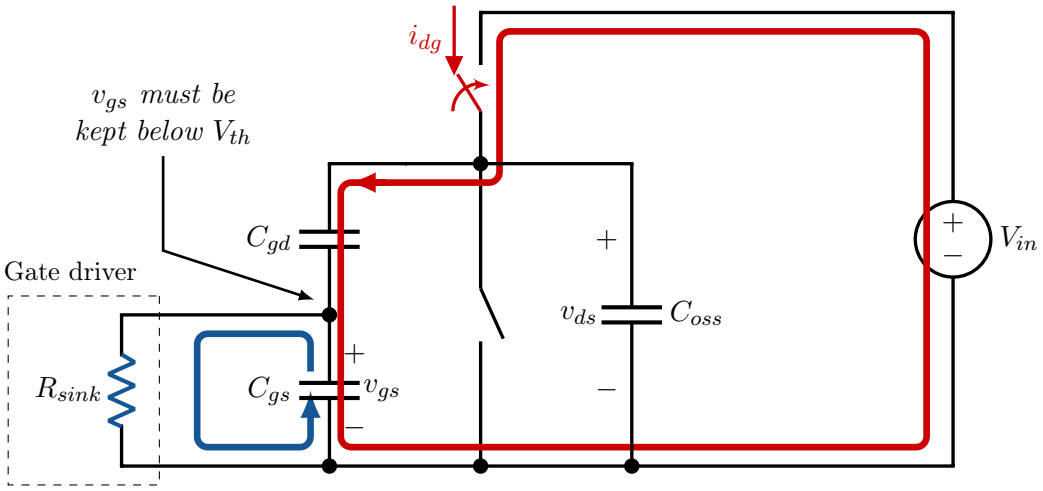


Figure 2.7: Impact of drain voltage transient on a synchronous/low-side switch. The faster the turn-on, the higher the rate of change of the drain-source voltage, thus the more charge will be transmitted to the gate. The gate has to be sufficiently tied to the source through a low impedance path (R_{sink}) to sink any energy in the gate avoiding a false turn-on.

yields the scaled current that flows into the gate as shown in equation 2.37.

$$i_{gs} = C_{gd} v'_{dg} = C_{gs} v'_{gs} \tag{2.35}$$

$$C_{iss} = C_{gs} + C_{gd} \tag{2.36}$$

$$i_{gs} = \frac{C_{gs} C_{gd}}{C_{iss}} v'_{ds} \tag{2.37}$$

$$v'_{gs} = \frac{C_{gd}}{C_{iss}} v'_{ds} \approx \frac{C_{gd}}{C_{gs}} v'_{ds} \tag{2.38}$$

Equation 2.38 suggests that the rate of change of the synchronous' gate voltage is directly proportional to the rate of change of drain voltage by the ratio of the drain-source to gate-source capacitance, which is fairly constant for E-HEMTs [11]. In hard switching, voltage transitions with a magnitude of V_{in}, which is the total voltage seen across the FET i.e. $\int_0 v'_{ds} dt = V_{in}$. Therefore the gate voltage rise is a scaled by the rise in v_{ds} by C_{gd}/C_{iss} as shown in equation 2.39, and using equation 2.35 we can describe the total charge entering

the gate as in equation 2.40:

$$\Delta V_{gs} = -\frac{C_{gd}}{C_{iss}} \int_0 v_{ds}\, dt = \frac{C_{gd}}{C_{iss}} V_{in} \tag{2.39}$$

$$Q_{tr} = \int i_{gs}\, dt = \frac{C_{gs} C_{gd}}{C_{iss}} V_{in} \tag{2.40}$$

For example in a hard switching application with an input voltage of 100 V and $C_{gd}/C_{iss} = 1\%$, the gate voltage will rise by 1 V which is well within the range of V_{th} for E-HEMTs and therefore risks shoot-through and needs to be addressed. Note that the rate of change of drain voltage is not the issue for an un-sourced but rather it is the magnitude of the input voltage that determines the amount of charge that will ultimately accumulate in the gate, which can be estimated using equation 2.37.

2.1.6.2 Transients on a sourced gate

Positive charge accumulating in the gate needs to be rapidly drained to avoid false turn-on. A pre-existing negative gate potential can be provided by a negative turn-off voltage to offset this charge. On the other hand it will increase the drain-source reverse conduction loss during dead-time. For totem pole drivers this is typically done by connecting the gate to the source through a low impedance path, represented by R_{sink} as illustrated in Figure 2.7, which includes the gate resistance. Now a gate current can be directly sourced to ground as shown in equation 2.41, and taking its Laplace and rerranging for $v_{gs}(\mathbf{s})$ yields equation 2.42. If we assume that v'_{ds} is a constant then we have a first order response as shown in equation 2.43, which suggests that the gate voltage reaches a maximum over time, and that the maximum voltage rise is a linear combination of all three relevant variables. $\overline{v'_{ds}}$ can be approximated using half the peak maximum drain voltage in equation 2.19. Compared to an un-sourced gate, the magnitude of the input voltage has no effect on the gate voltage rise

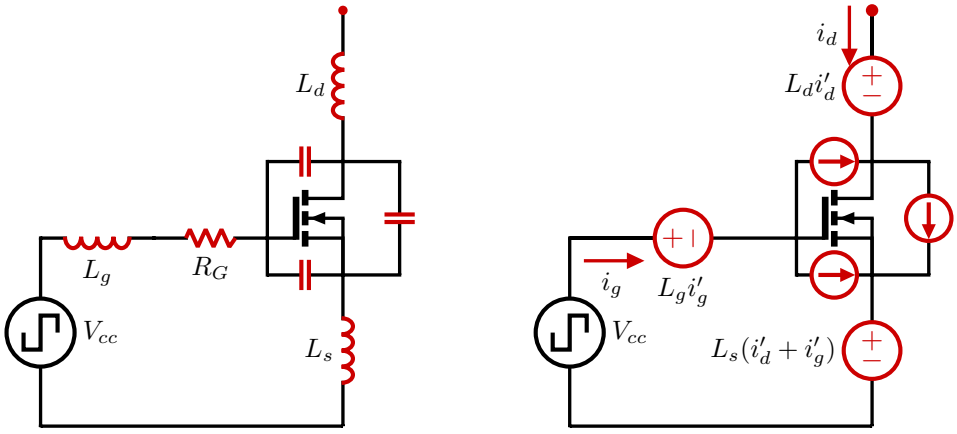


Figure 2.8: Parasitics surrounding a FET and an equivalent AC circuit representing parasitic capacitance and inductance as current and voltage sources, respectively.

but rather its the rate of change of the drain voltage that determines the peak gate voltage.

$$C_{gs}v'_{gs} = i_{dg} - i_{sink} = C_{gd}v'_{ds} - v_{gs}/R_{sink} \tag{2.41}$$

$$v_{gs}(\mathbf{s}) = \frac{(C_{gd}/C_{gs})v'_{ds}(\mathbf{s})}{\mathbf{s} + 1/R_{sink}C_{gs}} \tag{2.42}$$

$$v_{gs}(t) = R_{sink} \cdot C_{gd} \cdot \overline{v'_{ds}} \cdot (1 - e^{-t/R_{sink}C_{gs}}) \tag{2.43}$$

The speed of a drain transient during a hard switching turn-on has to be curtailed such that the induced gate current in the synchronous switch does not falsely turn-on and cause a shoot-through. This is why the synchronous FET in a half-bridge is recommended to have a turn-off resistance that is at least five times smaller than the turn-on resistance of the active FET.

2.1.7 Parasitic inductance

High speed transitions by GaN devices exhibit high rates of change in drain and gate voltage and current [29]. Therefore gate drive and power drive circuitry need to be sufficiently dense to provide minimal parasitic capacitance and inductance [47]. Inductance is influenced by the transistor's packaging and its overall integration in the circuit geometry. Given that

GaN devices are must faster than silicon MOSFETs, they need to be fitted in packages with minimal impedance if their high speed capabilities were to be tapped [48]. Parasitic inductance includes terminal and path inductance between and within the drive circuitry. In contrast to the analysis we saw earlier in subsection 2.1 where current and voltage transitions happen sequentially, parasitic inductance intermingles the current and voltage commutations [49]. After passing the threshold voltage, the FET begins to conduct a load current at a rate proportional to its transconductance. Loop inductance will curtail the current rise and because the FET is operating linearly its gate voltage will be suppressed. During the current commutation period the current magnitude is controlled by the gate voltage as in equation 2.10. The impedance by source-drain inductance can be modelled using a voltage source as shown in equation 2.44.

$$v_{L,s} = L_s i'_D = g L_s v'_{gs} \tag{2.44}$$

Parasitic inductance curtails the current rise thereby reducing the voltage across the gate. The drain current is made up of the channel current as well as any current derived from the gate's parasitic capacitance that is induced by any changes in drain voltage as shown in equation 2.45. We can express gate current as a function of drain voltage as shown in equation 2.46. Gate inductance will detract from the voltage across the gate as shown in Figure 2.8, and as expressed in equation 2.47.

$$i_D = i_{ch} + (C_{ds} + C_{gd}) \cdot v'_{ds} \tag{2.45}$$

$$i_g = C_{gs} v'_{gs} + C_{gd}(v'_{gs} - v'_{ds}) \tag{2.46}$$

$$v_{gs} = V_{cc} - R i_g - g L_s v'_{gs} - L_g i'_g \tag{2.47}$$

We can ignore gate inductance and use drain inductance to reflect the incremental inductance in the power loop i.e. $L_g = 0$, $L_d > L_s$. Converting equations 2.45, 2.46, and 2.47 into the

Laplace domain and rearranging wrt v_{gs} yields the second order solution [50]:

$$v_{gs}(\mathbf{s}) = \frac{V_{gs}}{\tau_m \tau_G' \cdot \mathbf{s}^2 + \tau_G'' \cdot \mathbf{s} + 1} \tag{2.48}$$

Where $\tau_m = gL_d$,$\tau_{G'} = C_{gd}R_g$, $\tau_{G''} = R_g C_{iss} + gL_s$. The underdamped solution is when $\tau_{G''}^2 < 4\tau_{G'}\tau_m$. We can deduce from that that the greater the product of $gL_D C_{gd} R_g$ the greater the likelihood for sinusoidal behaviour. The underdamped solution yields the following gate voltage, drain current and drain voltage, respectively:

$$V_{gs}(t) = V_{cc} - (V_{cc} - V_{th}) \exp\left(-t/\tau_a\right) \cdot \left(\cos(\omega_a t) + \frac{\sin(\omega_a t)}{\omega_a \tau_a}\right) \tag{2.49}$$

$$i_d(t) = g(V_{cc} - V_{th}) \left(1 - e^{-t/\tau_G} \left(\cos(\omega_a t) + \frac{\sin(\omega_a t)}{\omega_a \tau_a}\right)\right) \tag{2.50}$$

$$v_{ds}(t) = V_{in} - g(V_{cc} - V_{th})\omega_a(L_s + L_d) \cdot e^{-t/\tau_a}(1 + \left(\frac{1}{\omega_a \tau_a}\right)^2 \sin(\omega_a t)) \tag{2.51}$$

$$\tau_a = 2\tau_m \tau_G \prime / \tau_G'' \tag{2.52}$$

$$\omega_G = \left(1/\tau_m \tau_G - \left(\tau_G''/2\tau_m \tau_G'\right)^2\right)^{1/2} \tag{2.53}$$

Where $V_{gs,main}$ is the gate voltage at the end of the main transition period. The preferred overdamped solution is when $\tau_{G''}^2 > 4\tau_{G'}\tau_m$ and has the solution:

$$v_{gs}(t) = V_{cc} - (V_{cc} - V_{th})(e^{-t/\tau_b}\tau_b - e^{-t/\tau_c}\tau_c)/(\tau_b - \tau_c) \tag{2.54}$$

$$i_d(t) = g(V_{cc} - V_{th}) \left(1 - e^{-t/\tau_b}\tau_b - e^{-t/\tau_c}\tau_c/(\tau_b - \tau_c)\right) \tag{2.55}$$

$$v_{ds}(t) = V_{in} - g(V_{cc} - V_{th})(L_g + L_d)(e^{-t/\tau_b}\tau_b - e^{-t/\tau_c}\tau_c)/(\tau_b - \tau_c) \tag{2.56}$$

$$\tau_b = 2\tau_m \tau_{G'} / \left(\tau_G - \left(\tau_{G''}^2 - 4\tau_m \tau_{G'}\right)^{1/2}\right) \tag{2.57}$$

$$\tau_c = 2\tau_m \tau_{G'} / \left(\tau_G + \left(\tau_{G''}^2 - 4\tau_m \tau_{G'}\right)^{1/2}\right) \tag{2.58}$$

We can see in Figure 2.9 the drain voltage dips once the drain begins conducting a current

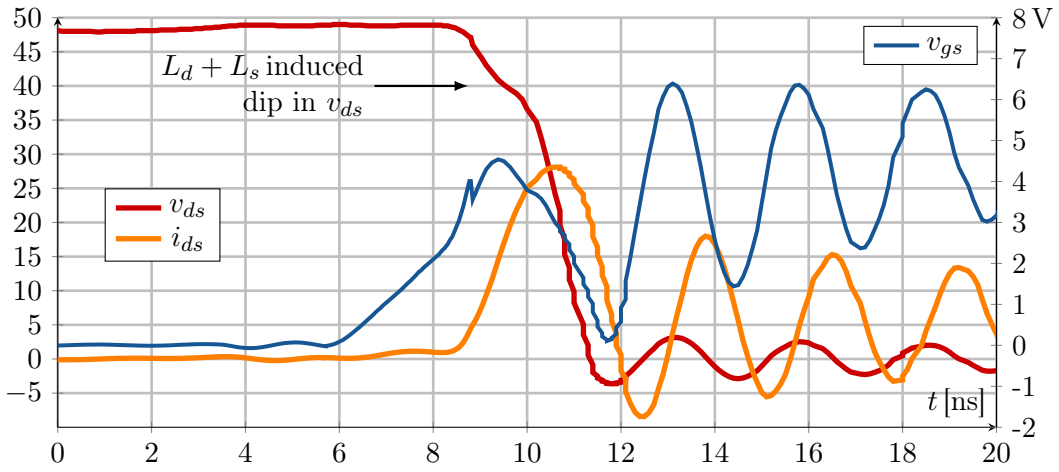


Figure 2.9: Hard switching turn-on with considerable parasitic inductance. The circuit includes a half-bridge of two EPC2001 GaN E-HEMTs with a load current of 0.5 A, input voltage of 48 V, common source inductance of 100 pH and gate inductance of 1 nH.

through L_d. This means that transition's voltage differential is lower. Furthermore, the parasitic inductance enhances the displacement current flow. Both these actions cause a faster voltage transition, but incur a negative voltage overshoot and oscillation (During a turn-off transition, the parasitic drain-source inductance prolongs the voltage rise time). At approximately at $t = 9$ ns when the gate enters the Miller period where it is expected that the gate voltage will plateau or decrease slightly, the Miller effect is so strong that the gate voltage returns back to zero until the voltage transition is complete, during which the channel current is also depleted as the E-HEMT returns to the linear region. After which the voltage rises again towards V_{cc} in an underdamped fashion with a frequency of $1/2\pi\sqrt{(L_d + L_s)C_{oss}}$.

2.2 Current Source Gate Drive

Suppose that a driver that has the capability of cycling power to a FET's gate with a constant current as shown in Figure 2.10. Such a driver has more leverage on switching speed allowing faster transitions and lower switching losses, and because the current source is based on inductance, it is capable of recovering electrical energy stored in the capacitor that

is dissipated in voltage source drives. Estimating switching times of current drives is simpler and more accurate because charge is the product of current and time and charge takes into account non-linear capacitance. For example, if a FET has a total gate charge of 2 nC at its turn on voltage, then it will take 2 ns to cycle the gate with a current of 1A or 1 ns with 2 A as illustrated in Figure 2.10(a). A current source driver essentially compresses voltage-charge relationship as shown in Figure 2.10(b), and because its a constant current source, it's blind to the supposed enhancement voltage and requires stringent gate voltage regulation, which is typically provided through diodes. The literature includes several other kinds of voltage source drivers that are enhancements of the totem pole [51, 52], as well as current source drivers[53, 54, 55, 56]. [57] provided a loss model for resonant drivers including their parasitic inductance. Other current source gate drivers are going to be reviewed below.

2.2.1 Current source drive advantages

1. High efficiency: current source drivers have inductance that can recover energy stored in the gate through resonance that would otherwise be dissipated.
2. Optimized and sustained gate current: A conventional drive has an exponentially decaying gate current profile while a current source driver maintains gate current, allowing for a faster and more efficient switching process. Leverage over gate current means a greater degree of freedom when it comes to minimizing hard switching losses.

2.2.2 Minimizing E-HEMT losses

Energy dissipated within a FET is of particular concern because it typically has the highest temperature and heat flux within a circuit. Thermal management is critical if GaN's superior characteristics are to be exploited. There are two sources of energy loss within a E-HEMT, namely losses in the gate and in the channel as shown in equation 2.59. On one hand having a low gate current allows for low gate losses, but on the other hand having a high gate current

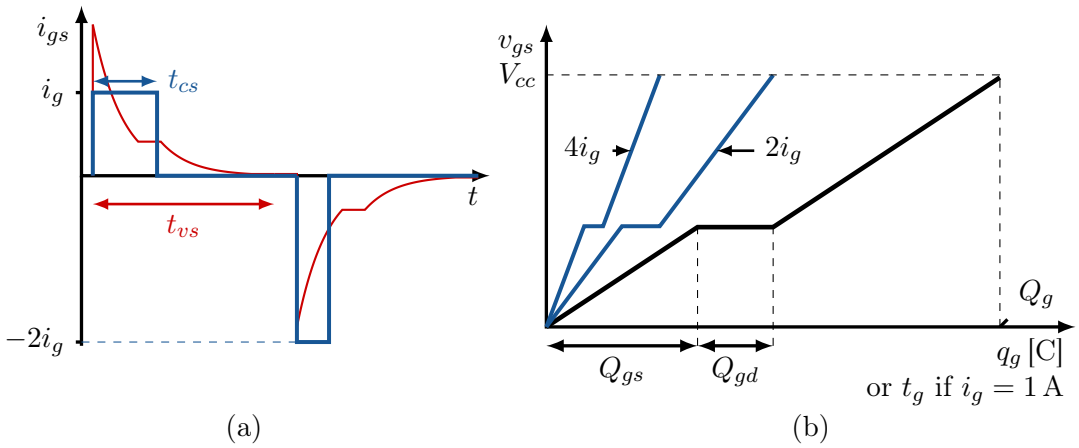


Figure 2.10: (a) Gate current in a current source gate driver (blue) vs voltage source gate driver. The discharging current is twice the size of the charging current. The areas under the current curve represents the total gate charge and is equal for both curves. (b) Gate voltage vs charge for a FET

reduces switching load losses in the 2deg channel. Energy lost in the gate with resistance R_g during a cycle including two transitions is given by equation 2.61, assuming that the gate current utilized in the turn-on and turn-off transitions are equal. The total time to cycle the gate, that is to discharge the capacitor from V_{cc} or charge to V_{cc}, can be calculated using equation 2.60, and so the energy wasted in the gate during a cycle is given by equation 2.61, where Q_g is the total gate charge. Losses due to the displacement of C_{oss} and $C_{oss,s}$ are time-independent and so load losses are the only time-dependant channel losses that the driver has the capacity of curtailing by providing for a faster transition.The turn-on losses can be expressed using equation 2.62. Q_{sw} is the total charge associated with duration of the current and voltage transitions, Q_{gd} is the gate to drain charge and associated with voltage transition; Q_{gs} is charge accumulated in the source before a voltage transition including current transition, and Q_{th} is the charge required to reach the threshold voltage, which is subtracted because it merely delays the transition and does not contribute to channel load loss.

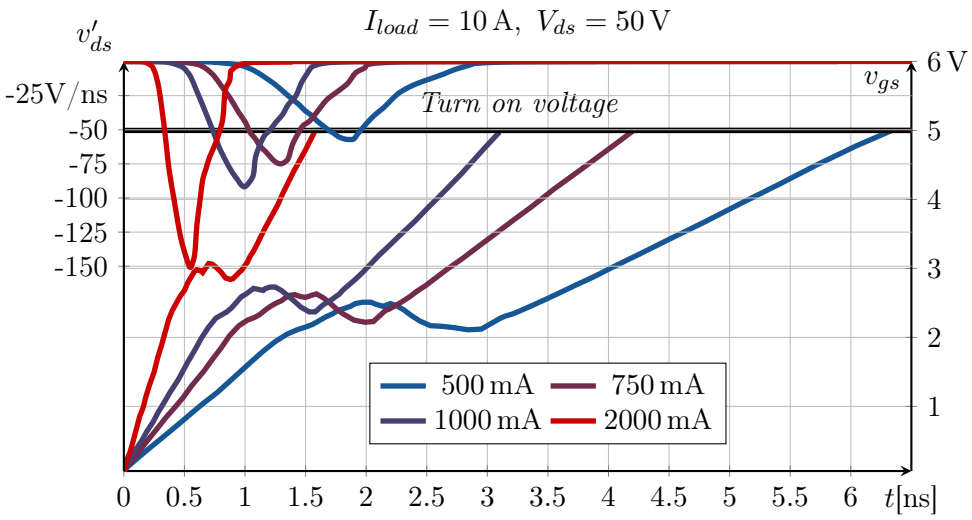


Figure 2.11: Gate voltage during a hard switching turn-on transition using a current source gate drive. The gate current is interrupted once the gate voltage reaches the turn on voltage of 5 V.

$$E_{sw} = E_g + E_{ch} \tag{2.59}$$

$$\tau_i = Q_g / i_L \tag{2.60}$$

$$E_g = 2 i_L^2 R_g \tau_i = 2 i_L R_g Q_g \tag{2.61}$$

$$E_{iv} = Q_{sw} I_{load} V_{in} / 2i \tag{2.62}$$

$$Q_{sw} = Q_{gd} + Q_{gs} - Q_{th} \tag{2.63}$$

The summation of the gate and the turn-on channel losses indicates that there is a current minima $i^\star$ that minimizes the total losses within the FET expressed in equation 2.64 and illustrated in Figure 2.12, which also shows that even a conventional drive with no drive resistance will still not provide an optimal switching performance vis-a-vis E-HEMT losses. We can see that the optimal gate current is proportional to the square root of the power across the switch. This calculation does not consider the gate drive losses, but it highlights that the gate current that minimizes hard switching losses in a FET is significantly greater

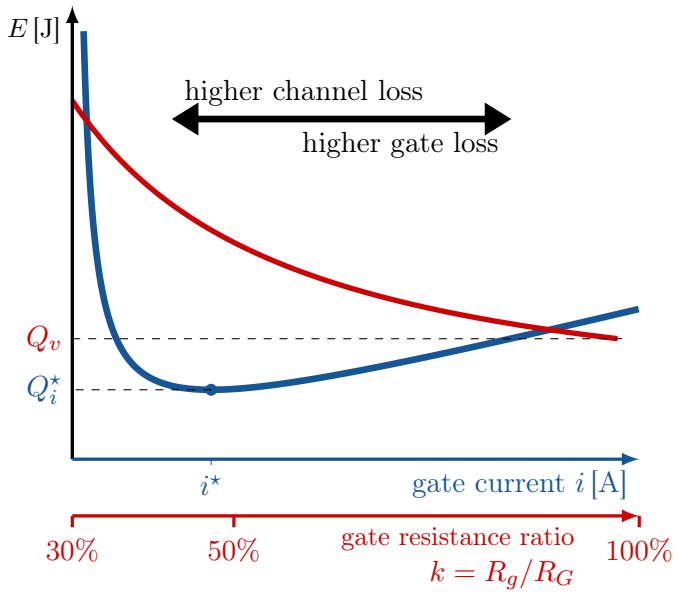


Figure 2.12: Hard switching loss in a HEMT with respect to gate current in a current source driver and with respect to k the ratio of gate resistance to total drive resistance in a voltage source driver .

than what conventional drives can offer.

$$i^\star = \sqrt{\frac{Q_{sw} I_{load} V_{in}}{4 Q_g R_g}} \tag{2.64}$$

2.2.3 Baseline with conventional drive

We saw that the ideal switching dynamics deviate from first order behaviour during the voltage transition. We can approximate the switching time as $1.6 R_g C_{iss}/k_d$ [58] where R_g is the gate resistance, C_{iss} is the input capacitance and k_d is the ratio of the gate resistance to the total drive resistance. On the other hand a current source drive will have a switching transition as shown in equation 2.60, and so a constant current source drive needs to have a magnitude as shown in equation 2.65 to match the speed of a conventional drive. In [58] Q_{sw}/Q_g is effectively approximated as 80%, which is in line with low voltage GaN E-HEMTs.

On the other hand, if we want to match the losses of a conventional drive, we can equate equation 2.61 with $C_{iss}V_{cc}^2$, which yields the current in equation 2.66.

$$i_L|\{t_i > t_v\} > \frac{Q_{sw}}{Q_g}\frac{k_d V_{cc}}{1.6R} \approx \frac{k_d V_{cc}}{2R_g} \tag{2.65}$$

$$i_L|\{C_{iss}V_{cc}^2 > E_g\} < \frac{C_{iss}V_{cc}^2}{2R_g Q_g} \tag{2.66}$$

2.2.4 High voltage energy storing

The gate current in a conventional drive is a function of the voltage differential across the gate. In a conventional driver, the differential's upper bound is the voltage source magnitude V_{cc}, which decays in roughly a first order fashion. The initial voltage differential can be increased by using a higher voltage but from a finite source i.e. a small capacitor. An inductor is added in series to curtail the initial peak current and to provide resonance. This is called high voltage energy storing and is explored in [52, 59, 60].

2.2.5 Resonant gate drive with continuous current

In [61] the totem pole driver is modified by adding an inductor in parallel with the gate as shown in Figure 2.13. The added capacitor is large and included to remove any bias dc current, and is not part of the resonant circuit or analysis. The switches operate in the same complimentary fashion as in a conventional drive except with a dead time to allow for a gate transition. During the steady states when the inductor is connected to the source or to ground, its current is increasing or decreasing at a constant rate, respectively. When both switches are off, the inductor forces a positive or negative current through the gate. This is the essence of how a current source gate driver works: using a current source that is not constrained by the dynamics of a voltage differential and can override the parasitic

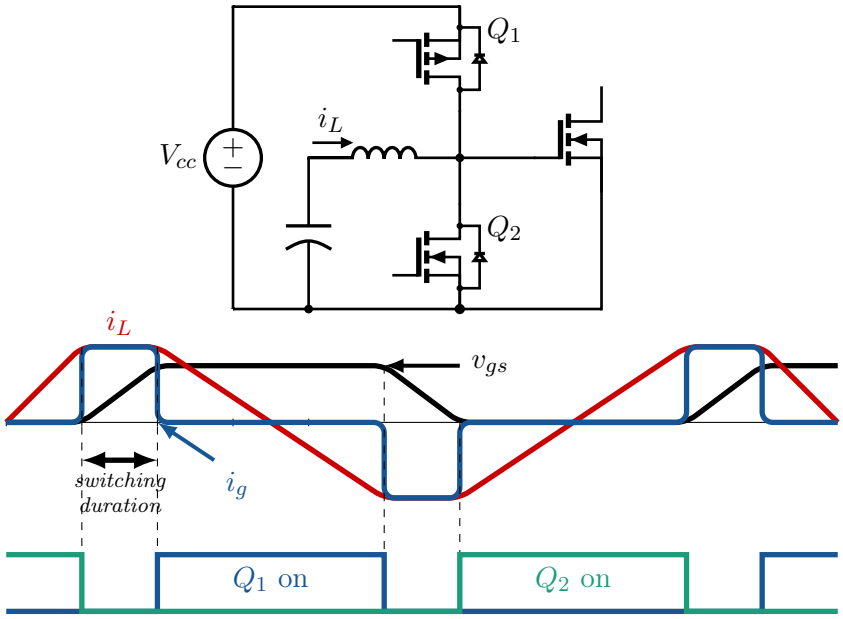


Figure 2.13: Resonant gate driver proposed in [61].

inductance. This driver is simple to design and configure. Its main drawbacks is the high conduction loss considering the continuous current through the inductor and one of the switches, which leads to an upper bound on the frequency that the driver will be more energy efficient than the totem pole. Therefore, the FOM of these switches may have to lean towards having a lower on resistance compared to their totem pole counterparts, which means it will not have a superior dynamic performance. Current source drivers with a continuous inductor current have higher circulating losses, higher inductance, and slower response than discontinuous current source drivers [62].

2.2.6 Resonant gate drive

This proposed gate drive in [63] is shown in Figure 2.14 and is another upgrade to the totem pole driver. An inductor is placed in series with the gate, as well as one diode between the gate and source that clamps negative voltage and another diode between the gate and V_{cc} to clamp positive voltages beyond the enhancement voltage. Interestingly the position of

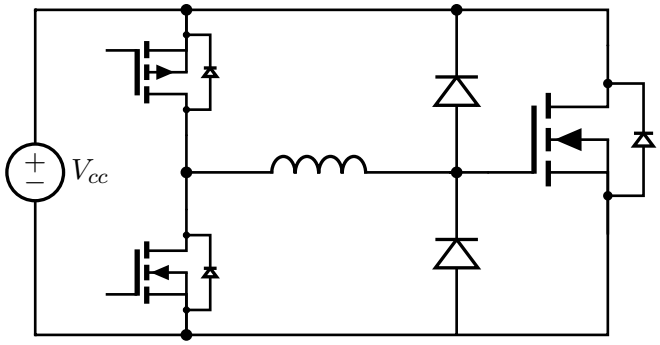


Figure 2.14: Resonant gate driver proposed for GaN E-HEMTs by Long et. al

this inductor is the same as that of parasitic gate inductance which is highly undesirable. However by tuning this inductance to be in full resonance we can use it to provide a more stable current providing for a faster transition. Such an under-damped operation can be described using second order dynamics found in A.2.2. Because resonance will introduce voltage overshoot, clamping is required to prevent the gate from being damaged, which is provided by the diodes. GaN E-HEMTs have lower gate resistances than MOSFETs and would therefore have relatively higher quality factors. Given a quality factor greater than give, the time required to cycle power to the gate can be estimated using equation 2.67 [63]. Note that the transition time no longer depends on gate resistance as in a totem pole gate drive, but on the LC values instead. The energy dissipated in the internal gate resistance is given by equation 2.68, where C_{iss} is the effective input capacitance including the diodes output capacitance. We can see that the portion of gating losses is divided between the gate and the resonant LC circuit, which is represented by its characteristic impedance Z_0 shown

in equation 2.69, which also suggests limited control over gating losses in the E-HEMT.

$$t_r = \pi/2 \cdot \sqrt{LC_{iss}} \tag{2.67}$$

$$E_g = \left(\frac{R_g}{R_g + Z_o}\right) C_{iss} V^2 \tag{2.68}$$

$$Z_o = \sqrt{L/C_{iss}} \tag{2.69}$$

$$I_{peak} = V_{cc}\sqrt{C_{iss}/L} \tag{2.70}$$

$$i(t) = \frac{2V_{cc}}{(4L/C_{iss} - R_G^2)^{1/2}} \cdot \exp\left(\frac{-R_G t}{2L}\right) \tag{2.71}$$

Given that E-HEMTs have lower input capacitance, the transition time would be quicker than in MOSFETs. While resonant transitions can accelerate transitions from 1.5 time constants to less than a half, its biggest drawback is that the resonant frequency sets the lower bound of the transition and the resonant inductor has to be large enough to have a sufficiently high quality factor.

2.2.7 Full bridge with inductor

The discontinuous resonant driver considered previously still behaves as a voltage source driver in the sense that the transitions are induced by voltage sources. Drivers described as current source gate drivers have a pre-charged inductor that has relatively more energy than the gate can accept, and therefore will maintain a high and constant gate current during a transition. Therefore conduction losses make a considerable portion of a current source driver's losses. Installing an inductor at the output a full bridge allows for a current to be generated discontinuously in either direction as proposed in [54]. A full bridge includes four switches configured in an H which can be seen as two half bridges sharing a load, and the gate is connected to one of the legs as shown in Figure 2.15.

Charging an inductor from left to right in order to turn on a gate is done through switches Q_2 and Q_3. This causes current to increase at a near constant rate of V_{cc}/L. Once

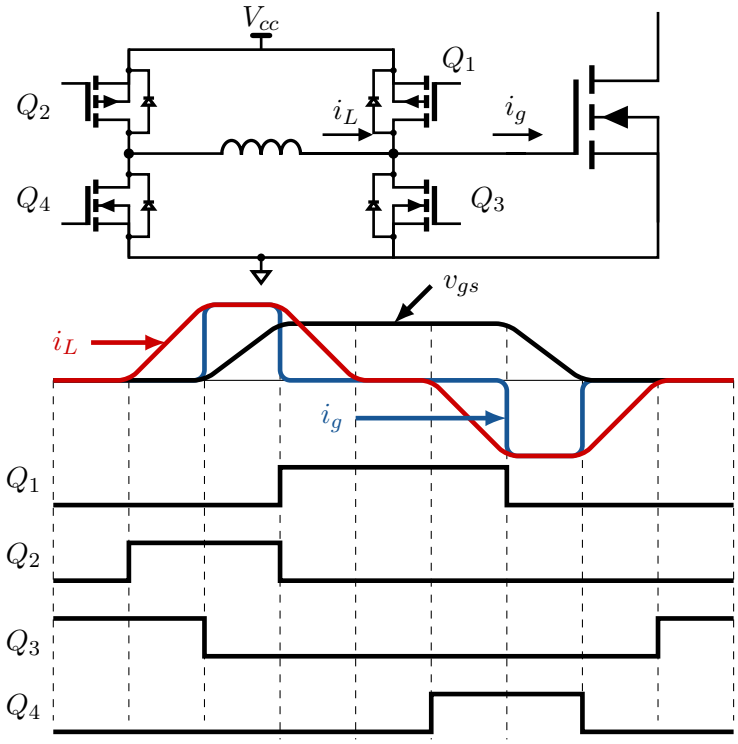


Figure 2.15: Full bridge inductor proposed by Eberle.

the inductor is charged with a pre-determined amount of current, Q_3 is opened forcing a current through the gate. Once the gate reaches a voltage equal to V_{cc} the body diode of Q_1 becomes forward biased which diverts the inductor current back to the source. During which Q_1 is softly turned on and conducts the current through its channel with lower losses and clamps the gate to V_{cc} through its channel. The opposite actions are applied to discharge the capacitor. The driver was also applied to a synchronous half bridge and the top driver was equipped was a bootstrapped supply to provide a floating source [64].

2.2.8 Current diversion problem

Current source drivers rely on diodes to provide voltage clamping to prevent the gate from causing a voltage overshoot. During discharging, there is a voltage differential across the gate that is proportional to the size of the gate current. The larger the gate current, the

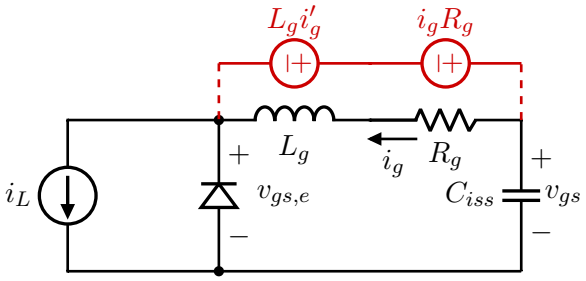


Figure 2.16: Illustration of the current diversion problem.

larger this voltage differential is going to be. This could be problematic as this could cause the diode to prematurely accept the inductor current, thereby reducing the gate current and consequently, the rate of change of gate voltage. This situation is made even more untenable by parasitic source and gate inductance which subtracts from the voltage across the gate, causing the current to prematurely divert through the diode. This is referred to as the current diversion problem, and it can increase the turn-off losses in a high-side FET [65], and is highlighted in Figure 2.16. To provide a bipolar supply a series of diodes can be connected in series of diodes that can be used, however this will greater energy losses [66, 67].

2.2.9 Motivation for synchronous resonant drive

One of the main challenge of the conventional totem pole driver operating in a half bridge is the Miller charge that accumulates following the turn-on of a high-side FET [68]. The driver has to have a very low impedance path for the low-side gate to absorb drain charge induced by a transient at the switching node as described in 2.1.6. Furthermore the push-pull driver operates on a single switch, and so requires fine dead time synchronization to minimize the energy losses when both switches are off. This is especially problematic for GaN devices that can switch in under 1 ns [69]. Operating with accurate dead times at this speed requires a controller circuit synchronized to a very fast clock with signal traces that have precisely matched impedance. A resonant synchronous driver can provide an alternative approach to these challenges by using coupled inductors to synchronise the switching events.

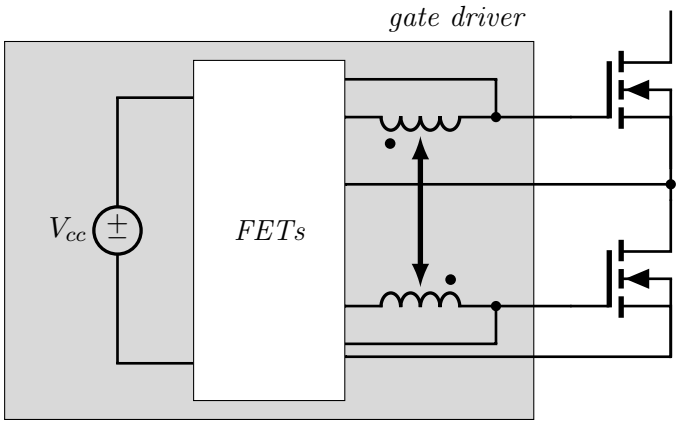


Figure 2.17: Basic idea of a resonant synchronous gate driver shown operating on a half bridge.

2.2.9.1 Resonant Synchronous Driver by Yao et. al.

The driver presented in [68] is a resonant synchronous driver that is shown in Figure 2.18 for a buck converter. The driver consists of five switches and four diodes, as well as a bootstrap diode to provide for a floating voltage source for the high-side switch. The switching transition of a resonant synchronous converter begins by discharging a gate. We will start with S_{bot} on and describe its turning off process. To initiate discharging, S_2 is closed, thereby initiating a current through L_2 that discharges the gate through resonance. The diode of S_5 adopts the inductor current as the gate potential reaches zero. After which S_2 is opened and S_3 is closed; the former interrupts the current through L_2 reflecting a positive current out of L_1 that charges the gate of S_{top}, and the latter enhances the voltage rise using the voltage differential by V_{cc} and clamps the gate during the turn-on state.

When it is time to turn-off S_{top}, S_3 is turned off and S_4 is turned on with ZCS, the latter which discharges the gate through resonance similar to S_{bot}. And similar to the body diode of S_5, D_2 clamps any negative voltage. S_4 is then turned off after allowing leakeage energy to dissipate to have ZCS, which reflects the current. S_1 is simultaneously turned on which compliments th ereflect current and charges S_{bot} to V_{cc}. An active switch S_5 is used

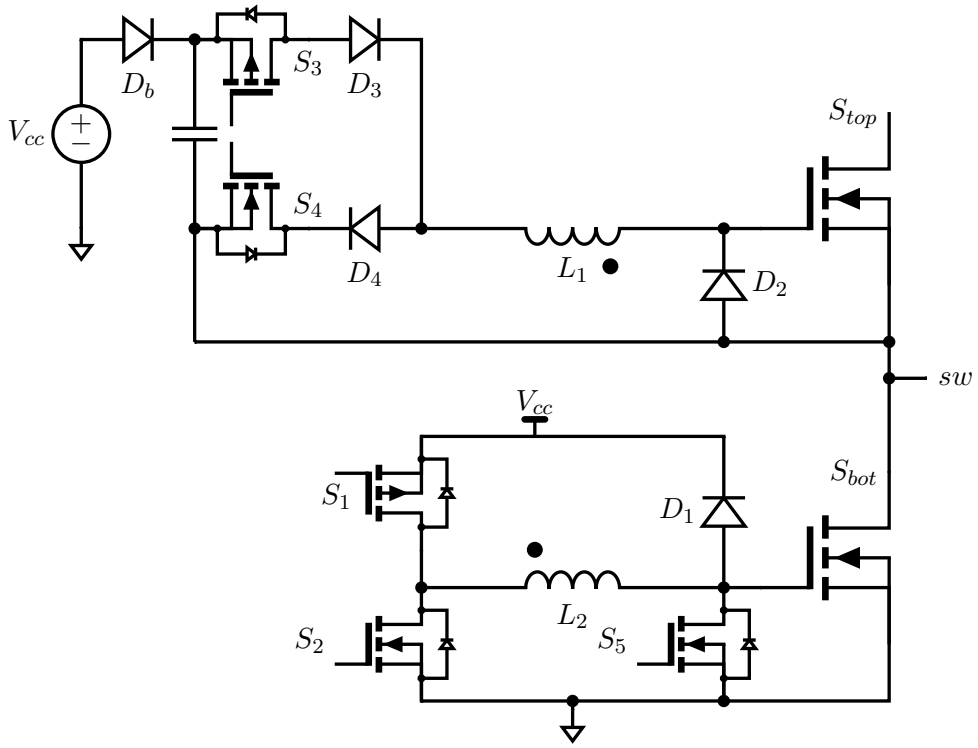


Figure 2.18: Resonant synchronous drive by Yao et al. applied to a half bridge.

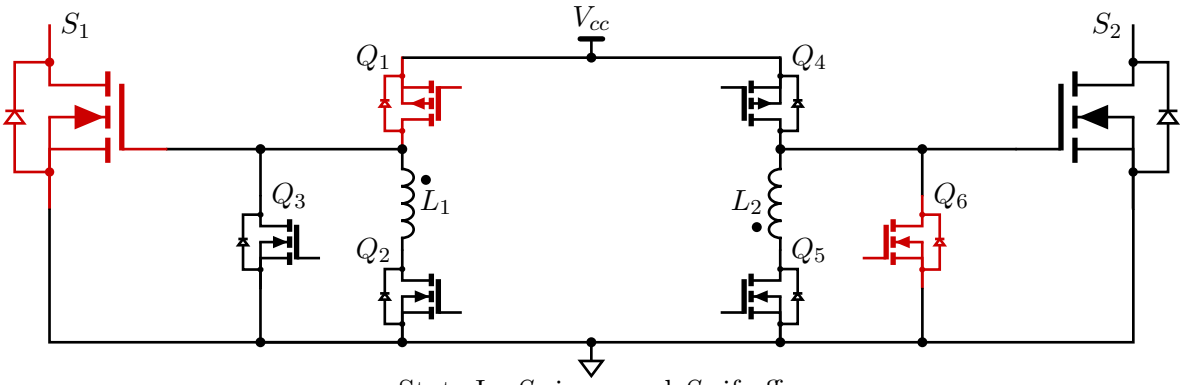
for freewheeling the inductor current of S_{bot} rather than a diode so a low impedance path is provided for the Miller charge.

Chapter 3

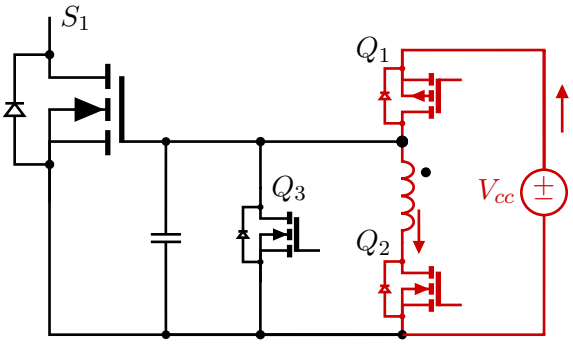
Proposed Driver

3.1 Introduction

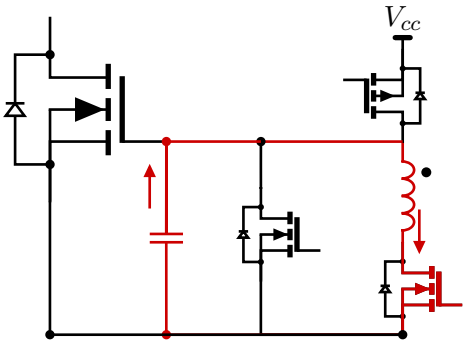
The literature review showed that resonant and current gate drivers can facilitate faster transitions and provide lower switching losses than the conventional totem pole driver. Most of the studies on gate drivers targeted MOSFETs that have substantially higher gate resistance and parasitic capacitance than E-HEMTs, both of which limit switching speed and capacity for gate energy recovery. Therefore it is expected that E-HEMTs have more to gain from current source gate drives. A new kind of resonant synchronous gate driver is introduced, analyzed and demonstrated in this Chapter. The driver operates on two synchronized E-HEMTs as shown in Figure 3.1, and its ideal waveforms are shown in Figure 3.2. Similar to the resonant synchronous driver in [68], the driver uses coupled inductors to reflect a current to create the synchronized switching action. However the proposed driver utilizes only six switches and no discrete diodes, and it is more versatile than the drivers in [68] as well as [63] as it allows for an initial non-zero gate current, thereby allowing fast switching transitions.



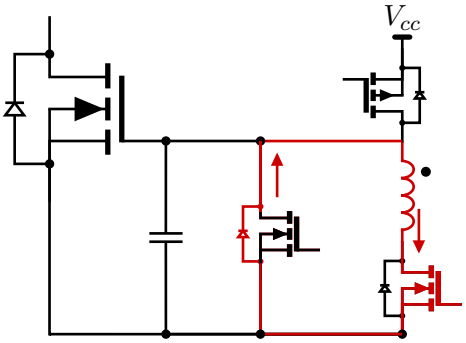
State I - S_1 is on and S_2 if off.



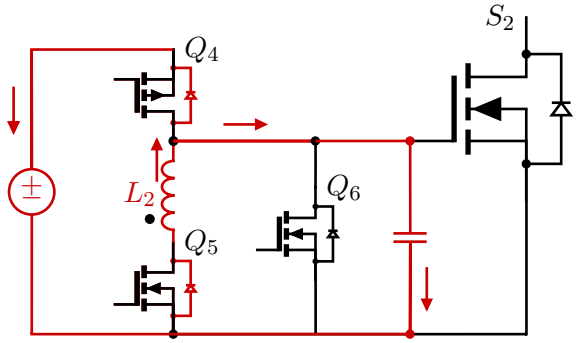
State II - Inductor charging



State IIIa - Gate discharging



State IIIb - Dead time



State IV - Gate charging

Figure 3.1: Proposed current source gate driver. For reference we will refer to S_1 and S_2 as the *power FETs*. Q_1 and Q_4 are referred to as the *high-side* FETs, Q_2 and Q_5 are the *low-side* FETs and Q_3 and Q_6 are the *sourcing* FETs.

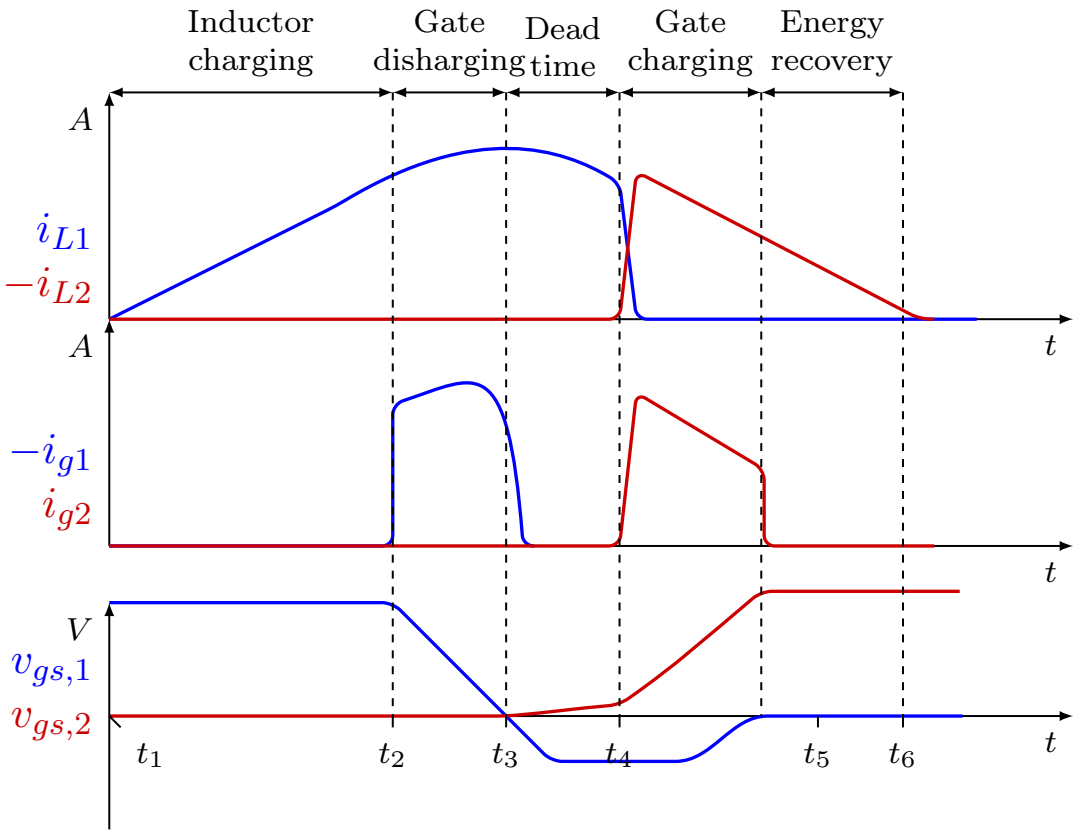


Figure 3.2: Ideal waveforms of the driver's output gate currents and voltage waveforms of the switched gates. The gate discharging and dead time states were enlarged for the sake of the illustration.

3.2 Operating Principle

A description of the driver's steady state operation is provided in this section. Operating states are defined by changes in signals to high-side or low-side FETs, and sub-states describe distinct intra-state changes. The ON state is defined with the left switch S_1 conducting. Below are the states for going from an ON state to an OFF state.

State I During state I, S_1 is on, and S_2 is off. Q_1 and Q_6 are closed/on; the former clamps the gate of S_1 to an optimal turn on voltage V_{cc}, and the latter clamps the gate of S_2 that is off to its source. Q_6 is opened shortly before the switching process begins, preparing

the gate of S_2 to accept charge following the current reflection between the coupled inductors at the end of state III.

State II *Inductor charging* - Q_2 is turned on softly which enables L_1 to be charged from the voltage source with a magnitude of V_{cc}. Current increases linearly at a rate of V_{cc}/L. An increasing current can not be induced between the coupled inductors because of the body diode of Q_5 (and Q_2 during the complimentary state).

State III *(1) Discharging of S_1's gate* - Q_1 is turned off, which diverts the inductor's current to pull charge from the gate of S_1. Given the relatively larger size of the inductor energy vs gate energy, current can be assumed to be constant and so the gate voltage's rate of change is approximately $-i/C_{iss}$ where i is the magnitude of the inductor's current, C_{iss} is S_1's equivalent input capacitance including the output capacitance of Q_3. This sub-state ends when the gate reaches source potential.

(2) Dead-time - Gate voltage continues to decrease until the body diode of Q_3 adopts all of the inductor's current. This sub-state can be referred to as a dead-time and ought to be minimized.

State IV *Charging of S_2's gate* - Q_2 is turned off which collapses the current in L_1. A decreasing current causes the current in L_2 to increase in the opposite direction, which passes through the diode of the complimentary low-side FET, Q_5, thereby charging the gate of S_2 to V_{cc} after which current is diverted to the voltage source thereby recovering the remaining magnetic energy through the diode of Q_4.

State V *Energy recovery, and the off state* - Q_4 is turned on with zero voltage switching as the gate has reached V_{cc}, thereby clamping the gate of S_2 to V_{cc}, and Q_3 is also turned on softly which clamps the gate of S_1 to its source.

State VI *Charging of L_2* - This state is equivalent to state II described above.

State VII *Discharging of S_2's gate* - This state is equivalent to state III described above.

State VIII *Charging of S_1's gate* - This state is equivalent to state IV described above.

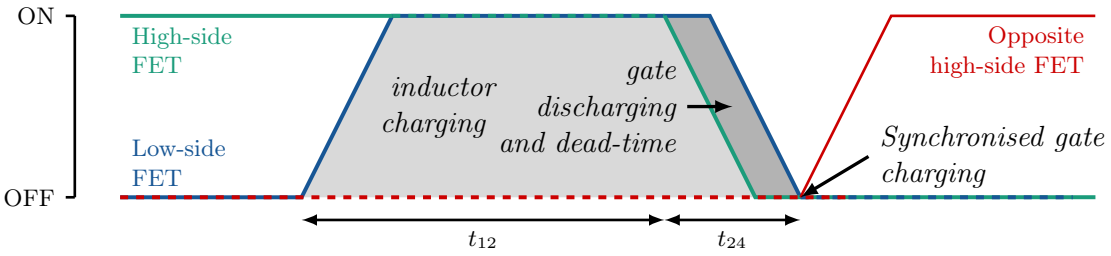


Figure 3.3: Switching activity of the driver's control FETs.

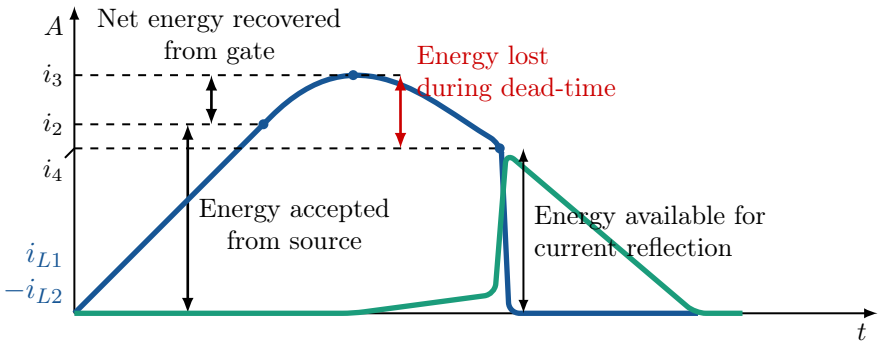


Figure 3.4: Current plot and representation of the energy flow of the driver's coupled inductors.

State IX *Energy recovery and the on-state* - This state is equivalent to state V described above.

3.3 Energy Balance

In this analysis we will use the energy conservation principle to estimate the driver's operating losses and state variables. The parasitic capacitance of the gates is assumed to be constant, which is a more reliable assumption if the driver was operated under ZVS conditions. Nevertheless, time estimates based on gate charge are accurate for as long as it is safe to assume that gate charge is constant [58]. The power FETs are assumed to be identical and all complimentary components are identical.

3.3.1 State II: inductor charging

Q_2 is turned on which initiates the charging of the inductor from the voltage source. The charging current passes through the drain to source resistance of the high-side and low-side FETs, Q_1 and Q_2, as well as the resistance of the inductor as shown in equation in 3.1. During this preset charging interval the system acts as a first order RL circuit with a time constant of L/R_{12}. Because the charging time t_{12} is much smaller than the circuit's time constant, we can assume that the voltage across the inductor remains constant for the period. And so the inductor current i increases linearly at a rate of V_{cc}/L and the current attained after t_{12} is given by equation 3.2. The average inductor current $\overline{i_{12}}$ can be estimated as half the current at t_2, therefore the total losses during state II can be given by 3.3. The energy stored in the inductor at the end of state II is given by 3.4. An increasing current can't be induced in the coupled inductor because Q_5's diode is reverse biased.

$$R_{12} = R_{on(Q_1)} + R_{on(Q_2)} + R_L \tag{3.1}$$

$$i_2 = t_{12} V_{cc}/L \tag{3.2}$$

$$E_{12} = i_2^3 R_{12} L/2V_{cc} = t_{12}^3 \left(V_{cc}/2L\right)^2 R_{12} \tag{3.3}$$

$$E_2 = i_2^2 L_1/2 = \left(t_{12} V_{cc}\right)^2/2L \tag{3.4}$$

3.3.2 State III(1): gate discharging

There are two distinct operating sub-states in this resonating state. This includes III(1): discharging of the gate of S_1 to source potential, and III(2): a dead time period where the inductor current is freewheeling through the diode of the sourcing FET Q_3.

Q_1 is turned off, which initiate the discharging process. The discharging circuit has a resistance made up of the gate resistance R_g as well as R_l and the on resistance of Q_2 as

shown in equation 3.5. During this period, the inductor current continues to increase as it absorbs the electrical energy stored in the capacitor, some of which is lost due to conduction through R_{12}. For the purposes of calculating the discharge time, the inductor's energy gain as well as the energy lost are safely ignored as they are much smaller than the magnetic energy accepted from the voltage source. The time required for the inductor current i_2 to reduce the gate's potential from V_{cc} to source potential is given by equation 3.6, and the energy lost during the gate discharging process is given by equation 3.8. The inductor assumes the balance of the energy during the gate discharge. And so the final magnetic energy can be greater than what was consumed from the voltage source if the energy adopted from the gate E_{iss} - given in equation 3.9 - is greater than what was lost in conduction as shown in equations 3.10 and 3.11. The constant current assumption is reliable considering the large energy differential between the pre-charged inductor and the charged gate. For the application of this driver, we are dealing with a gate with a capacitance of 250 pF, and an inductance of approximately 100 nH. With an inductor current of 1 A, the inductor has $\times 8$ more energy than what is cycled to the capacitor. Using the constant current assumption together with the conservation of energy yielded results with accuracies within 3% of the resonant model.

$$R_{23} = R_g + R_{ds,Q_2} + R_L \tag{3.5}$$

$$t_{23} \approx Q_G / i_2 \tag{3.6}$$

$$Q_G = Q_g + Q_{oss,Q_3} \tag{3.7}$$

$$E_{23} = i_2^2 R_{23} t_{23} = t_{12} V_{cc} R_{23} Q_g / L \tag{3.8}$$

$$E_{iss} = \int^{V_{cc}} C_{iss} v_{gs} \, dv_{gs} \tag{3.9}$$

$$\Delta E_{23} = E_{iss} - E_{23} \tag{3.10}$$

$$E_3 = E_2 + \Delta E_{23} \tag{3.11}$$

3.3.2.1 To pre-charge or not to pre-charge

Notice that the inductor charging state is not critical and the discharging can be begin with a zero initial inductor current. The is done by turning the low-side FET on after turning off the high-side FET, which practically means that the system has no charging time. This is a suitable feature to have considering conduction losses make up a considerable portion of the driver's losses and it can be suitable for ZVS applications that don't have to necessarily be optimized for a minimal transition time. With a zero initial inductor current, we can estimate the time to discharge the capacitor and the energy dissipated during the discharge using equations 3.12 and 3.13, respectively. Note that to assume fully resonant behaviour, the quality factor of the inductor, expressed in equation 3.15, must be greater than five [70].

$$t_{23} = \pi/2 \cdot \sqrt{LC_{iss}} \tag{3.12}$$

$$E_{23} = \left(\frac{R_g}{R_g + Z_o}\right) C_{iss} V^2 \tag{3.13}$$

$$Z_o = \sqrt{L/C} \tag{3.14}$$

$$Q = 2\pi f L / R_{23} \tag{3.15}$$

3.3.3 State III(2): dead time

The timing between the opening of Q_1 and Q_2 determines the time available to discharge a gate. The difference between the time available and the time it actually takes for the gate to reach source potential is defined as a dead time, as given by equation 3.16. Q_3 adopts the inductor current as the gate voltage approaches 0V. We can model the IV loss through the channel of Q_3 by using an equivalent resistance R_D, and so the total resistance is given by equation 3.17. The inductor current at the end of the dead time interval is shown in

equation 3.18 and the energy dissipated is given by equation 3.19.

$$t_{34} = t_{24} - t_{23} \tag{3.16}$$

$$R_{34} = R_{ds,Q_2} + R_D + R_L \tag{3.17}$$

$$i_4^- = i_3 \exp(-t_{34} R_{34}/L) \tag{3.18}$$

$$E_{34} = \int_0^{t_{34}} i_{34}^2 R_{34}\, dt = \frac{L i_3^2}{2} \left(1 - \exp(-2t_{34} R_{34}/L)\right) \tag{3.19}$$

The lower bound on the dead time duration is set by the frequency of the digital clock. For example if it is expected that discharge to occur in 2 ns, but the system can only reliably operate with a clock cycle of 5 ns then the driver is expected to incur 3 ns worth of dead time.

3.3.3.1 Complimentary charging during dead time

A decreasing current can be reflected between the coupled inductors. Therefore, during the dead time the complimentary gate that is soon to be turned on is slowly charged at a rate expressed in equation 3.20, where v_{gs2} is the complimentary gate voltage, k is the coupling coefficient, and C_{iss} is the equivalent input capacitance of the gate. The losses during this event can be ignored.

$$v'_{gs2} \approx \frac{k i_3 R_{34}}{L C_{iss}} \tag{3.20}$$

3.3.4 Post state III(2): negative gate potential

Actions of state III together with those of State IV incur three types of losses during t_{45}. The two losses in the original leg connected to S_1 are denoted as A1 and A2 and the loss in the second leg is denoted as B1, and thir sum is given by equation 3.21.

$$E_{45} = E_{45(A1)} + E_{45(A2)} + E_{45(B1)} \tag{3.21}$$

As shown in Figure 3.2, any amount of dead time will lead to a negative potential at the gate which will ultimately be dissipated through resonance. If we assume that dead time is long enough to allow for gate to settle at the forward negative voltage of the sourcing FET then the additional losses for the discharged gate are:

$$E_{45(A1)} = C_{iss} V_F^2 / 2 \tag{3.22}$$

Where V_F is the source to drain voltage of the sourcing E-HEMTwith the freewheeling current i_3. For E-HEMTs the reverse voltage is about 2 V for a current on the order of 1 A. Any negative potential in the gate has to be dissipated through the diode before the sourcing HEMTis turned on, otherwise the HEMTwill incur switching losses when it is turned on.

3.3.5 State IV: leakage energy

Q_2 is opened, which interrupts the current in L_1. This causes a negative di/dt that induces current to flow out of L_2 with strength determined by the coupling coefficient. i_4^- is the current in L_1 before opening Q_3, k is the coupling coefficient and i_4^+ is the equivalent current transmitted to the coupled inductor after opening Q_3 as expressed in 3.23. The energy that is not transmitted to the coupled inductor is dissipated through resonance and is given by equation 3.24.

$$i_4^+ = -k \int_0 \frac{di_4^-}{dt} dt = k i_{4^-} \tag{3.23}$$

$$E_{45(A2)} = (1 - k^2) L i_{4^-}^2 \tag{3.24}$$

3.3.6 State IV: charging of complimentary gate

The current flowing through the inductor is passing through the diode of the low-side FET Q_5 and can charge both the gate of S_2 as well as the voltage source as illustrated in Figure

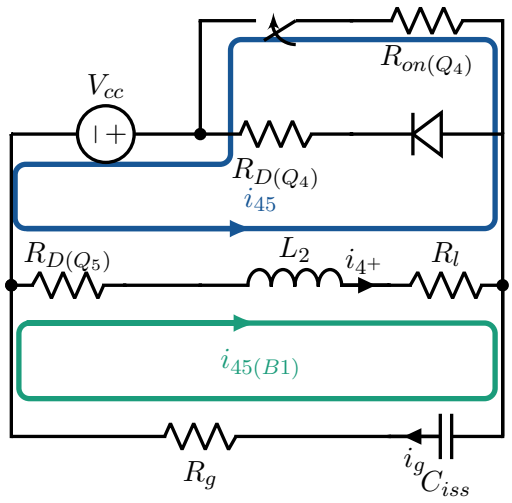


Figure 3.5: State IV circuit model showing charging of the complimentary gate and voltage source.

3.5. The current initially flows through the gate thereby charging it to V_{cc}. The current path is through the gate, L_2 and the diode of Q_5, the latter which will be modelled as a resistance as shown in equation 3.25. The time required for the gate to reach V_{cc} is given in equation 3.26. Because we are charging the capacitor, the inductor current decreases during this period as it transmits energy to the gate, not withstanding conduction losses that are incurred. In the discharging case, the conduction losses offset the energy gained from the gate. In case of charging both the gate and conduction losses reduce the inductor's energy. To obtain a better approximation of the the average inductor current, we can consider the inductor's energy as the average with and without the gate energy as shown in equations 3.27 and 3.28. The remaining magnetic energy after charging the gate to V_{cc} is given by

equation 3.29.

$$R_{45(B1)} = R_g + R_l + R_{D(Q_5)} \tag{3.25}$$

$$t_{45(B1)} \approx Q_G / i_4^+ \tag{3.26}$$

$$\overline{i_{45}} = \sqrt{(2E_4^+ - E_{iss})/2L} \tag{3.27}$$

$$E_{45(B1)} = \overline{i_{45}}^2 \cdot R_{45(B1)} \cdot t_{45(B1)} \tag{3.28}$$

$$E_5 = E_{L,4^+} - E_{iss} - E_{45(B1)} \tag{3.29}$$

3.3.7 State V: recovery of remaining energy

When the gate reaches V_{cc}, Q_4 is turned on softly, and the remaining current flows through its channel thereby recovering the remaining magnetic energy. The conduction resistance for this sub-state is given in equation 3.30, and the behaviour is of a clamped first order RL circuit with a forced DC input. Such a circuit would have a current response as shown in equation 3.31. The charging process is complete when the diode of Q_5 no longer reverse biased as shown in equation 3.32. Setting equation 3.31 to zero yields the duration shown in equation 3.33. Using the expression for current we can multiply by the conduction resistance and integrate to yield the lost energy as shown in equation 3.34 where i_5 is the inductor current at the end of gate charging.

$$R_{56} = R_{D(Q_5)} + R_L + R_{on(Q4)} \tag{3.30}$$

$$i_{56} = \frac{-V_{cc}}{R_{56}} \cdot \left(1 - \exp\left(-(L/R_{56} \cdot t)\right) + i_5 \cdot \exp\left(-(L/R_{56}) \cdot t\right)\right. \tag{3.31}$$

$$i_{56} > 0 \tag{3.32}$$

$$t_{56} = \frac{L}{R_{56}} \cdot \ln\left(\frac{V_{cc}/R_{45(B2))}}{i_{45(B1^+)} - V_{cc}/R_{45(B2))}}\right) \tag{3.33}$$

$$E_{56} = L i_5^2 \left(1 - \exp(-2t_{56}L/R_{56})\right)/2 \tag{3.34}$$

3.3.8 High-side clamping delay

The driver's control signals ought to be scheduled such that the the converter's losses are minimized, including both drive and power losses, as illustrated in Figure 4.4. There are also some qualitative issues to consider. For example, in our analysis we assumed that the turn-on of the high-side switch happens at the same time the gate reaches V_{cc}, which allows for ZVS and no reverse recovery loss. However given control signals are operated in discrete time steps and GaN devices are extremely fast, ZVS may not be achievable or worse, a gate voltage overshoot can occur due to the large voltage differential across the diode of the high-side FET. The only practical and safe option to preventing a voltage overshoot may be to turn on the opposite high-side FET the same time the inductor current is to be transferred to the gate. While this will incur a hard switching loss, it will avoid damaging the gate which would have a detrimental consequence on the gate's operation. Nevertheless, from the principle of conservation of energy we know that the magnetic energy will still be recovered as described above. For the following simulation, a constant 2 ns delay is inserted between the opening of a low-side FET and the opening of its complimentary high-side FET.

3.3.8.1 Reverse recovery charge

If the high-side FET is a MOSFET as shown, then it will incur a reverse recovery charge if the switch is turned on with a current present in the body diode. In other words, reverse recovery losses are incurred if the gate voltage goes beyond V_{cc}, and are avoided if the high-side switch is turned on under ZVS or even with hard switching as long as the gate voltage does not exceed V_{cc}.

Chapter 4

Driver Evaluation

4.1 Class E Inverter

The proposed driver can be applied to any pair of synchronous FETs, including those in a half bridge or push-pull configuration. A push-pull Class E inverter was selected to demonstrate the proposed gate driver, which acts as an inverter that supplies a coil that transmits power through magnetic resonant coupling to a receiver coil, which is connected to a rectifier as shown in Figure 4.1.

A Class E inverter belongs to a family of power amplifiers in the RF communication industry used in high frequency power amplification [71]. The class E inverter has an ideal switching efficiency of unity and is therefore an attractive candidate for power applications including dc-dc conversion and wireless power transfer [72, 71, 73]. GaN HEMTs are excellent candidates for power amplifiers because of their high linearity and low parasitic capacitance and several studies have proven their superior performance over silicon [74, 75, 76, 77, 78]. Several studies have also investigated the performance of GaN devices for WPT utilizing Class E inverters [79, 80, 81].

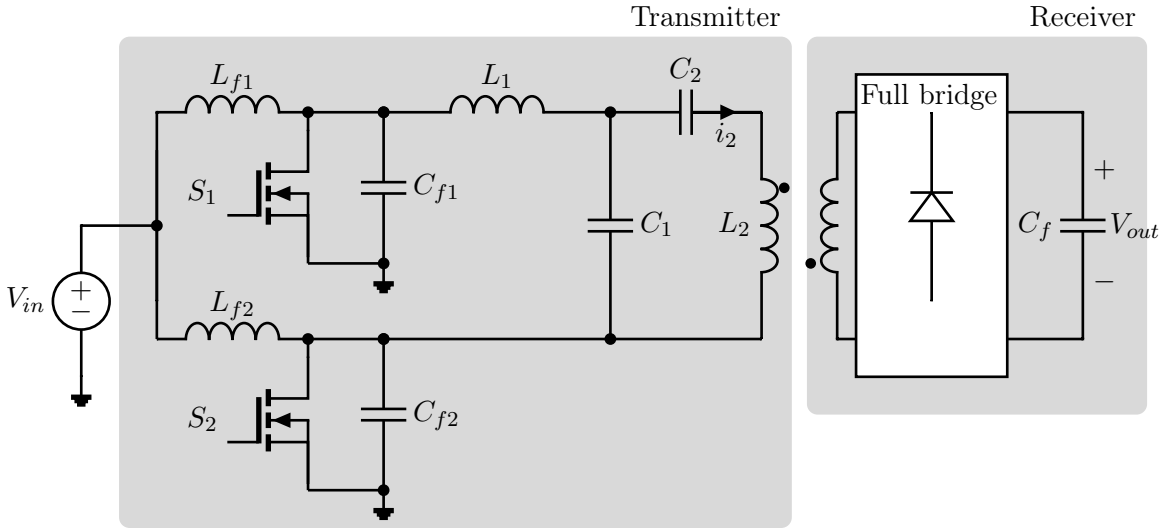


Figure 4.1: Push-pull Class E inverter circuit used to demonstrate proposed driver.

4.1.1 Operation

A Class E inverter can be thought of as an AC current source that is tuned with a series resonant LC filter [82]. A current develops in the input inductor L_f when the switch is closed, and when opened the inductor current resonates with the parallel capacitor C_f causing voltage to ideally peak to to $3.56V_{in}$ before it returns to zero with a zero slope as shown in Figure 4.2[82]. Therefore while Class E inverters allow for lower losses, they still require high power devices that can withstand their peak drain-source current and voltage values. Installing two amplifiers in parallel offset by 180° is referred to as a push-pull circuit, and it allows a doubling of the AC output and odd order harmonics are avoided [83]. And by adding a capacitor between the outputs of a push-pull the RMS current through the switches is reduced [73]. Having a finite input inductance enables ZVS conditions across a wide load range without requiring closed loop control [84]. However a lower inductance means larger AC current through the input inductor which increases losses and EMI issues [79]. The first loop L_1C_1 acts as an output filter for the inverter, and the second filter L_2C_{2eq} acts as an input filter to the transmitter, and their frequencies are turned to the fundamental as shown

in equations 4.1 and 4.2. The ideal switching waveforms of a single Class E amplifier are shown in Figure 4.2.

$$\frac{1}{\omega^2} = L_1 C_1 = L_2 C_{2eq} \tag{4.1}$$

$$C_{2eq} = C_1 C_2 / (C_1 + C2) \tag{4.2}$$

.

4.1.2 Design parameters of a Class E inverter

The design equations of a Class E amplifier can be expressed in an infinite number of ways as the values of the input inductance and the converter's duty cycle are not defined [85]. A comprehensive analysis of a push-pull Class E amplifier operating with a 50% duty cycle is provided in [86]. The optimal operating setting for a Class E inverter includes ZVS turn-on as well as zero voltage derivative switching (ZVDS) turn-on, and the design includes the selection of the size of the reactive components given a resonant frequency. Its modelling assumptions include [84]:

1. The converter experiences no conduction losses including the power FETs which also have no dead time or dead time losses. All the DC input is converted into an AC output as shown in equation 4.3. This assumption will require tuning of the circuit.
2. FET output capacitance is constant, which is fair considering the required capacitance is typically much larger for frequencies $<$1 MHz.
3. Output (transmitter) voltage is sinusoidal, requiring a sufficiently high output impedance compared to the load as shown in equation 4.4. I_R is the amplitude of the output current, R is the output resistance, I_{DC} is the input current DC offset, and V_{in} is the

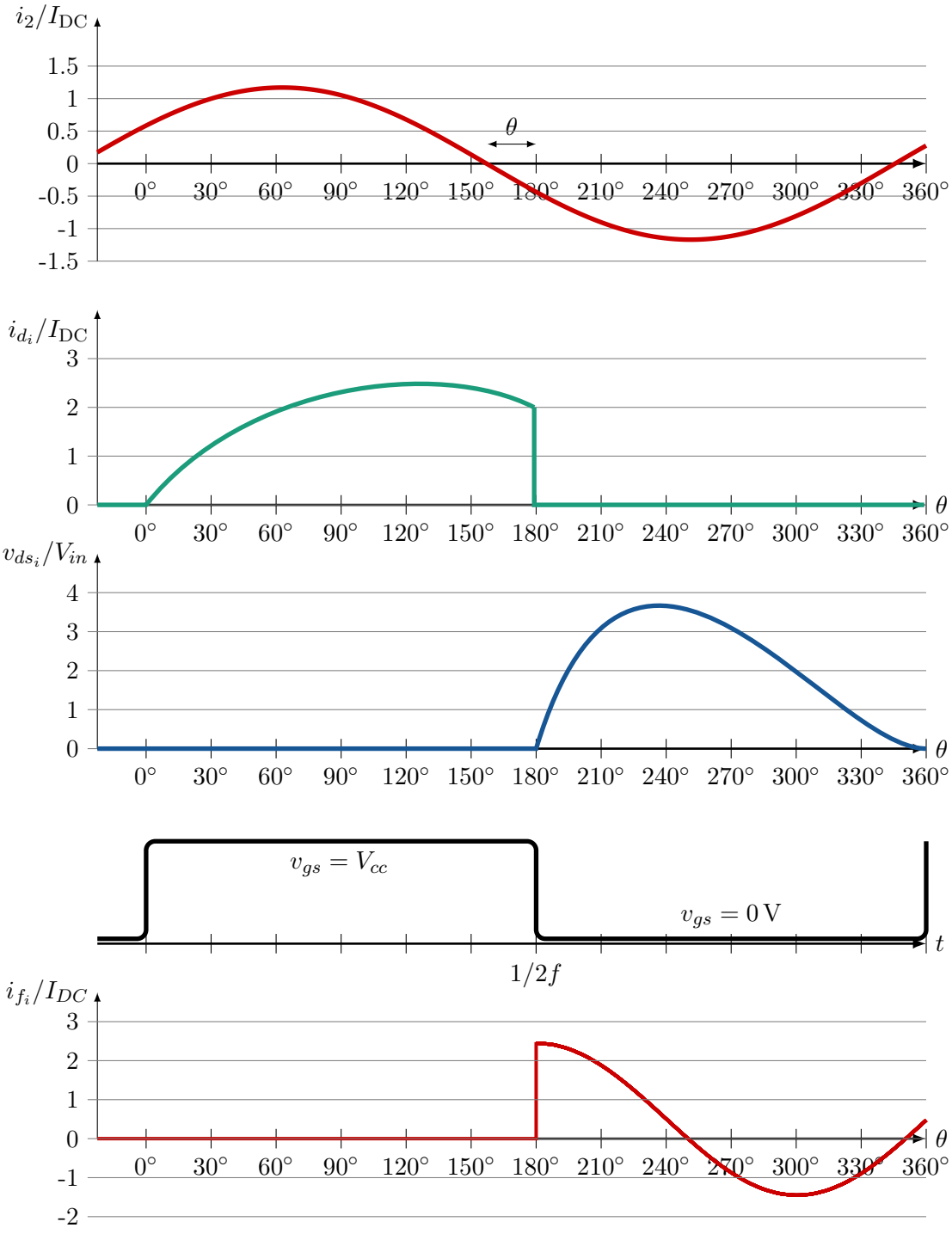


Figure 4.2: Normalised waveforms of a push-pull Class E inverter satisfying both ZVS and ZVDS. The ideal class waveforms are for a purely resistive load i.e. no magnetic coupling or DC rectification.

voltage magnitude of the supply.

$$I_R^2 R/2 = I_{DC} V_{in} \tag{4.3}$$

$$i_R(\omega t) = I_R \sin(\omega t - \phi) \tag{4.4}$$

The solutions with a duty cycle of 50% are shown in equations 4.5, 4.6, and 4.7.

$$k_L = \omega L_f / R = 0.732 \tag{4.5}$$

$$k_C = \omega C_f R = 0.685 \tag{4.6}$$

$$k_P = P_{out} R / V_{in}^2 = 1.365 \tag{4.7}$$

Equation 4.7 suggests that there are only two free design variables between the output resistance, input voltage and output power. Therefore if all three variables are pre-determined by the application it will lead to sub-optimal operation which may still include ZVS.

4.1.3 Coupling and transfer efficiency

Wireless power transmission happens through magnetic resonance between a transmitter and receiver coils. The figure of merit for the coils is given by equation 4.8, where k is the coupling coefficient between the receiver and transmitter [87]. The closer the coils are together, the more k approaches unity. The receiver and transmitter provide an opportunity for voltage transformation through their turns ratio. The magnetizing inductance is given by equation 4.10 and the output capacitance required to provide a DC output with a ripple

20W solar PV tile Transmitter and receiver	
Input at STC	
Open circuit voltage	19.7 V
Short circuit current	1.5 A
Maximum power point voltage	17.2 V
Maximum power point current	1.2 A
Maximum power	20 W
Tx: 1 MHz Push-pull Class E inverter Reactive components as per Figure 4.1	
L_{f1}, L_{f2}	2.6 µH
C_{f1}, C_{f2}	4.7 nF
L_1	3.3 µH
C_1	7.75 nF
C_2	5.75 nF
C_{dc}	10 nF
Magnetizing inductance L_{r4}	8 µH
Tx:Rx turns ratio	1.45

Table I: Demonstration board's main parameters.

$V_{pp,out}$ is given by equation 4.11 [87, 88].

$$\text{FOM} = k\sqrt{Q_t \times Q_r} \tag{4.8}$$

$$Q = \omega L/R \tag{4.9}$$

$$L_M = k\sqrt{L_1 L_2} \tag{4.10}$$

$$C_{dc} = \frac{I_{out}}{2f\Delta V_{pp,out}} \tag{4.11}$$

Driver FET	Partno	V_{ds}^{max}	$R_{ds(on)}$	Q_g	C_{iss}	Die area
Lowside and sourcing	EPC2110(Q_1 and Q_2)	120 V	110 mΩ	0.8 nC	100 pF	1.83 mm^2
Highside	CSD25480F3	20 V	132 mΩ	0.7 nC	150 pF	0.47 mm^2
Power FET	EPC2019	200 V	50 mΩ	1.8 nC	250 pF	1.82 mm^2

Table II: Main parameters of selected FETs.

Component	Description
S_1 and S_2	E-HEMT 200 V, 10 A EPC2019 by EPC
Q_1 and Q_4	CSD25480F3 by TI. Silicon depletion mode pmos.
Q_2 and Q_3	EPC2110 by EPC. Two E-HEMTs in a single die with their sources connected together.
Q_5 and Q_6	EPC2110 by EPC .
L_1 and L_2	CoilCraft SLC7530 100 nH coupled inductor with signal isolation of 25 V, DCR 0.125 mΩ.

Table III: Driver components selected for the demonstration board.

4.1.4 Solar wireless power transfer

Solar PV technology allows the direct conversion of sunlight into an electrical current and has been in exponential growth around the world since 2009. PV cells are electrically and structurally combined into PV modules that are interconnected using robust connectors. DC wiring equipment including connectors, disconnects, and their associated mechanical fittings, are the main culprits in solar failures including fires and the cause of spurious arc-fault system tripping [89, 90, 91, 92, 93]. It is expected that wireless charging can minimize or avoid risk associated with modular DC wiring and the system's installation cost by eliminating the need for an interconnecting bus cable as illustrated in Figure 4.3. A demonstration board was created to demonstrate the transmission of 20 W from a solar tile and the selected FETs are shown in Table III. To reduce parasitic inductance, EPC2110 was selected to host a leg's low-side FET and sourcing FET. This allows for a compact design around the power switch, and a minimal inductance between the low-side and sourcing FET, which ensures that the

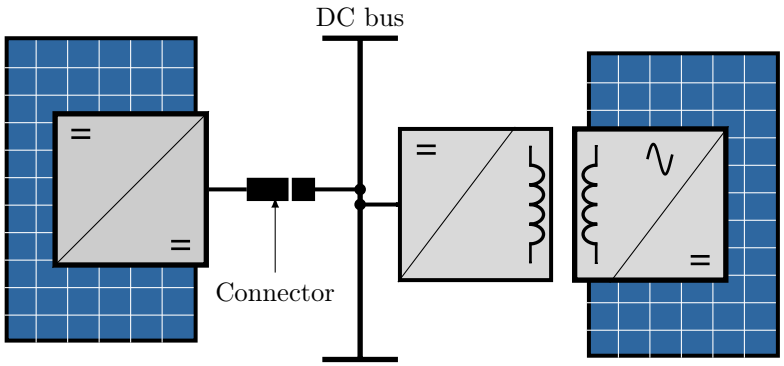


Figure 4.3: A single line diagram sketch of an interconnection of PV modules to a DC bus. The module on the left is wired to the bus using conductors and connectors and the one on the right transmits its power to the DC bus by magnetic coupling using a transmitter, receiver and a rectifier.

gate's voltage does not considerably fall below 0 V. 3D models of the demosntration board are shown in Figure- 4.8, 4.9 and 4.10.

4.2 Simulation Results

A simulation of the circuit was completed in PSIM software which uses static FET parameters to model switching behaviour. A 50 ps time step was used for all simulation results. The impact of assuming a constant input capacitance is negligible considering the switches are operating with ZVS. A model of the power circuit was built as shown in Figure 4.1. The driver and the power circuit's parameter are given in Table I, II, and III. The driver's charging and discharging times were manipulated to find minima in driver and channel losses as illustrated in Figure 4.4. The gating losses incurred by a conventional totem pole driver is shown in equation 4.12 and is drawn on each plot in Figure 4.5, which displays the results of the charging and discharging sweeps.

$$2fC_{iss}V^2 = 2 \times 1\,\text{MHz} \times 250\,\text{pF} \times (5\,\text{V})^2 = 12.5\,\text{mW} \tag{4.12}$$

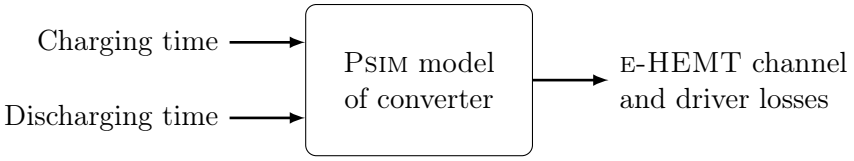


Figure 4.4: Main gate design variables are sweeped using PSIM to determine the optimal design parameters that reduce the system's losses.

The charging and discharging durations were sweeped and the E-HEMT channel and driver losses were observed. The observed driver losses shown in Figure 4.5 are measured by integrating the current through V_{cc}, and this includes all the losses including inductor's conduction losses, dead time, switching losses, negative gate voltage and leakage energy. The only losses not considered are the gating losses of the control switches which are driven by a conventional driver and will therefore incur their own gating losses as shown in equation 4.13. Table IV shows the breakdown of losses of the optimal case[1]. Figure 4.6 displays the waveforms with the optimal settings at nominal conditions as well as with an output resistance 1000 times greater than nominal to emulate open circuit conditions. p_i, n_i, and g_i where $i = \{1, 2\}$, refer to the gate-source voltage of the high-side FET, low-side FET and sourcing FET, respectively. Wide waveforms are provided in Figure 4.7.

$$2f \sum C_{iss}^{driver} V^2 = 2 \times 1\,\text{MHz} \times 2 \times 250\,\text{pF} \times (5\text{V})^2 = 25\,\text{mW} \tag{4.13}$$

[1]If an activity incurs E nJ losses per cycle, which are assumed to be independent of other cycles, then it will incur E mW per MHz of the switching frequency.

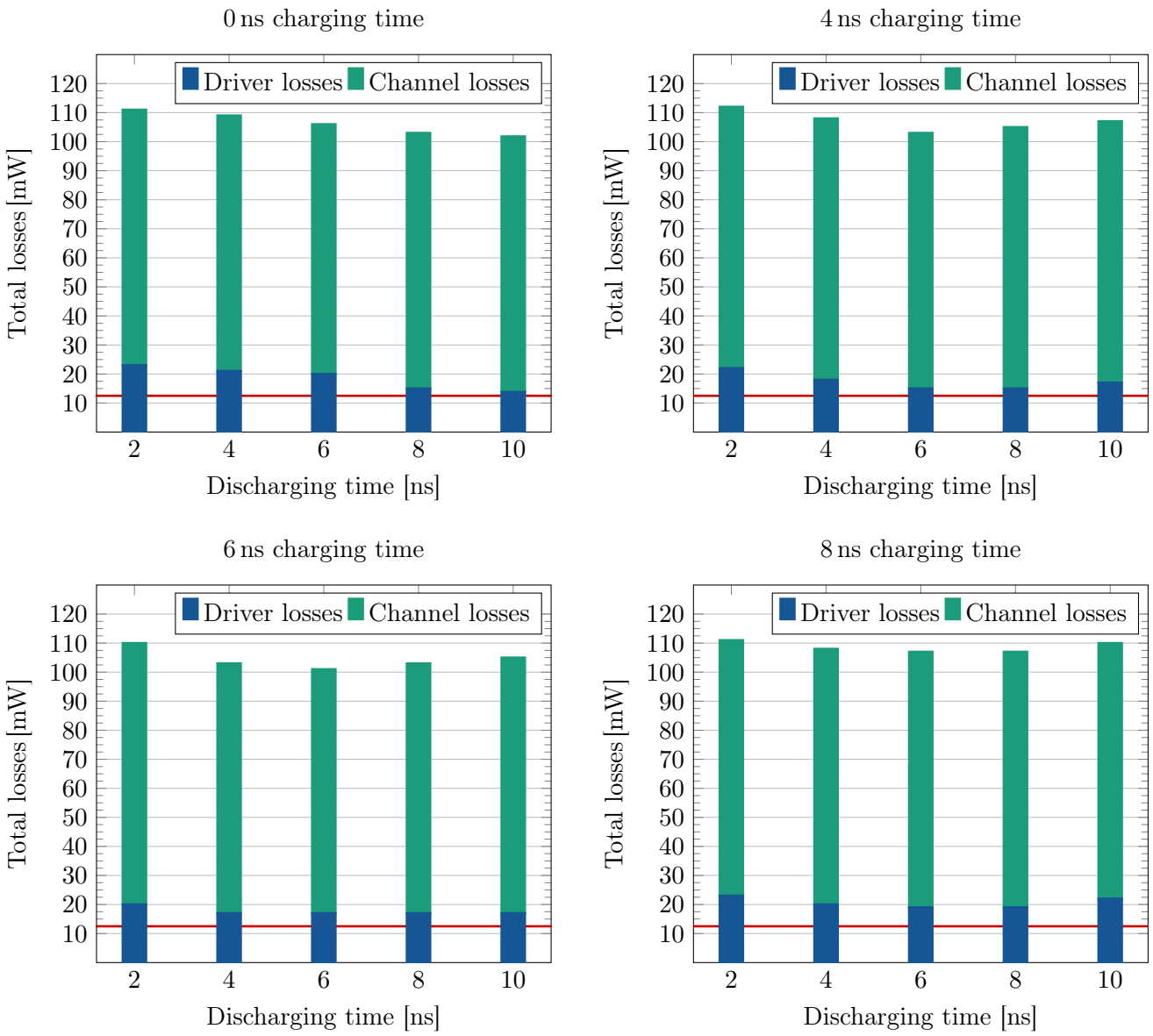


Figure 4.5: Channel and driver losses with respect to charging and discharging times during nominal operating conditions.

Low-side channel losses	3.5 mW
High-side channel losses	+2.4 mW
Gating and sourcing channel losses	+1 mW
Leakage losses	+0.1 mW
Inductor conduction losses	≈ 0 mW
Leg losses	= 6.9 mW
Driver losses, ×2 leg losses	13.8 mW

Table IV: Breakdown of driver losses with optimal charging and discharging durations of 0 ns charging time and 10 ns, respectively.

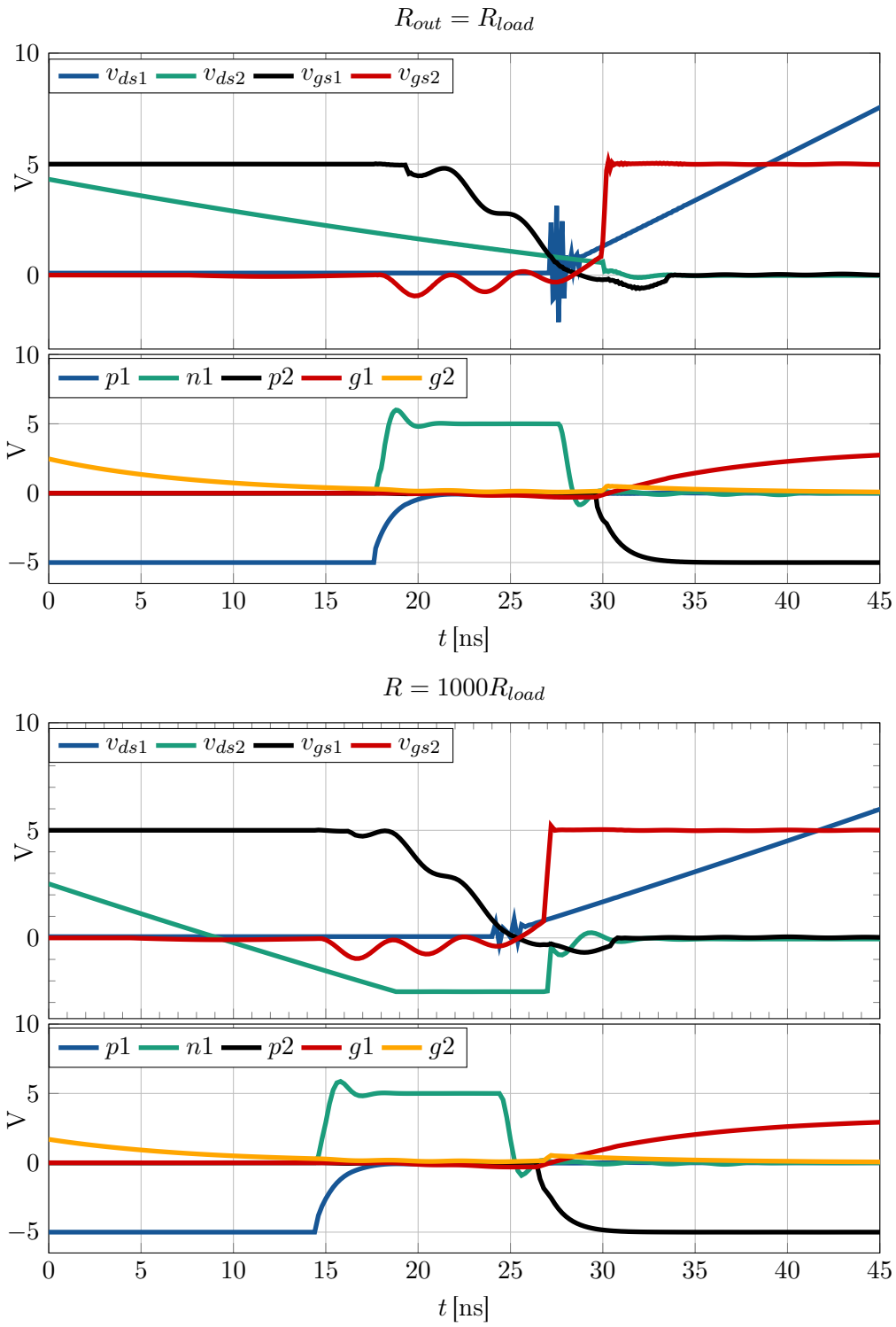


Figure 4.6: Drain and gate voltages of optimal settings with 0 ns charging time and 10 ns discharging time.

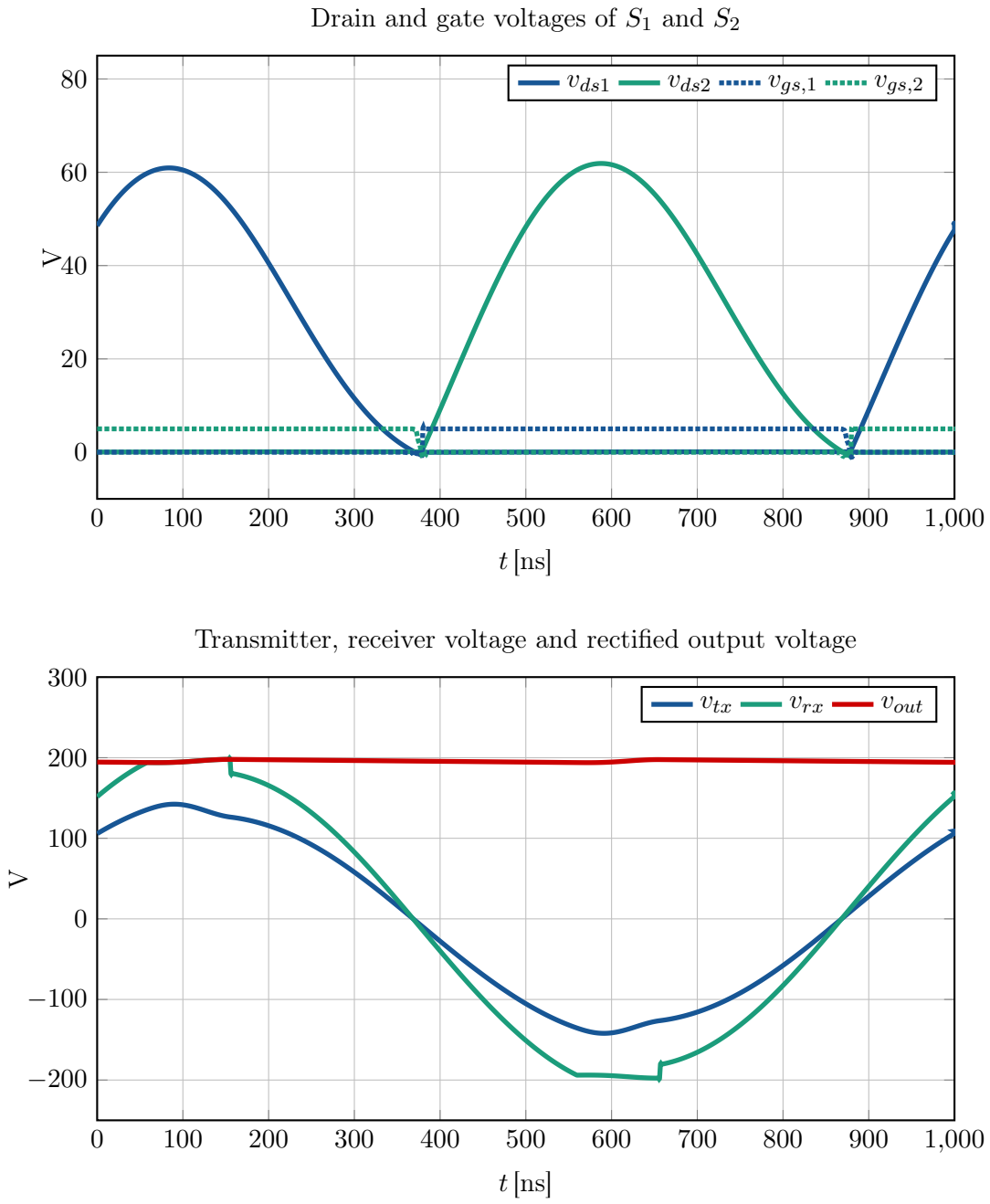


Figure 4.7: Simulation waveforms of nominal operation including drain voltages, transmitter and receiver voltages.

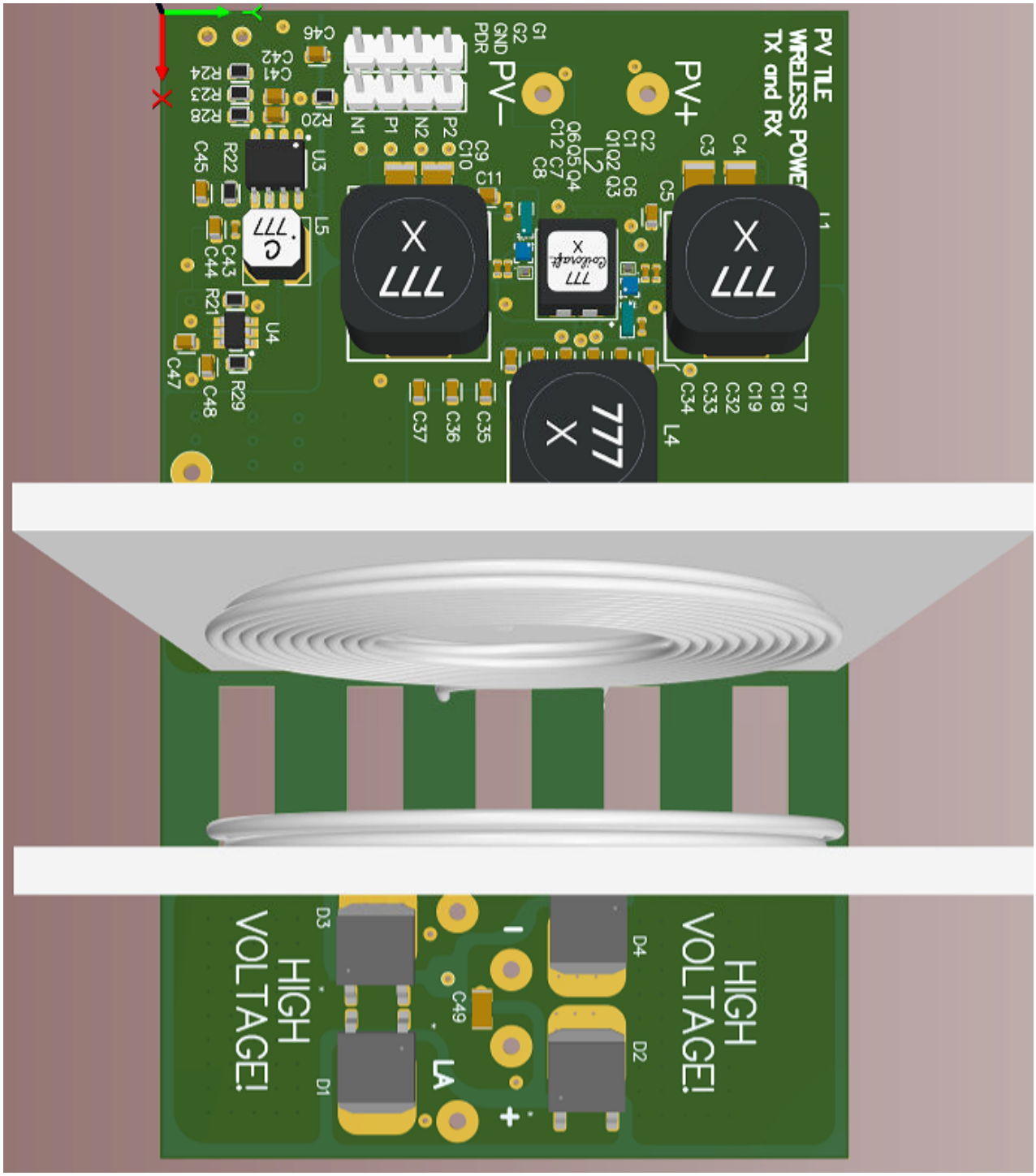


Figure 4.8: Top far view of demonstration board, 100 mm×60 mm

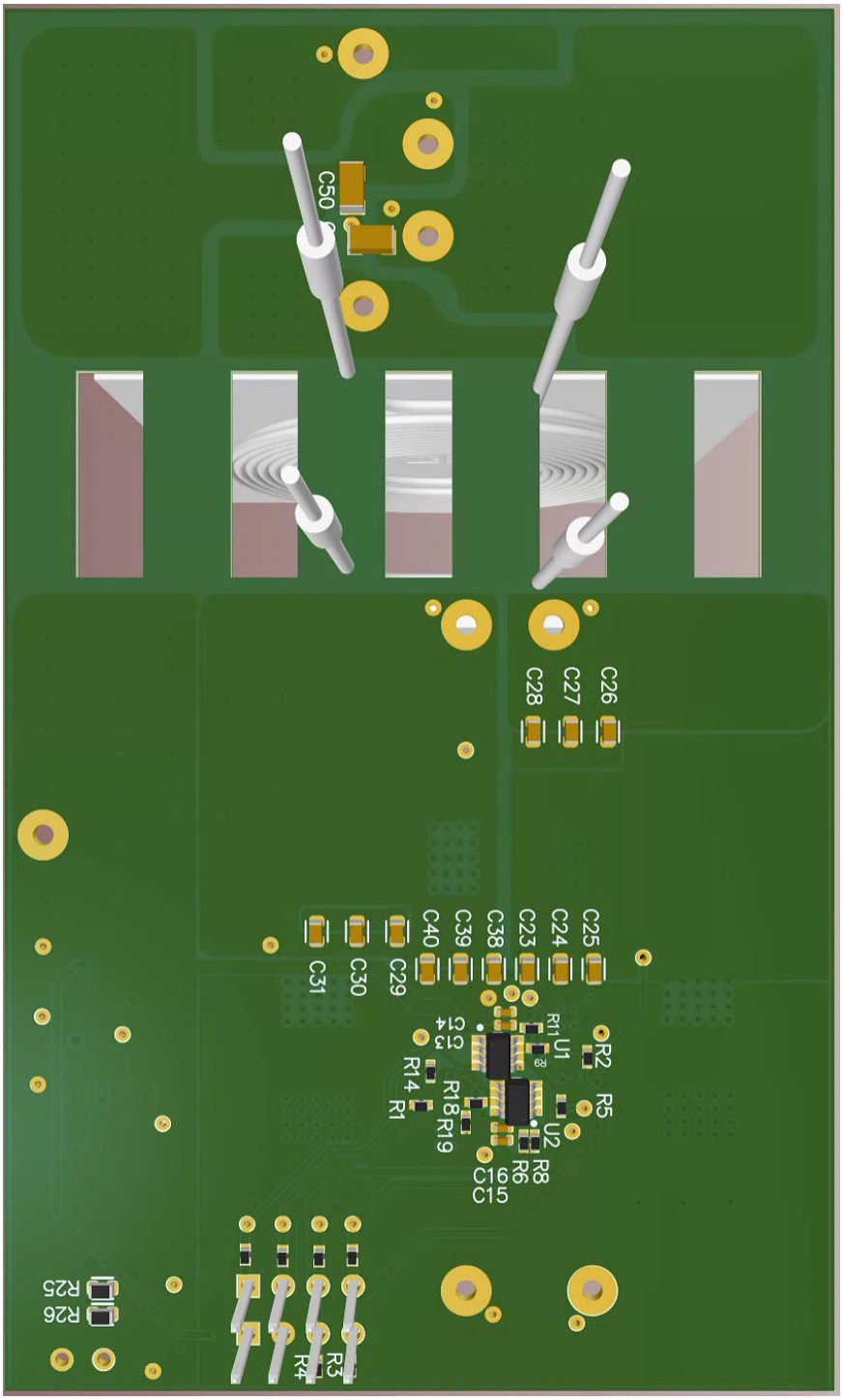


Figure 4.9: Bottom far view of demonstration board.

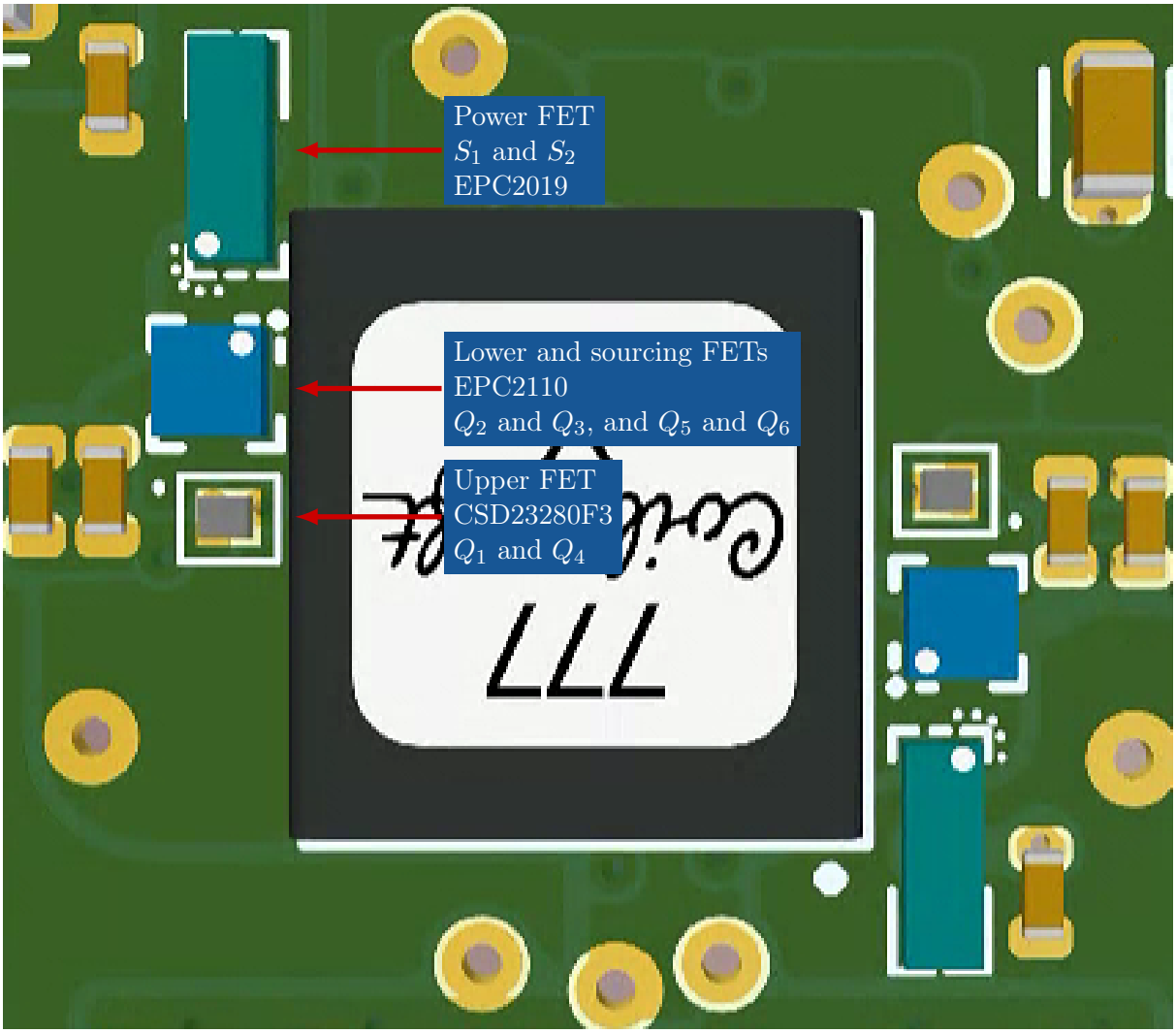


Figure 4.10: Top close up view of gate driver.

4.3 Conclusion

The proposed resonant synchronous driver was proven to provide reliable switching and gate energy recovery. Channel losses are weakly dependant on the driver charging and discharging durations, and no clear global minima in channel losses was found when sweeping charging and discharging durations. This is expected given the switches operate with ZVS switching. The converter still experiences ZVS with no load conditions and without any closed loop control. However the drain voltage no longer experiences ZVDS and a negative voltage incurs reverse conduction loss, which increases channel losses by 10 mW or 25%.

Not pre-charging the inductor yielded the lowest driver losses. This is because pre-charge conduction losses make up a considerable part of the overall losses and their biggest impact is on minimizing hard switching channel losses which is not possible with ZVS. In the results of Figure 4.6 we can see that starting with a zero initial inductor current and allowing the inductor to discharge the gate for 10 ns, allowed all of the energy to be adopted under resonant dynamics and incurred essentially no dead-time. A longer discharging duration will have dissipated more of the absorbed energy, leading to greater losses. Note that the voltage source provides the balance of the gate energy required through the high-side FET, and so the driver losses include the gating power required to charge the gate. In Table IV we can see that the energy flowing to the drain of the sourcing FET and to the power gate is 1 mW, which suggests that approximately (1mW/(12.5mW/2)) 86% of the gate energy is recovered and transmitted from one gate to another.

The low-side FET dissipates about 50% more energy than the high-side FET despite them having similar on resistances. This is because a large portion of the losses in the low-side FET are incurred during reverse conduction when the complimentary gate is being charged. Turning on the low-side FET during the complimentary charging states can reduce this loss but it will double its operating frequency which will double its hard switching losses.

Chapter 5

Conclusion

Faster and more efficient gate drivers are required to facilitate the next generation requirements of high speed synchronous switching of GaN E-HEMTs. A review of the dynamics and challenges of hard switching of E-HEMTs with the conventional totem pole gate drive justified the need for another approach to driving GaN devices. Current source gate drivers have the capacity of providing faster and more efficient operation that can further take advantage of the superior switching performance of GaN E-HEMTs. A baseline was created to compare the performance of current source drivers with the conventional driver, and a review of prominent current and resonant drivers was provided. A novel resonant synchronous gate driver was introduced and demonstrated to provide energy recovery and stable switching waveforms in a push-pull ZVS application with a switching frequency of 1 MHz.

5.1 Future Work

1. Investigate whether doubling the frequency of the low-side FETs to enhance the channel during the complimentary charging states will lead to improved driver performance.
2. Explore adaptive control techniques that tune the driver's parameters and inverter's frequency to minimize reverse conduction losses during dead-time.

3. Explore the ways a solar's power-voltage curve can be manipulated to satsify ZVS and ZVDS.
4. Replace the high-side depletion-mode MOSFET with an E-HEMT, which will have a considerably faster response and lower losses. This will considerably improve the switching performance especially for applications that have optimally high gate currents, such as in the hard switching half bridge topologies.
5. Apply the driver to a half-bridge hard switching topology. By pre-charging the inductor the driver is expected to significantly reduce the channel load losses, enabling a more efficient high frequency operation. Furthermore, the sourcing FET can rectify the drain-gate charge that is induced during the high speed drain voltage transient. It can do this as described in this thesis by providing a low impedance path through its channel, or by stretching the driver's dead-time period to allow the synchronous FET to accumulate a low enough negative voltage to offset the expected drain charge.

Appendix A

First and second order models

A.1 Inductor current in LC Model

$$V_{cc}(s) = sLi - Li_0 + Ri \tag{A.1}$$

$$i(\mathbf{s}) = \frac{LI_0 + V_{cc}}{\mathbf{s}L + R} = I_0 \exp(-R/Lt) \tag{A.2}$$

Inverse laplace:

$$i(t) = I_0 \exp(-Rt/L) + L^{-1}\left[\frac{V_{cc}}{\mathbf{s}L + R}\right] \tag{A.3}$$

A.2 Natural Response

The series RLC model is frequently encountered in the thesis. Below is a description of the RLC model with an initial inductor current and capacitor voltage. A KVL around the RLC circuit yields,

$$v_L + v_C + v_R = 0 \longrightarrow L\frac{di}{dt} + v_c + iR = 0 \tag{A.4}$$

Dividing by L, and substituting charge $q = Cv_c = di/dt$,

$$q'' + \frac{q}{LC} + \frac{R}{L}q' = 0 \tag{A.5}$$

Converting everything into the Laplace domain. The Laplace of inductor voltage is $v_L(\mathbf{s}) = L(\mathbf{s}i(\mathbf{s}) - i(0))$.:

$$\mathbf{s}^2 q(\mathbf{s}) - \mathbf{s}q(0) - q'(0) + \frac{q(\mathbf{s})}{LC} + \frac{R}{L}(sq(\boldsymbol{s}) - q(0)) = 0 \tag{A.6}$$

Rearranging for $q(\mathbf{s})$)

$$q(\mathbf{s})(\mathbf{s}^2 + R\mathbf{s}/L + 1/LC) - q(0)\mathbf{s} - q'(0) - \frac{R}{L}q(0) = 0 \tag{A.7}$$

Dividing by C to obtain v_c.

$$v = \frac{q}{C} = \frac{1}{C}\frac{q(0)\mathbf{s} + q'(0) + Rq(0)/L}{\mathbf{s}^2 + R\mathbf{s}/L + 1/LC} \tag{A.8}$$

Where $i_0 = q'(0)$ and $v_0 = q(0)/C$

A.2.1 Forced response of series RLC

The RHS of the previous equations will now equation some input $\frac{V_{in}(t)}{L} \rightarrow \frac{V_{in}(\mathbf{s})}{L}$. If we assume the input is a DC source, then $v_{in}(\mathbf{s}) = V_{in}/\mathbf{s}$ where V_{in} is the magnitude of the source.

$$v = \frac{q}{C} = \frac{1}{C}\frac{V_{in}/L\mathbf{s} + q(0)\mathbf{s} + q'(0) + Rq(0)/L}{\mathbf{s}^2 + R\mathbf{s}/L + 1/LC} \tag{A.9}$$

A.2.2 RLC voltage overshoot

Gate transitions can be superficially modelled with an undamped second order RLC system with solution shown below :

$$v_{gs}(t)/V_{cc} = 1 + K \cdot \cos(\omega_d t + \theta) \cdot \exp^{-\alpha t} \tag{A.10}$$

$$\alpha = \frac{R}{L} \tag{A.11}$$

$$K = -\frac{1}{\sqrt{1-\zeta^2}} \tag{A.12}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{A.13}$$

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} \tag{A.14}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{A.15}$$

$$\theta = \tan^{-1}\frac{\zeta}{\sqrt{1-\zeta^2}} \tag{A.16}$$

Where R, L, C is the total gate resistance, inductance and gate capacitance, respectively. The normalized voltage overshoot can be obtained by setting the derivative of $dV_o/dV_{cc} = 0$

$$\frac{V_o}{V_{cc}} = \frac{V_{pk} - V_{cc}}{V_{cc}} = \exp\left(\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}\right) \tag{A.17}$$

We note that overshoot only exists in an under-damped case, i.e. $\zeta < 1$. The upper bound of the overshoot is 100% for the lowest values ζ. The conditions for this to be true in terms of gate resistance can be obtained by rearranging Equation A.14:

$$R > \frac{2}{\sqrt{C/L}} \tag{A.18}$$

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