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Delta-Sigma Modulator for Wideband and Multi-Band Radio Systems

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Delta-Sigma Modulator for Wideband and Multi-Band Radio Systems

by

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Abstract

The proliferation of modern communication systems places stringent requirements on analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to operate on wideband signals while being power and resource efficient. In this thesis, the utilization of delta-sigma modulators for wideband and multi-band applications in both the receiver and transmitter is addressed. The first model proposes a low-complexity frequency band decomposition-based parallel DSM ADC architecture which lowers the resource consumption considerably compared to the conventional QMF-FBD ADC and maintains an acceptable SNDR. An FPGA implementation and resource estimation of the proposed model was performed as a proof of concept. The second model presents a concurrent dual band DSM architecture for spectrum aggregation transmitter application and provides a comprehensive analysis of step-by-step design process. The quantization noise is shaped in this architecture enabling concurrent transmission of two signals with low in-band noise interference. Simulation was performed with two carrier frequency bands of LTE signals as proof of theory.

Acknowledgements

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I express my gratitude to my parents, my wife, my sister and my brother for their support and encouragements. Especially, I would like to thank my mother for her guidance, encouragement and prayers and my wife, Tanzina for her tremendous support.

To my parents and my wife

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List of Symbols, Abbreviations and Nomenclature

Symbol	Definition
ADC	Analog-to-Digital Converter
BPDSM	Band-pass Delta-sigma Modulator
DAC	Digital-to-Analog Converter
dB	Decibel
DSM	Delta-Sigma Modulator
FBD	Frequency Band Decomposition
GHz	Giga Hertz
HPDSM	High-pass Delta-Sigma modulator
IF	Intermediate Frequency
LPDSM	Low-pass Delta-Sigma Modulator
LTE	Long Term Evolution
MHz	Mega Hertz
NTF	Noise Transfer Function
OSR	Oversampling Ratio
PA	Power Amplifier
PAPR	Peak to Average Power Ratio
QMF	Quadrature Mirror Filter bank
RF	Radio Frequency
S/H	Sample and Hold
SNDR	Signal-to-Noise and Distortion Ratio
SMPA	Switching Mode Power Amplifier
STF	Signal Transfer Function
TIDSM	Time Interleaved Delta-Sigma Modulator

Chapter One: Introduction

Wireless connectivity has grown immensely within the last decade with a greater impact on human life. Today mobile-cellular subscriptions are almost as many as people on earth. Figure 1-1 shows the growth of mobile subscriptions within between 2005 and 2013. Mobile revolution is empowering more people in different sectors like education, health, government, banking, environment and business with more Information Communication Technology (ICT) applications. Continuous high growth of mobile broadband using 3G resulted with more than 2 billion subscriptions worldwide which is almost 40% of the total population of the world [1].

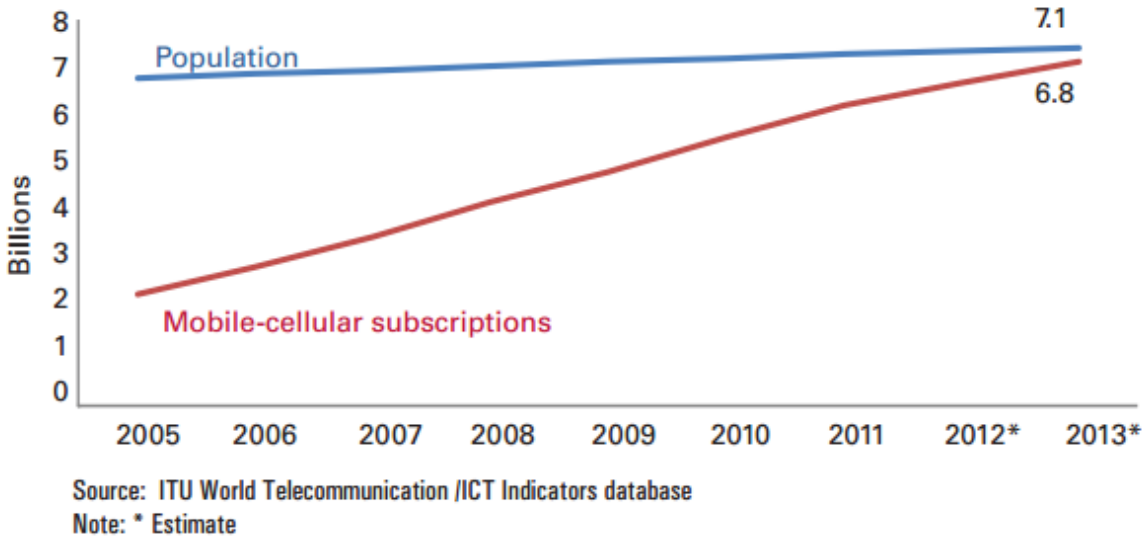


Figure 1-1. Growth of the number of mobile users over the years [1].

Continuous evolution of the technology leading to the cost reduction of the underlying hardware as well as the seemingly unceasing desire to unleash every electronic device has been the driving force for this growth. In order to accommodate different usage scenarios, a multitude of wireless standards have been evolved, which is categorized by the data rate and the range of communications shown in Figure 1-2. It has become a significant design challenge to support this multitude of wireless standards for current and future wireless devices.

At least more than five different wireless standards are supported by a cellular handset today, which operates at several frequency bands. Typically for supporting each wireless standard a dedicated transceiver IC along with necessary peripheral components are employed. Regardless of the increased complexity, the continuously reduced cost of hardware due to the advancement of the CMOS technology, the demand for reconfigurable, multi-standard, multimode wireless devices will only accelerate in near future. In this large market for cell-phones, especially with broadband standards, any research that can bring changes in performance such as bandwidth, integrations size i.e. less resources, and battery life will have a significant effect on the wireless communication market [3].

Moreover, there is a push for more flexible spectrum allocation for the next generation communication systems. Next generation mobile communication systems like international mobile telecommunications-advanced (IMT-advanced) models require a wide bandwidth of approximately 100 MHz to provide transmission data services at 1 Gbps [2]. From a practical perspective, as coordinating a contiguous band for suitable mobile communication is very

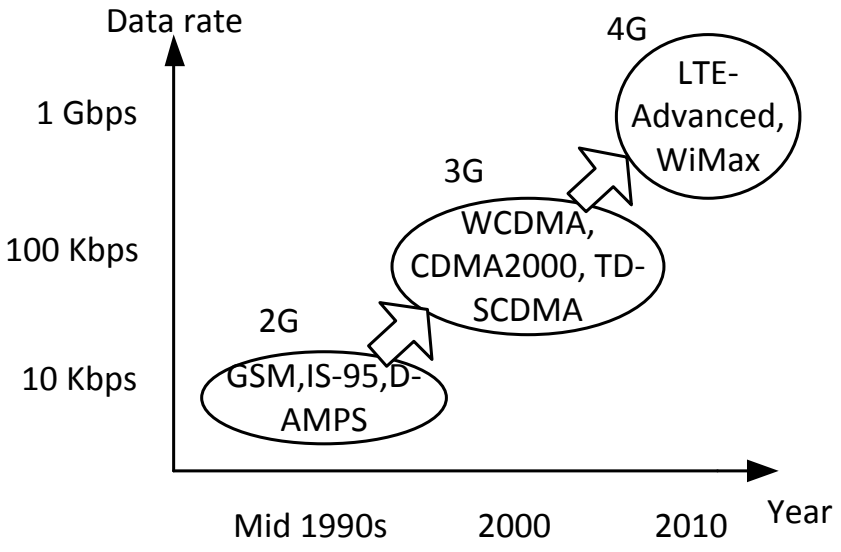


Figure 1-2. Evolution of communication standards and their data rates.

difficult, spectrum aggregation technique can be a solution for wide bandwidth high speed data communication. Flexible spectrum allocation can make more efficient and cost-effective use of the radio-frequency spectrum. However, to fulfill these requirements reconfigurable, multi-standard, wideband RF transmitters and receivers such as Software Defined Radio (SDR) is the most appropriate system approach.

The development of software defined radio (SDR) (Figure 1-3) that can be used across different frequency bands and for multi-standard applications is a critical element for the convergence of different communications systems. Efficiency in power and spectrum handling for supporting different frequency carriers are important features of SDR concept [3][4][5]. An efficient procedure to reconfigure the radio system to any new wave form without changing the hardware to support multiple standards simultaneously is a design challenge for SDR. This brings us to the fact that, extensive use of DSP blocks is inevitable for designing SDR. Nevertheless, a scheme of processing the RF signal entirely in the digital domain places an incredible burden in the analog-to-digital (ADC) and digital-to-analog converter (DAC) circuits.

Reconfigurable transmitter and receiver places the ADC and DAC closer to the antenna to remove as much analog preprocessing blocks as possible [6]. Furthermore, moving the ADC/DAC closer to the antenna imposes more stringent requirements on their performance metrics like bandwidth, dynamic range (resolution), and resources employed. For multi-standard systems like SDRs, the ADC/DAC is expected to have a wide bandwidth in several gigahertz as well as medium to high resolution (8 to 10 bits)[8]-[11].

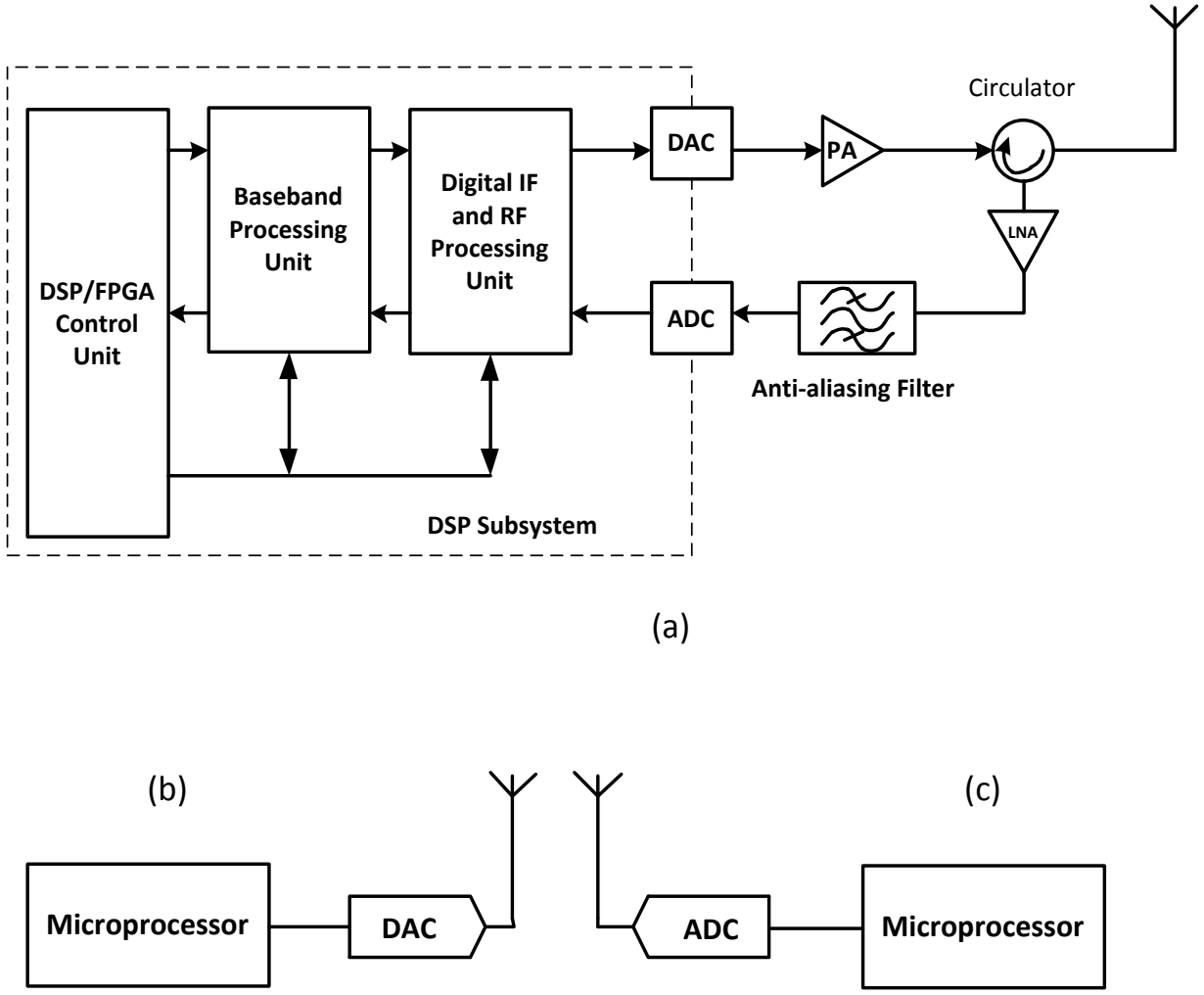


Figure 1-3. (a) Ideal SDR transceiver architecture, (b) SDR transmitter block diagram, (c) SDR receiver block diagram [6].

1.1 Trade-off: Bandwidth vs. Resolution

It has been revealed that for different ADCs there is an inverse relationship between the resolution and the signal bandwidth [12]. It is very much possible to attain high-speed i.e. wide bandwidth analog-to-digital conversion with low resolution, but the bandwidth decreases drastically with the increase of resolutions or vice-versa. The fastest single (non-parallel) ADC in literature is reported to have 4 to 6 bits with sampling rate up to 4 GHz for Nyquist rate single

flash ADC [13]-[15]. The highest resolution ADCs available are delta-sigma modulators with a few tens of megahertz [16].

Flash ADC architectures are comprised of a parallel comparator array where the number of comparators increases exponentially with the resolution. Figure 1-4 shows a generic schematic of a flash ADC where an analog input signal is compared with an array or resistors to generate the reference voltages. The output of the comparators, after several amplification and latching stages, are formed as thermometer code before it enters the encoder. The thermometer code is converted to a gray or a binary code by the encoder in the final stage [13].

The number of the required comparators in an N-bit flash ADC is calculated to be 2^N. The separation of the adjacent reference voltages for the comparators shrinks exponentially as the number of the comparators increases [12]. As a result, a larger area and power are required to design a high resolution flash ADC. The component matching is also difficult for a large number

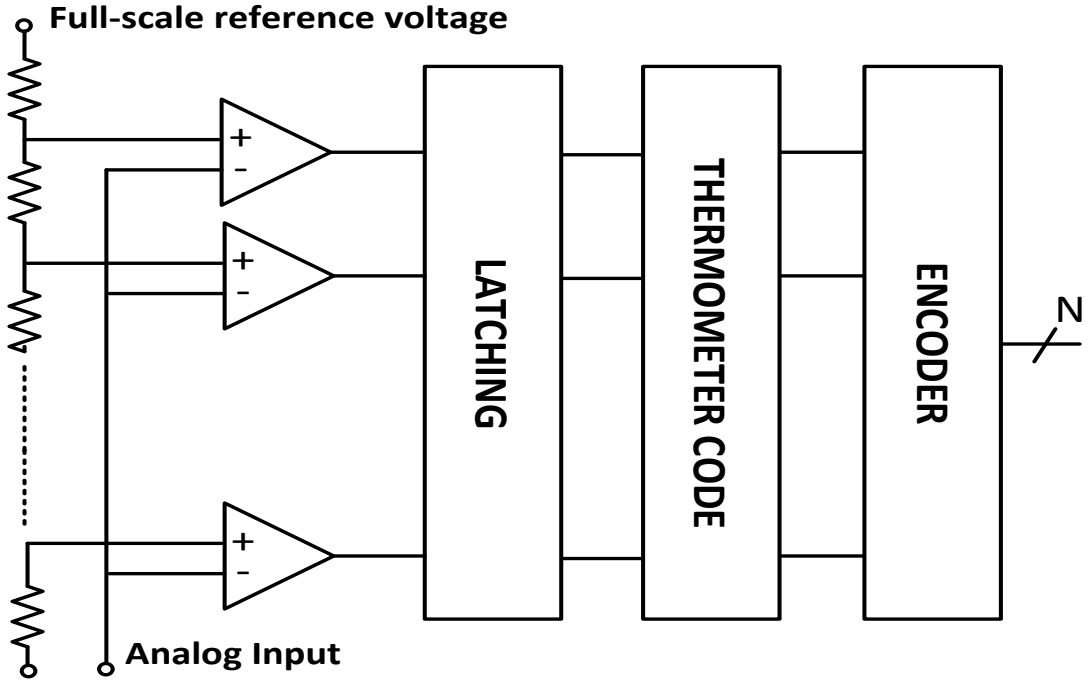


Figure 1-4. Generalized block diagram of Flash ADC [7].

of comparators in an array. Moreover, as the input capacitance increases, it reduces the input bandwidth in flash ADCs. Therefore, single flash ADCs can rarely achieve more than 6 bits in GHz speed.

There is a trade-off between speed and resolution for delta-sigma modulators. Generally a very high oversampling ratio compared to the Nyquist sample rate is employed for DSM. Figure 1-5 shows a generic architecture of a delta-sigma modulator. The concept of delta-sigma modulator is based on oversampling and quantizing the signal. The analog input signal is fed to an integrator, the output of which goes to a quantizer. The output of the quantizer is then fed back and compared with the input for the differences so that the average of the quantized signal tracks the average of the analog input signal. The employment of a feedback loop in the modulator results in different transfer functions for the input signal and quantization noise. The quantization noise is suppressed and shaped outside the useful frequency band and thus the higher resolution is achieved [17]-[18].

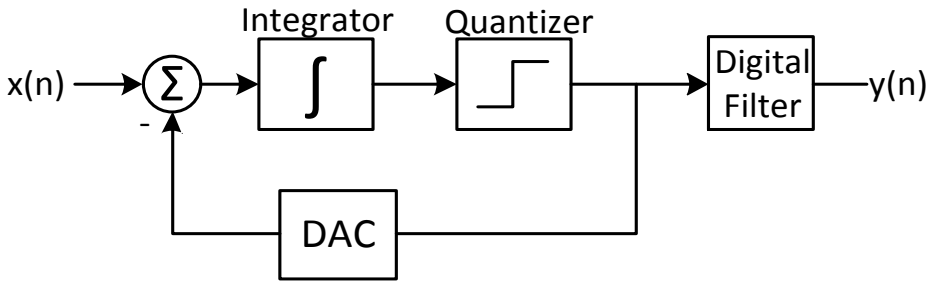


Figure 1-5. Generalized block diagram of Delta-Sigma Modulator.

The oversampling ratio (OSR) is only achievable to a certain limit which constrains the wide bandwidth applications. However, alternative techniques can be applied to attain comparatively large noise suppression with low oversampling ratio.

Increasing the order of the modulator to improve the noise shaping can be an approach to reduce the OSR requirements of delta-sigma modulators for high frequency applications [19]. The stability, however, is a critical issue for higher order DSMs [20][21], as well as, the sensitivity to component mismatch [19]. Multi-bit quantization is employed to enhance the noise shaping of DSM [22]. However a multi-bit DSM digital-to-analog converter (DAC) generates a varying envelop signal which cannot be employed for the purpose of driving a switching mode power amplifier (SMPA) for delta-sigma modulator based transmitter [23]. Moreover, designing the feedback loop for multi-bit DSM is challenging, as well as, the nonlinearity of the feedback loop directly contributes to the nonlinearity of the modulator.

Other approaches includes the usage of cascaded stages where, multiple stages of noise shaping cascaded together can achieve a high degree of quantization noise suppression with low oversampling ratio. As the stages can employ single-bit quantization, the linearity and stability issues associated with high order and multi-bit modulators can be avoided. However, the number of the useful cascaded stages is limited and complexity increases as the number of stages increase [22].

Parallel processing technique can be employed to design wideband high resolution ADC/DAC, which alleviates the speed limitation of wideband DSMs. A simple parallel DSM is constructed by connecting several DSMs in parallel and applying the signal simultaneously to all channels [24]. The output of all the channels can then be combined to get the desired output. However, increased hardware and power consumption are some drawbacks of parallelism techniques. Nonetheless, compensation for errors as a result of non-idealities and mismatch between parallel channels becomes challenging for these types of architectures. Three major parallel architectures will be reviewed and compared in Chapter 2.

1.2 Objective and Thesis Contributions

The objective of the thesis is to study and analyze the Delta-Sigma modulator for wideband receiver and transmitter applications. It proposes two architectures, which are aimed to solve the basic imperfections of wideband DSM for receiver and transmitter architectures respectively.

The two major contributions proposed in the thesis are detailed below-

- The first work proposes a novel architecture for a low complexity frequency band decomposition based delta-sigma modulator for wideband receiver applications.
- The second work proposes a novel low complexity delta-sigma modulator for concurrent dual band spectrum aggregation transmitter application.

1.3 Thesis Outline

The organization of the thesis is as follows: Chapter 2 discusses the basics of delta-sigma modulator followed by a background review of three conventional parallel ADC architectures in the literature with their advantages and disadvantages. It also discusses various figures of merits to test the ability of the proposed architectures to meet the design purpose.

Chapter 3 presents the proposed architecture for low complexity frequency band decomposition based delta-sigma modulator. An FPGA level implementation and required resource calculation is also presented as a proof of concept.

Chapter 4 presents the proposed architecture of another delta-sigma modulator for concurrent dual band spectrum aggregation transmitter application. Design methodology and simulation results are discussed for this architecture.

Finally, Chapter 5 is dedicated to summarizing the work done, deriving the conclusions and making suggestions for future work.

Chapter Two: Delta-Sigma Modulator Basics and Parallel Techniques

2.1 Delta-Sigma Modulator Overview

The concept of delta-sigma modulator is based on oversampling and quantizing the signal as well as shaping the quantization noise generated in the process. Usually a single-bit quantizer is chosen to convert a varying envelope signal to a signal with constant envelope. A high amount of quantization noise is generated at the output of DSM both inside and outside the band of interest. Regardless of the quantization noise shaped outside the signal band of interest, a portion of the noise remains in the band of interest, which degrades the quality of the converted signal. Generally it is assumed that the quantization noise is uncorrelated to the input signal and modeled as white noise which is added to the signal [17][18]. DSM employs oversampling in order to distribute the quantization noise evenly over larger frequency band and therefore achieve smaller in-band noise [17][25]. The oversampling ratio (OSR) of a signal is defined as the ratio of the sampling frequency (f_s) to the signal bandwidth (BW):

$$OSR = \frac{f_s}{BW} \tag{2-1}$$

For measuring the signal quality and the amount of in-band noise in the converted signal by DSM, the metrics employed for this research was signal-to-noise and distortion ratio (SNDR). The SNDR is defined as follows [26]:

$$SNDR = 10\log\left(\frac{Desired\ Signal\ Power}{In-Band\ Noise\ and\ Distortion\ Power}\right) \tag{2-2}$$

The quantization noise modeled as a white noise added to the signal, the SNDR of the signal at the output of the quantizer can be written as:

$$SNDR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) + 10\log(\frac{f_s}{BW}) \quad (2\text{-}3)$$

Where, σ_x^2 is the variance or power of the input signal, and σ_e^2 is the power of the quantization noise.

From (2-3), the SNDR will be improved approximately 3 dB if the oversampling ratio (OSR) is doubled. Figure 2-1 shows the effect of the oversampling of the signal on the generated quantization noise quantity at the quantizer output.

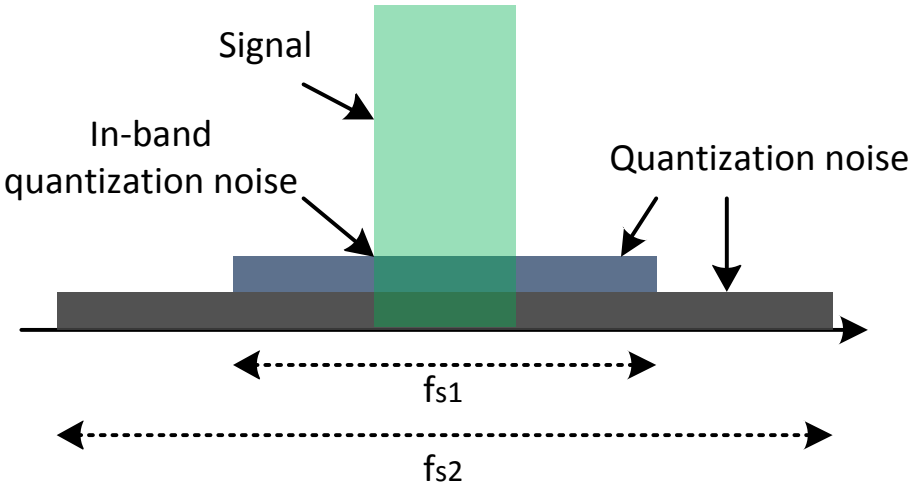


Figure 2-1. Effect of OSR on quantization noise [3].

Oversampling a signal reduces the in-band quantization noise, yet the signal quality needs to be improved further to be employed in communication systems. For instance, for an SNDR improvement by 20 dB for a single bit quantizer, the required OSR of the signal is about 100 times. For example, for a signal with 10 MHz bandwidth requires about 1 GHz of sampling frequency, i.e. the clock frequency of the system, which might not be feasible. Shaping the quantization noise outside the band of interest with DSM can improve further the SNDR of the quantizer [17][25]. The block diagram of a first order DSM is shown in Figure 2-2 [17]. The model consists of an integrator and a quantizer. For mathematical modeling, the quantizer is

modeled as a quantization noise with a random noise source $E(z)$ and an adder. If the integrator is replaced with its equivalent discrete z transform model, the transfer function of the DSM can be derived as follows:

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{2-4}$$

Where, $X(z)$, $Y(z)$ and $E(z)$ are the z-transforms of the input, output and quantization error respectively. Here the signal transfer function (STF) and the noise transfer function (NTF) are given by:

$$STF(z) = z^{-1} \tag{2-5}$$

$$NTF(z) = (1 - z^{-1}) \tag{2-6}$$

From (2-5) it can be observed that the STF is just a delay and the NTF is equivalent to a high-pass filter [25]. Usually the signal is located at frequency around zero or baseband for DSM. Therefore, the STF is generally a delay or a linear gain for transferring the input to the output without any distortion. For DSMs the order of the loop filter is defined with the order of the NTF. From (2-6), it can be easily realized that this NTF represents a first-order DSM.

Consequently, the output of the DSM is a quantized signal with a quantization noise shaped outside the band of interest to the higher frequency which is shown in Figure 2-3.

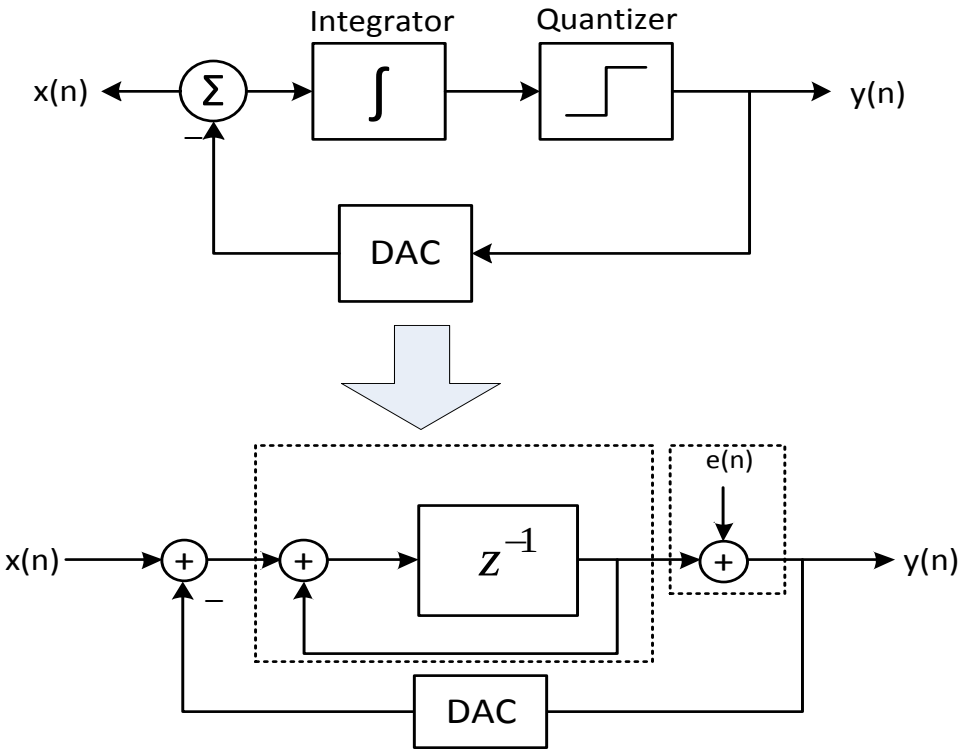


Figure 2-2. Block diagram of a first order DSM and z-domain equivalent circuit [3].

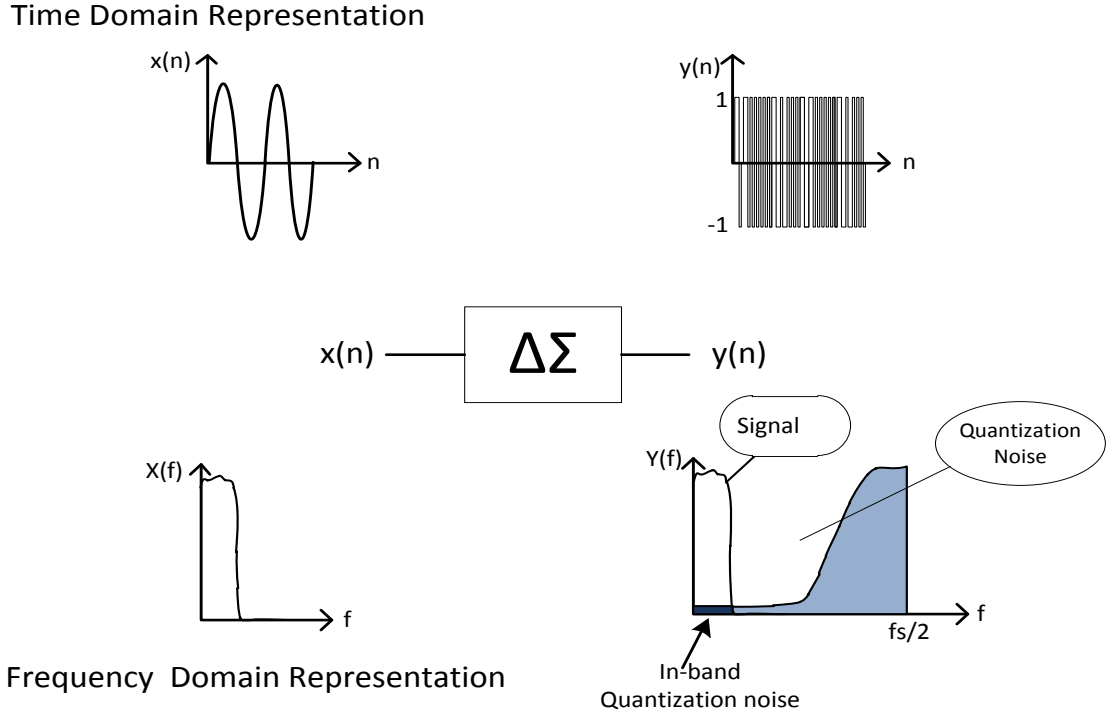


Figure 2-3. Input and output of a DSM in time and frequency domain [3].

For the case of 1st order DSM (Figure 2-2), the SNDR can be calculated as follows [17]:

$$SNDR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log(\frac{\pi^2}{3}) + 30\log(\frac{f_s}{BW}) \quad (2\text{-}7)$$

Where σ_x^2, σ_e^2, f_s, and BW are, power of the input signal, power of the quantization noise, sampling frequency, and bandwidth respectively.

It can be resolved after comparison between (2-3) and (2-7), a signal with OSR of 100 can improve the SNDR by 55dB for a 1st order DSM, whereas the improvement will be only 20 dB for the same OSR without a DSM.

Increasing the order of the delta-sigma modulator will improve the in band signal quality furthermore. As the order of the DSM is defined by the order of the NTF:

$$NTF = (1 - z^{-1})^L \quad (2\text{-}8)$$

The SNDR for the higher order DSM is calculated as follows [17]:

$$SNDR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log(\frac{\pi^{2L}}{2L+1}) + 10(2L+1)\log(\frac{f_s}{BW}) \quad (2\text{-}9)$$

However, maintaining the stability in higher order DSMs is critical [25].

2.1.1 Low-Pass, Band-Pass and High-Pass DSMs

A Z-domain representation of the aforementioned first order low-pass DSM (LPDSM) is illustrated in Figure 2-4. (2-4) shows the transfer function of first order LPDSM. There are two other delta-sigma modulator architectures according to their frequency response; Band-Pass DSM (BPDSM) and High-Pass DSM (HPDSM). The input signals of these DSM topologies are IF signals, rather than baseband. From their name it can be understood that BPDSM operates on the band-pass frequency range and HPDSM operates on high-pass frequency range.

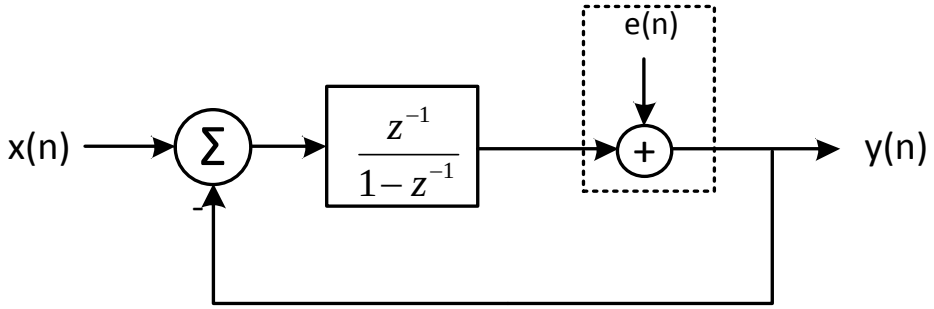


Figure 2-4. First order LPDSM.

There are several different techniques to design the transfer function for BPDSM and HPDSM in the literature [59][60]. However, the transfer function for BPDSM and HPDSM can also be derived from the corresponding transfer function of LPDSM by applying some mapping functions. The mapping for deriving the transfer functions are as follows [29]:

$$z^{-1} \rightarrow -z^{-2} (LP\ to\ BP) \tag{2-10}$$

$$z^{-1} \rightarrow -z^{-1} (LP\ to\ HP) \tag{2-11}$$

A second order LPDSM and corresponding BPDSM and HPDSM is shown in Figure 2-5, where the BPDSM and HPDSM is obtained by mapping $-z^{-2}$ and $-z^{-1}$ for z^{-1}. The frequency response and pole-zero plots of all three DSMs NTF are shown in Figure 2-6. The transfer functions of BPDSM and HPDSM are as follows:

$$Y_{BP}(z) = -z^{-2} X(z) + (1+z^{-2})^2 E(z) \tag{2-12}$$

$$Y_{HP}(z) = -z^{-1}X(z) + (1+z^{-1})^2 E(z) \tag{2-13}$$

(2-12) and (2-13) show the transfer functions of BPDSM and HPDSM respectively, where $NTF_{BP} = (1+z^{-2})^2$, $NTF_{HP} = (1+z^{-1})^2$ and $STF_{BP} = -z^{-2}$, $STF_{HP} = -z^{-1}$. It can be observed that the order of the NTF shows the order of the modulator which in this case is 2.

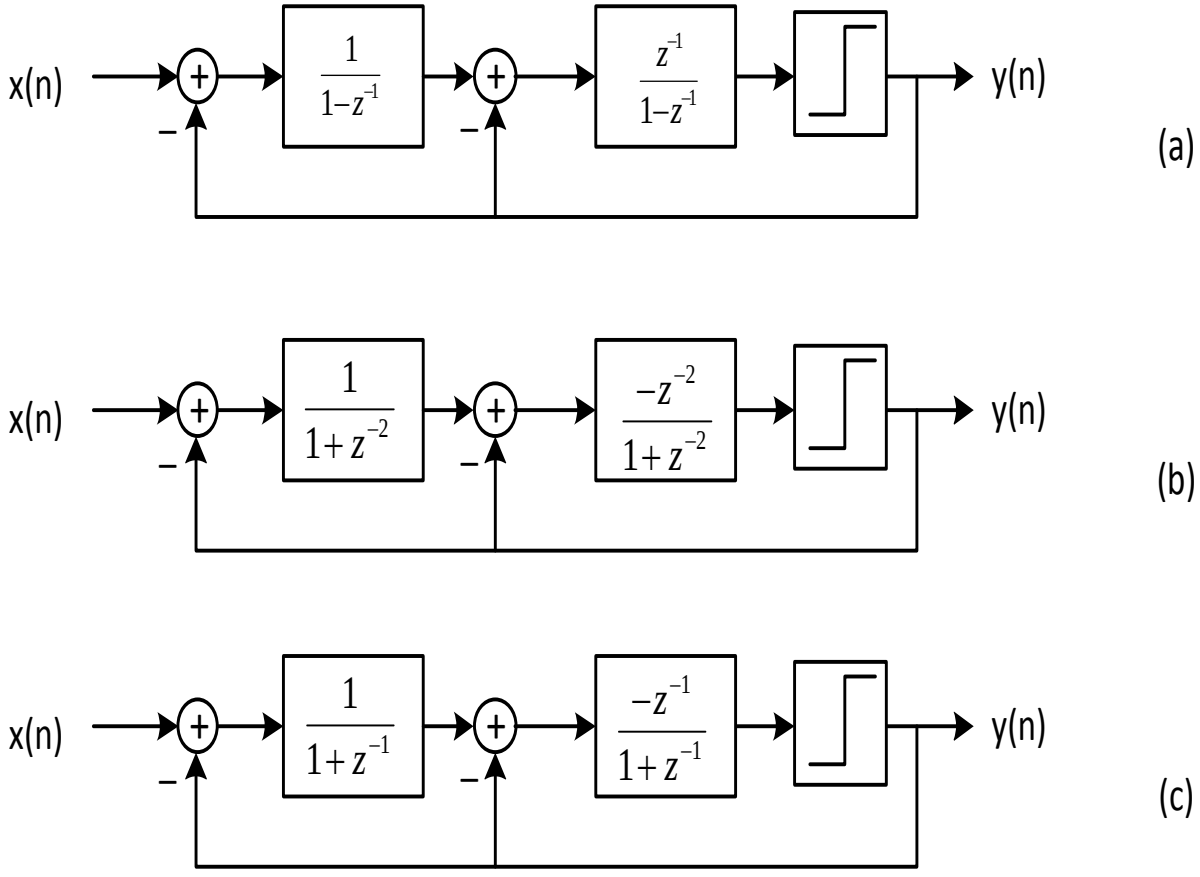
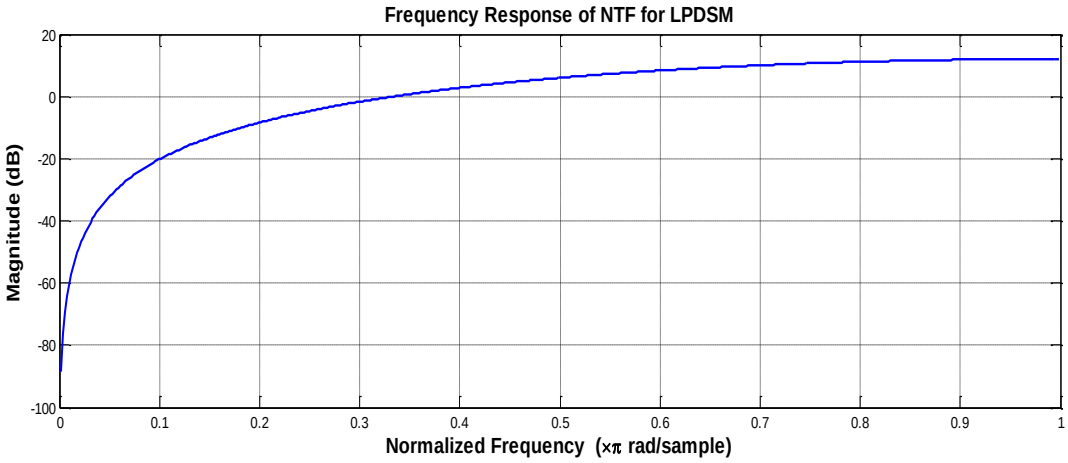
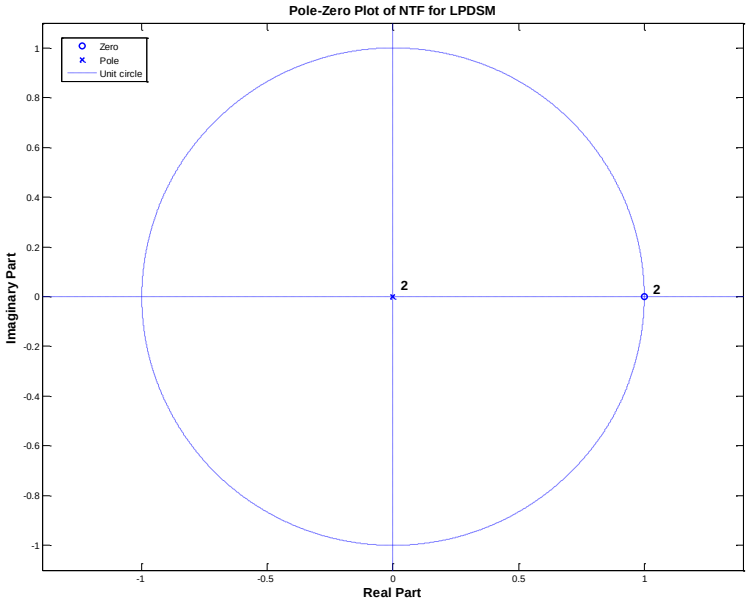
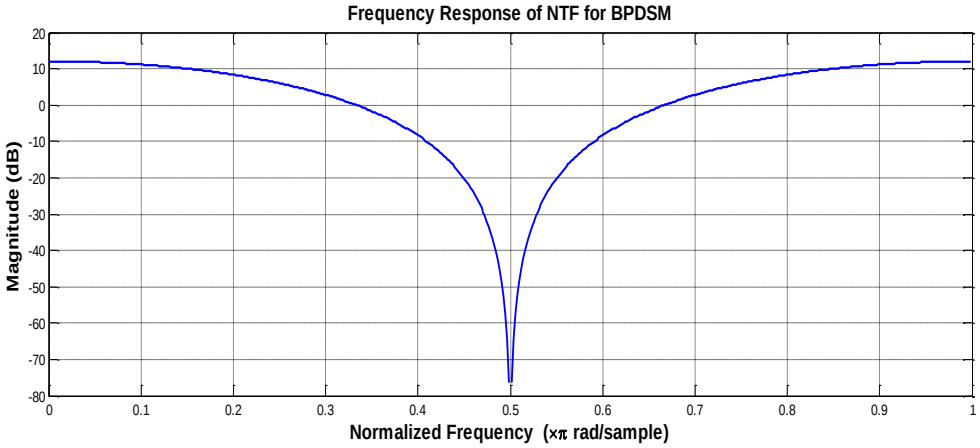


Figure 2-5. Second order (a) LPDSM, (b) BPDSM, (c) HPDSM [3].


Frequency Response of NTF for LPDSM
Magnitude (dB)
Normalized Frequency (×π rad/sample)


Pole-Zero Plot of NTF for LPDSM
Zero
Pole
Unit circle
Imaginary Part
Real Part
2
2


Frequency Response of NTF for BPDSM
Magnitude (dB)
Normalized Frequency (×π rad/sample)

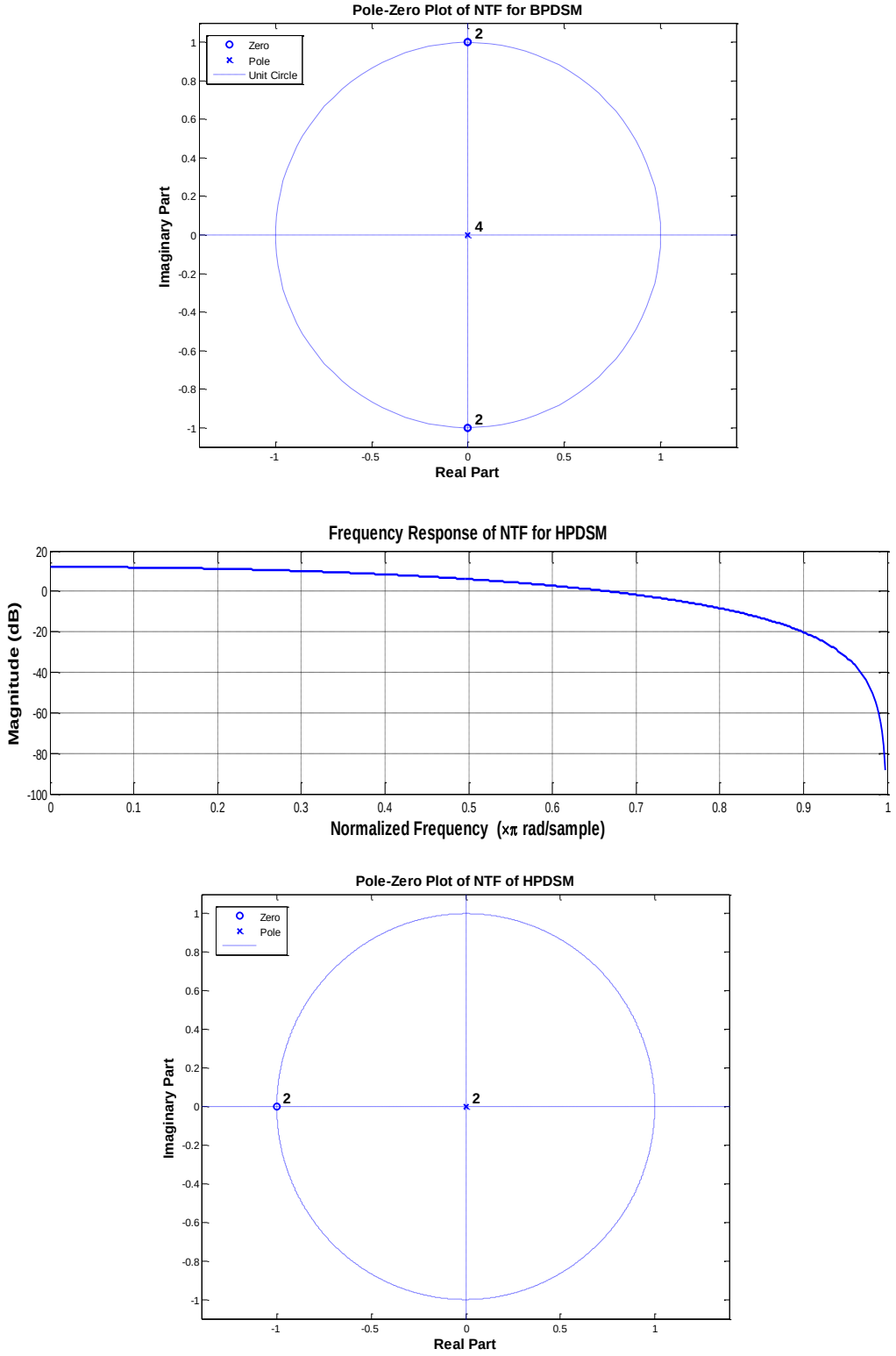


Figure 2-6. Frequency response and Pole-zero plot of the NTF of (a) LPDSM, (b) BPDSM, (c) HPDSM.

2.2 Parallelism Techniques for Wideband DSM

As discussed previously, delta-sigma modulators produce quantized data usually in a bi-level format, where the quantization noise is shaped and pushed outside the useful signal band. However, the very high processing speed requirements in DSM limit its applications [24][33]. Parallel processing techniques can be applied to DSMs to address the speed limitation issues for wideband applications.

The general idea of implementing parallelism in delta-sigma ADC structure is that, a wideband input signal is fed simultaneously to the parallel channels. The signal is then modulated and filtered optionally before it is applied to DSM. The output of the DSM is then filtered and demodulated. Finally, the outputs from all the channels are added to get the final wideband output signal equivalently to a signal with oversampling as number of channels [24][30]. A generalized architecture of the parallel delta-sigma modulator is shown in Figure 2-7, where each channel of the parallel structure converts only a part of the wideband signal, thus the OSR is reduced while achieving high resolution, linearity and low in-band noise. In literature, there are three major architectures for parallel processing which can be applied for delta-sigma modulators: Time-Interleaved architecture, Hadamard Modulated architecture, and Frequency Band Decomposition based architecture.

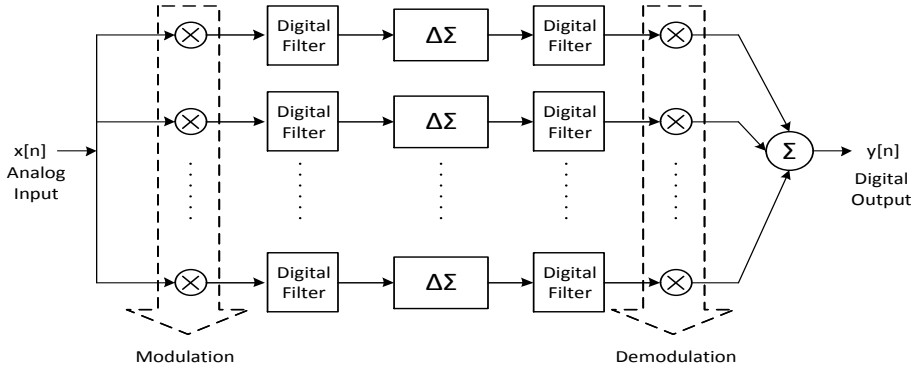


Figure 2-7. Generalized Parallel Delta-Sigma ADC Architecture.

2.2.1 Time Interleaved Delta-Sigma Modulator

Time interleaved Delta-Sigma Modulators (TIDSM) utilize polyphase decomposition techniques [26] [32] which employ a method, where an arbitrary transfer function can be decomposed into pseudo circulant transfer functions matrices. These transfer function matrices are then implemented in parallel channels with multi-rate signal processing. In this architecture input is down-sampled M times and delayed in each channel before the polyphase components [32] are applied, where each row of the matrix becomes the transfer function of each channel in the modulator. The output of each channel is then again up-sampled by M times and added with a delay to re-construct the output signal. Here M is the number of channels, which is also the row and column size for the transfer function matrix.

In this architecture, polyphase multi-rate technique is extensively used to derive the structure of the parallel ΔΣ. If a transfer function $H(z)$ is provided then the equivalent polyphase model circuit could look like below:

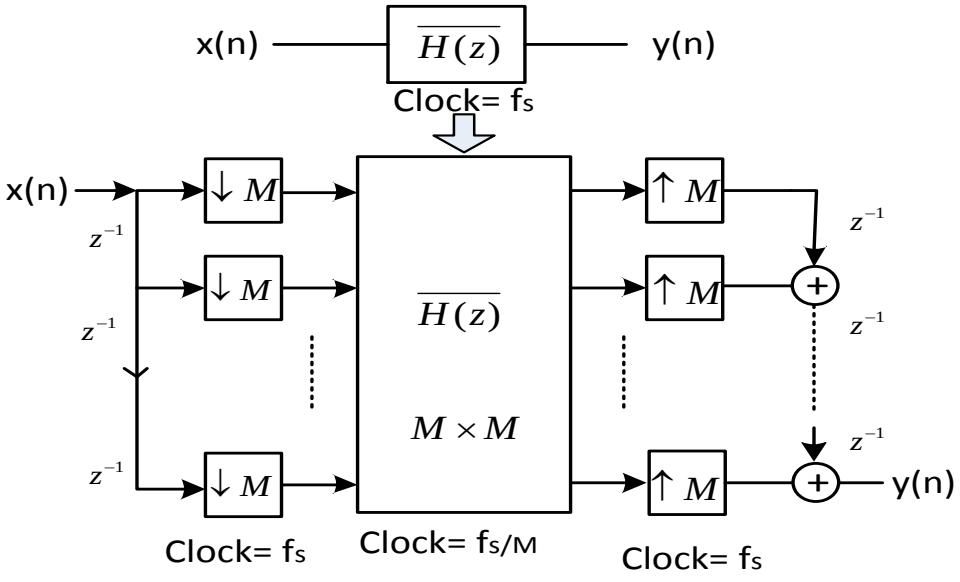


Figure 2-8. Time Interleaved DSM block diagram with polyphase technique [3][26].

Here $\overline{H}(z)$ is an $M \times M$ transfer function matrix which can be expanded as [26]:

$$\bar{H}(z) = \begin{bmatrix} E_0(z) & E_1(z) & \cdots & E_{M-1}(z) \\ z^{-1}E_{M-1}(z) & E_0(z) & & E_{M-2}(z) \\ \vdots & & \ddots & \vdots \\ z^{-1}E_1(z) & z^{-1}E_2(z) & \cdots & E_0(z) \end{bmatrix} \tag{2-14}$$

Where, $E_i(z)$ are the polyphase components of $H(z)$. The relationship between H(z) and $E_l(z)$ is given by [26]

$$H(z) = \sum_{l=0}^{M-1} z^{-1} E_l(z^M) \tag{2-15}$$

If a second order delta-sigma modulator is taken as reference which has two transfer functions $H_1(z)$ and $H_2(z)$ in the loop:

$$H_1(z) = \frac{1}{1-z^{-1}} \tag{2-16}$$

$$H_2(z) = \frac{z^{-1}}{1-z^{-1}} \tag{2-17}$$

From (2-15), the polyphase components for each transfer function can be calculated. For example, the polyphase components for a 4 channel TIDSM are given below.

For (2-16) the polyphase components are:

$$E_0(z) = \frac{1}{1-z^{-1}} \tag{2-18}$$

$$E_1(z) = E_2(z) = E_3(z) = \frac{1}{1 - z^{-1}} \tag{2-19}$$

For (2-17) the polyphase components are,

$$E_0(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2-20}$$

$$E_1(z) = E_2(z) = E_3(z) = \frac{1}{1 - z^{-1}} \tag{2-21}$$

From (2-18) – (2-20), the $\overline{H_1}(z)$, and $\overline{H_2}(z)$ matrices can be written as follows:

$$\overline{H_1}(z) = \begin{bmatrix} \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ z^{-1}\frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ z^{-1}\frac{1}{1-z^{-1}} & z^{-1}\frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ z^{-1}\frac{1}{1-z^{-1}} & z^{-1}\frac{1}{1-z^{-1}} & z^{-1}\frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \end{bmatrix} \tag{2-22}$$

$$\overline{H_2}(z) = \begin{bmatrix} z^{-1}\frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ z^{-1}\frac{1}{1-z^{-1}} & z^{-1}\frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ z^{-1}\frac{1}{1-z^{-1}} & z^{-1}\frac{1}{1-z^{-1}} & z^{-1}\frac{1}{1-z^{-1}} & \frac{1}{1-z^{-1}} \\ z^{-1}\frac{1}{1-z^{-1}} & z^{-1}\frac{1}{1-z^{-1}} & z^{-1}\frac{1}{1-z^{-1}} & z^{-1}\frac{1}{1-z^{-1}} \end{bmatrix} \tag{2-23}$$

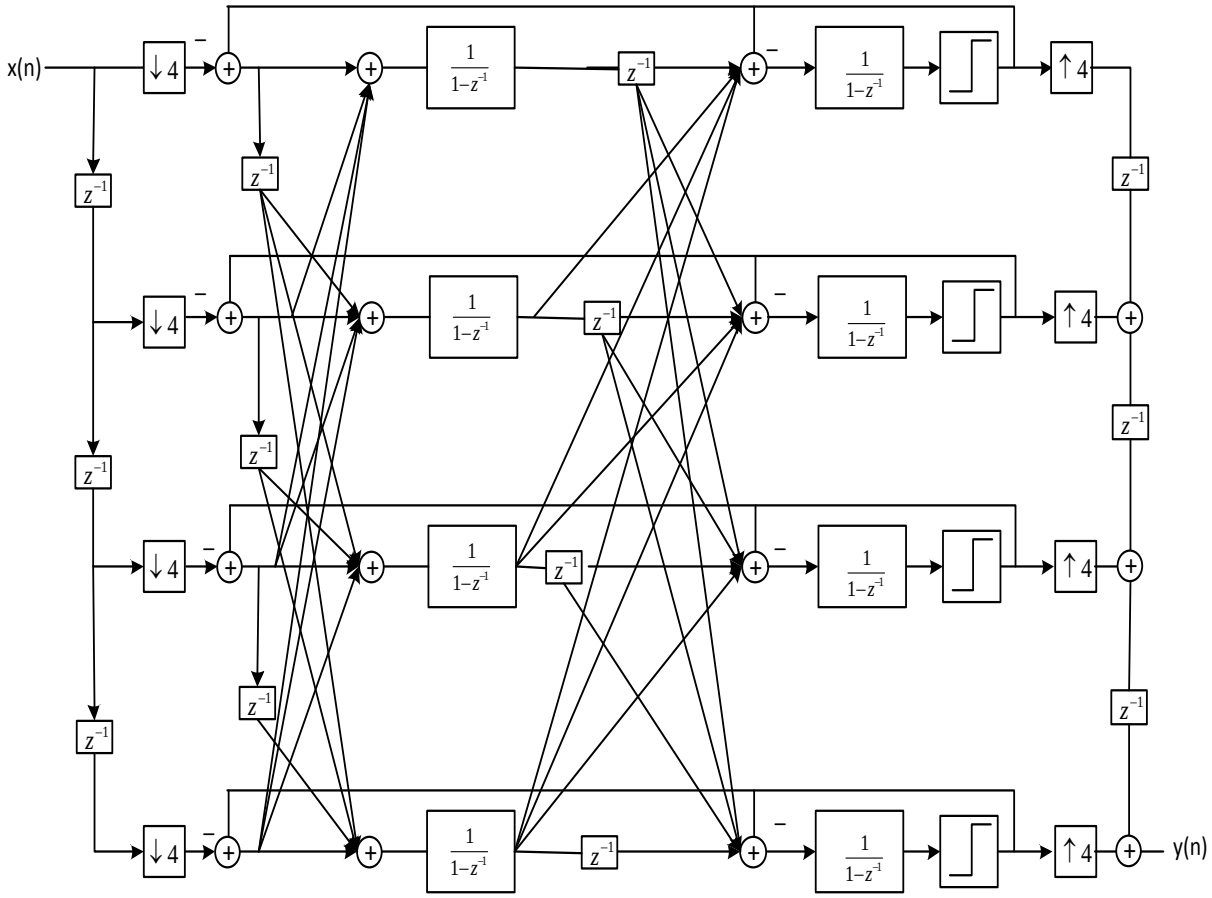


Figure 2-9. Four channel TIDSM.

2.2.2 Hadamard Modulated Delta-Sigma Modulator

Hadamard Delta-Sigma Modulator employs Hadamard Sequence for modulation and decomposition the signal for A/D conversion and doesn't require either time interleaving or oversampling [33] – [36]. In this architecture each channel input sequence is multiplied by a specific ±1 Hadamard sequence before the delta-sigma modulation is applied. The output of delta-sigma modulator on channel is low-pass filtered and multiplied again by a delayed version of input Hadamard sequence and recombined for achieving overall output.

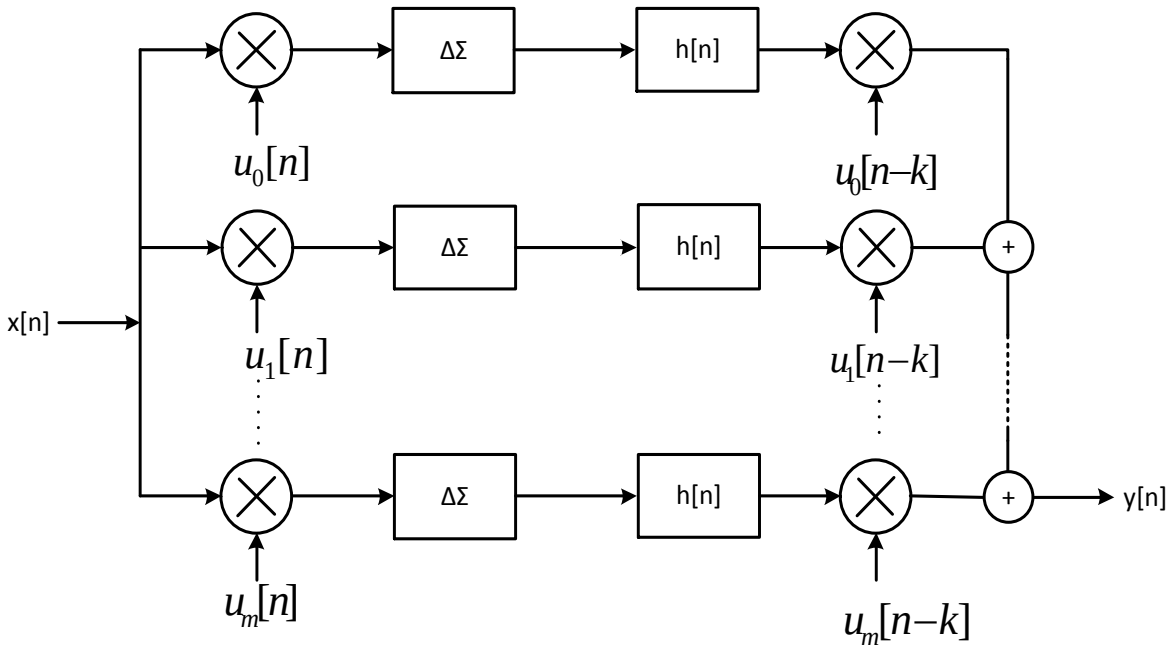


Figure 2-10. Hadamard modulated DSM [33].

In the above Figure 2-10 above, $u_r[n]$ is the r-th row of Hadamard Matrix, whereas the delayed version of the input sequence is given by $u_r[n-k]$ with k as the system delay [33]. Generalized algorithm for generating Hadamard matrices is given by,

$$H_{n+1} = \frac{1}{\sqrt{2}} \begin{bmatrix} H_n & H_n \\ H_n & -H_n \end{bmatrix} \tag{2-24}$$

$$H_i = \begin{bmatrix} H_{i-1} & H_{i-1} \\ H_{i-1} & -H_{i-1} \end{bmatrix} \tag{2-25}$$

A 4×4 Hadamard modulated DSM sequence is given by:

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \tag{2-32}$$

A four channel Hadamard modulated DSM is shown in Figure 2-11. The main advantage of this architecture is that, there is no oversampling requirement unlike other parallel architectures [33]. As the quantization error components of the DSM are not Hadamard modulated at the input before filtering, the effect of filtering is not cancelled.

However, in comparative analysis it has been found that both Hadamard DSM and TIDSM are very prone and sensitive to channel gain and off-set miss matches [24][30][31].

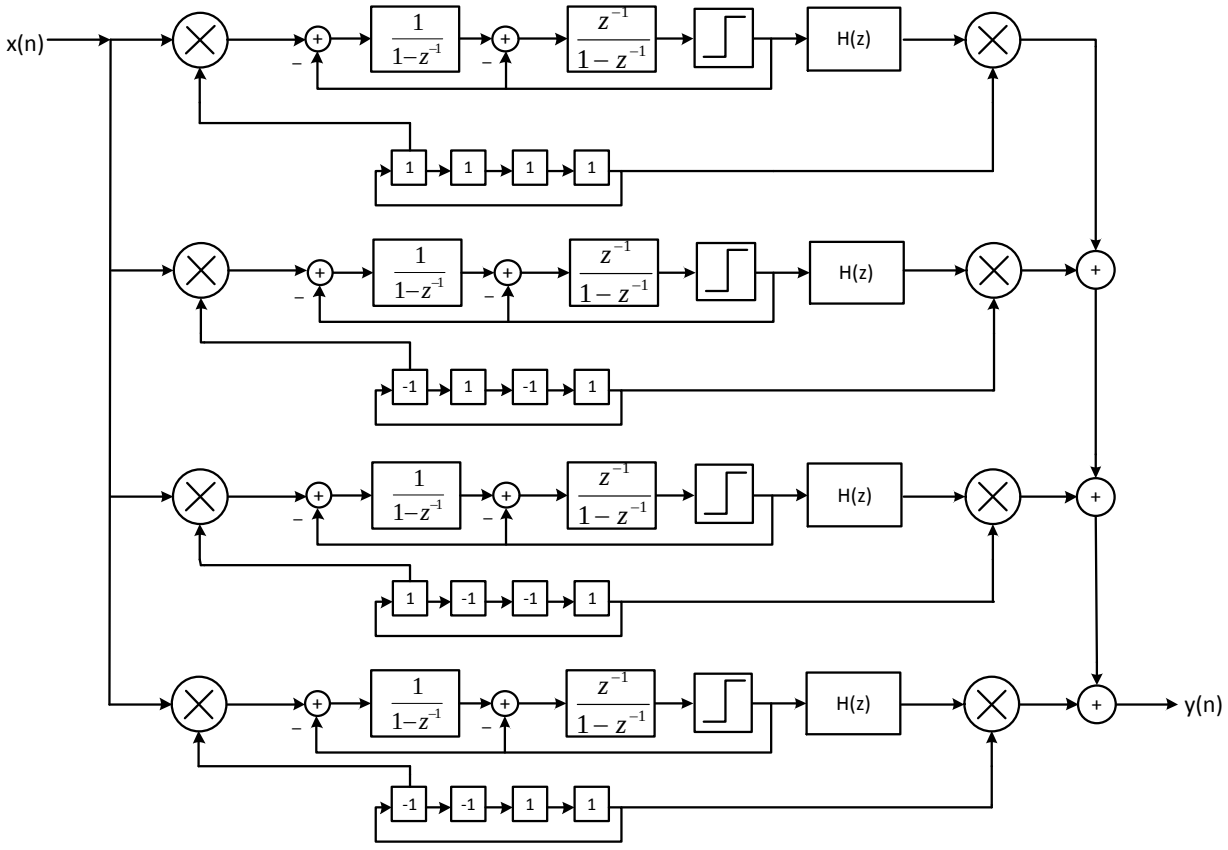


Figure 2-11. Four Channel Hadamard Modulated DSM.

2.2.3 Digital Frequency Band Decomposition ADC (QMF/FBD-ADC)

Frequency band decomposition (FBD) based ADCs break the wideband signal down to smaller bands and employ different band reject noise shaping transfer function for each band for A/D conversion. Quadrature mirror filterbank (QMF) was applied to decompose the wideband signal a set of sub-band signals in [37]-[39].

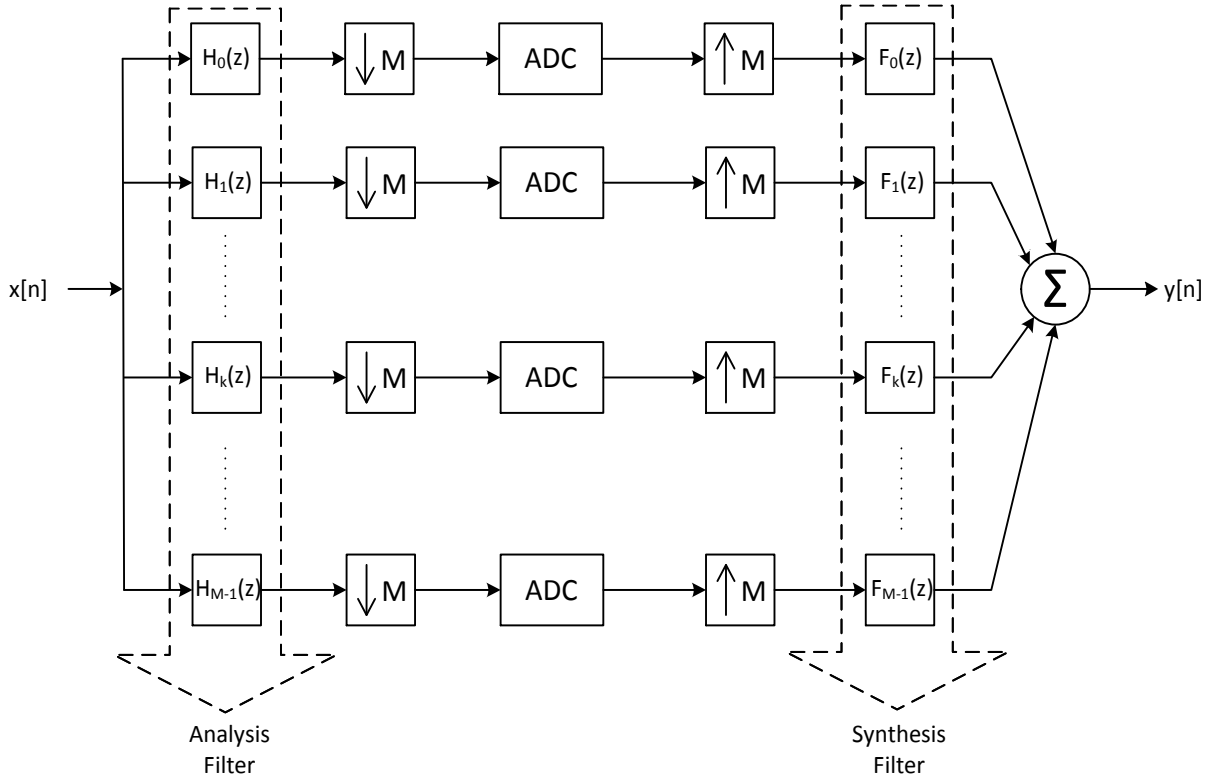


Figure 2-12. QMF FBD ADC architecture [37].

Figure 2-12 shows, an M channel FBD ADC architecture where a discrete time input signal $x[n]$ is passed through a filterbank of an array of M number of filters, $H_k(z)$ and decomposed to M sub-band signals. The first filter of the array is low-pass filter and the rest of them are band-pass filter. The first stage of the filter bank is called the analysis filters, which are

frequency selective in contiguous bands with bandwidth π/M. Figure 2-13 shows this filtering scheme of contiguous band frequency selective filtering.

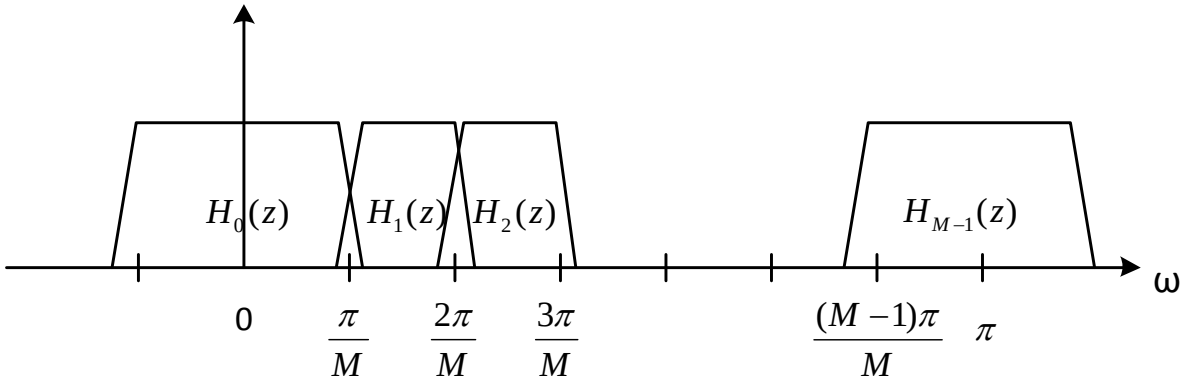


Figure 2-13. Filtering scheme of QMF FBD ADC [7][37]-[39].

After the first stage of filtering, the sub-band signals are then down-sampled by a factor of M before they are fed to the ADCs. Each sub-band is digitized at the rate $1/M$ of the original input signal. The output of the ADC is upsampled by M times and fed through another filter-bank $F_k(z)$ which is called the synthesis filter to remove the extra terms generated from undersampling. So the final output has the same sampling rate as the input. The transfer function of FBD DSM is given by [37]:

$$Y(z) = \frac{1}{M}\sum_{l=0}^{M-1}\left[X\left(zW^l\right)\sum_{k=0}^{M-1} H_k\left(zW^l\right)F_k\left(z\right)\right] \tag{2-33}$$

Where, $W = e^{j2\pi/M}$, Y(z) is the output, $X\left(zW^l\right)$ is the sub-band signal and $H_k\left(zW^l\right)$, $F_k\left(z\right)$ are analysis and synthesis filters respectively. To achieve perfect reconstruction at the output the

analysis and synthesis filters can be designed such that the output gives a delayed and scaled replica of the input signal with aliasing cancellation.

Comparative analysis in the literature shows that Frequency Band Decomposition (FBD) architecture is very much insensitive to channel mismatch and jitter due to uneven sampling [24] [30] [31].

However, the implementation of analysis filters with switched-capacitor filters introduces switching noise and limits the speed of the system and the SNDR.

2.2.4 Frequency Band Decomposition Based ADC in Literature

Different techniques have been introduced for frequency band decomposition (FBD) based delta-sigma architecture in the literature [37] – [52]. Quadrature mirror filter-banks are employed to decompose a wideband signal into sub-bands for processing in QMF FBD ADC [37]-[39]. A Multiband delta-sigma architecture that was proposed in [40], [41] employs M channels operating in parallel on the M bands. Each channel contains band pass delta-sigma modulators. A filter bank attenuates the out-of-band noise for each channel before all the outputs are added together. Finally the added output is passed through a low-pass filter for perfect reconstruction of the wideband signal. Another sub-band decomposition technique [42] employing a bank of tuned band pass delta-sigma modulator was also developed independently by other authors. A programmable quantization noise null band pass delta-sigma modulator [43] was employed along with multi-rate filter banks in this architecture which performs more efficiently by varying the resolution across the bandwidth. To ease the high precision requirement of the band pass DSMs, a variant of the FBD architecture using continuous time analog delta-sigma modulator namely Extended Frequency Band Decomposition (EFBD) was proposed [44]-[46] where the high precision requirements of the band pass DSM was addressed.

Analog DSM, multiple stages of filtering, demodulation and remodulation is employed in this architecture to increase the efficiency of FBD, which, however, is more complicated in design as the Signal Transfer Function (STF) of analog modulators need to be corrected in two or more stages through amplitude correction and phase alignment separately. A frequency translating hybrid architecture was proposed in [7][47] which needs some digital compensation for mismatches [48] requires high precision when designing.

FBD is a very natural way to widen the bandwidth of DSM and has some advantages over other parallel structures. However it is still very complex to design, as, in general, each channel of the FBD DSM has to be designed carefully for different frequencies and multiple stages of filter banks have to be incorporated in the design. The FBD architectures found in the literature require high oversampling of the input signal before feeding it to the DSM channel.

Chapter 3 proposes a low complexity Frequency Band Decomposition Delta-Sigma architecture to address the design complexity of the conventional FBD.

2.3 Delta-Sigma Modulator Based Transmitter and Dual Band Application

A general block diagram of a delta-sigma modulator based transmitter [27] is shown in figure 2-14 which consists of a delta-sigma modulator, frequency up-converter and a power amplifier (PA). The PA employed is a switching mode power amplifier (SMPA) driven with a constant envelope signal obtained from DSM to achieve maximum PA efficiency. Though the high clock speed requirement to achieve good signal quality limits the application of delta-sigma based transmitters [26], this type of transmitter has some serious advantages like linearity and PA efficiency [28].

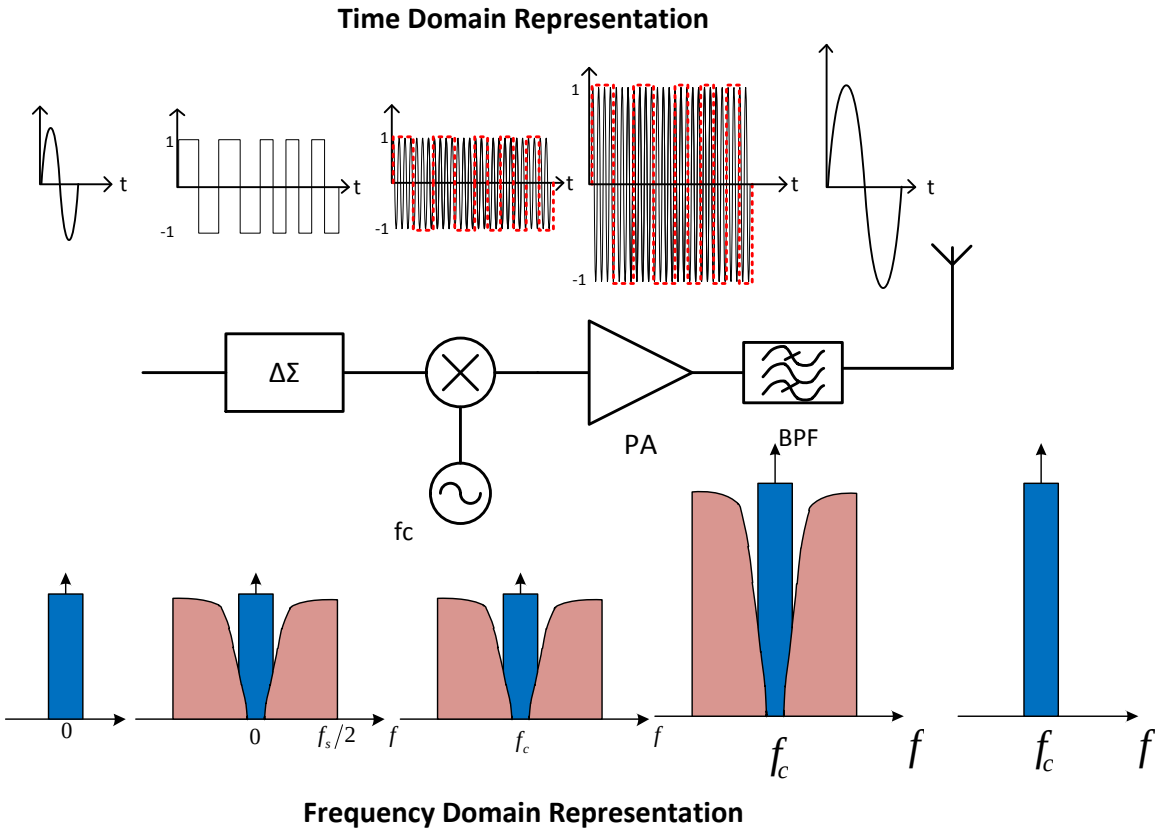


Figure 2-14 . Generic block diagram of DSM based transmitter architecture [3].

However, these transmitter architectures are designed for single band applications. For implementing in dual band spectrum aggregation application DSM and the PA needs to be redesigned. Architecture incorporating DSM for dual band spectrum aggregation technique consisting of several linear PAs was reported in [53][54]. Nevertheless, the method proposed for DSM outputs a multi-level signal which is difficult to employ for driving SMPA. Moreover, the DSM architecture proposed has some stability issues and gets unstable for certain signals.

Chapter 4 proposes DSM architecture to address the stability and complexity issue for concurrent dual band spectrum aggregation transmitter application.

2.4 Conclusion

The basic aspects of delta-sigma modulators (DSMs) have been reviewed in this chapter. Three major parallel architectures have been discussed extensively along with the literature review for them which lay all the groundwork for the work done in this thesis. Based on these discussions the contributions of this thesis will be presented in the subsequent chapters.

Chapter Three: Low Complexity Frequency Band Decomposition Based Delta-Sigma Modulator

3.1 Introduction

A low complexity parallel architecture for wideband analog to digital conversion is proposed in this chapter. The proposed Frequency Band Decomposition (FBD) approach employs frequency down conversion of the input signal along with low-pass delta-sigma modulators (DSMs) and low-pass filters, resulting in a less complex architecture. Several simulations and FPGA implementation were performed to verify the proposed theory.

3.2 Proposed Frequency Band Decomposition Based DSM

The proposed parallel architecture for delta-sigma modulator (DSM) is based on frequency band decomposition (FBD) shown in Figure 3-1. This architecture is inspired from the theory of the mixer operation.

In this architecture a wideband input signal is simultaneously fed to all the parallel channels. Each channel consists of two mixers, a low-pass delta-sigma modulator (LPDSM), and a low-pass filter. In each channel the different segments of the wideband input signal are transferred to baseband. Then they are fed to a low-pass delta-sigma modulator. For simplicity of the design a second order delta-sigma modulator has been employed in this work. The output of the DSM is then filtered with a low-pass filter. As the complexity is attempted to be reduced in this proposed architecture the filter employed has all the same specifications in terms of frequency response and coefficients. The filtered signal is then shifted back to its original position and the outputs of all channels are added together to obtain the wideband output.

In most of the parallel delta-sigma modulators discussed in chapter 2 as well as conventional FBD, the discrete time input signal is heavily upsampled/oversampled and filtered

with an anti-aliasing filter to remove the spectral replicas before it is fed to actual delta-sigma. However, in the proposed model a discrete time signal is directly fed to the system after oversampling 'K' times and the oversampling ratio is also kept very low inside the FBD.

This methodology envisages the wideband signal to be divided into several segments and the center frequency of each segment are shifted to the baseband for processing with a low-pass DSM. The number of parallel channels depends on the number of segments used.

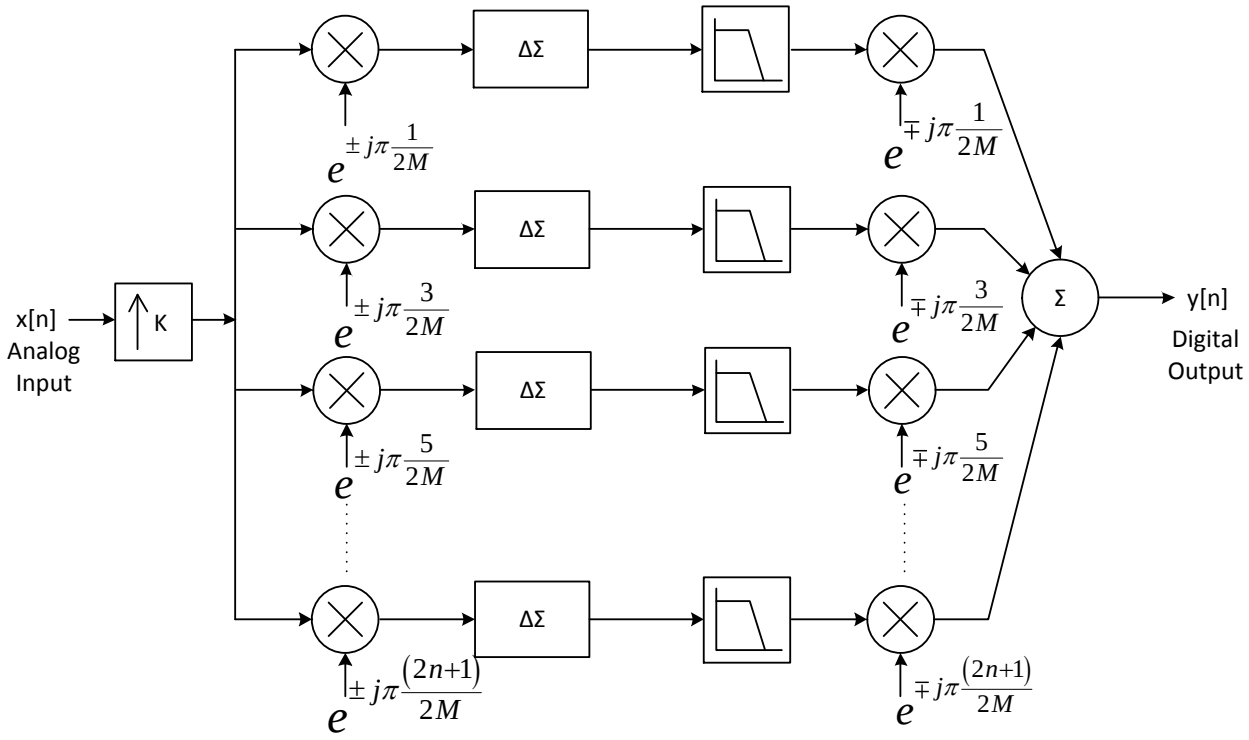


Figure 3-1. Proposed low complexity FBD Architecture.

The output signal frequency of the mixer is the absolute value of the difference of the frequencies of the two inputs signals. When down-converting the part of the signal to the baseband, the relationship between the input and output frequency of the mixer is given by

$$f_{IF} = \left| f_{LO} - f_{IN} \right| \tag{3-1}$$

From the above equation it can be derived that, if a signal is multiplied with a second signal with the center frequency of that of the first signal the output signal will be shifted to the baseband.

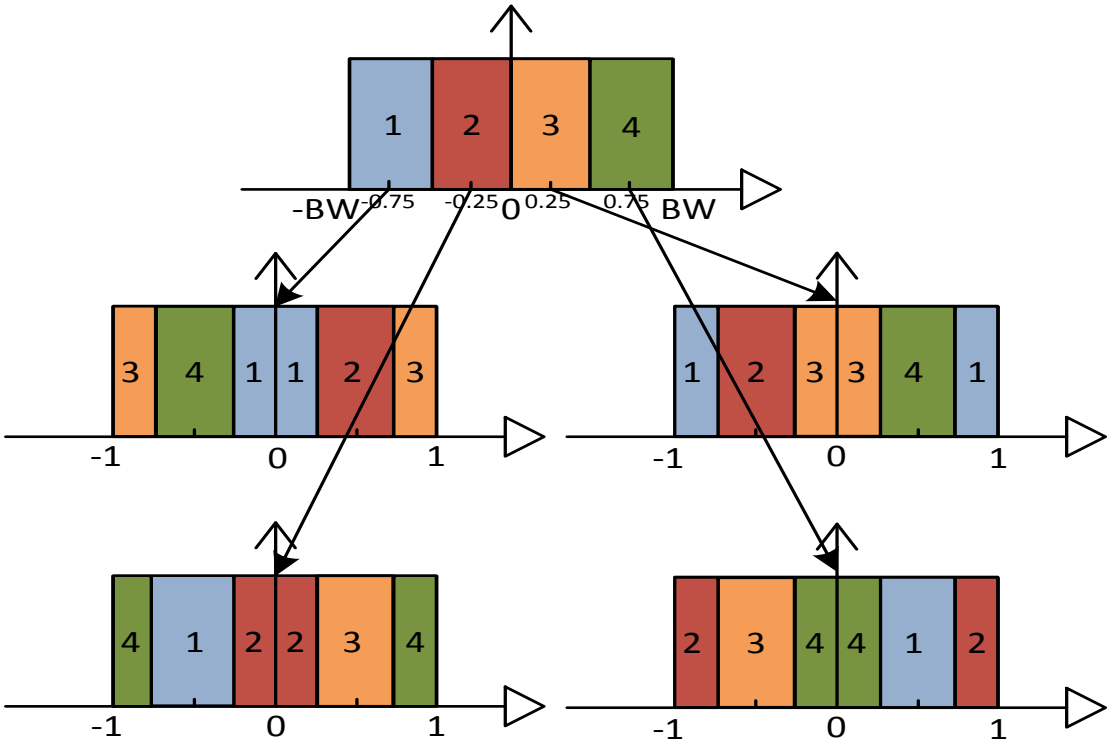


Figure 3-2. Shifting the signal frequency in the proposed model.

In this thesis a four channel FBD based DSM has been designed, in which the wideband signal is divided to four sub-band signals. As shown in Figure 3-2, different segments of the wideband signal are transferred to the baseband by multiplying the center frequency of that particular segment. The frequency calculation for the input of the complex mixer is given by,

$$\omega_c = \pm\left(\frac{2n+1}{2M}\right)\pi \tag{3-2}$$

Where $0 \leq n \leq M-2$ and $M \in \mathbb{N}$ is the number of channels. Bandwidth of the signal processed by each channel is,

$$BW_c = \frac{BW}{2M} \tag{3-3}$$

The FBD structures discussed in the literature employ BPDSM and HPDSM for processing different segments of the signal other than the baseband, whereas in the proposed method a low order (e.g. second order) low-pass DSM has been used. The transfer function of the second order delta-sigma modulator is given by,

$$Y(z) = z^{-1}X(z) + (1-z^{-1})^2 E(z) \tag{3-4}$$

So the STF of the second order delta-sigma modulator is just a delay and the NTF(z) = $(1-z^{-1})^2$.

As we are employing low-pass delta-sigma modulators which have a defined conversion bandwidth, any frequency outside the band of interest of the modulator can be treated as the quantization noise and can be shaped outside the band of interest. In this architecture, this feature of noise shaping is utilized for the purpose of reducing the complexity of the design and resources involved in the implementation of the model. After the oversampling of the signal the proposed architecture does not employ any other stage of filtering before it is processed by DSM. Therefore, all the other out-of-band replicas of the signal spectrum and the part of the signals, outside the band of interest, are treated as the quantization noise as shown in Figure 3-3. The proposed model discards the filters from the front part of the modulator as it can be seen from Figure 3-1. This idea significantly reduces the complexity and the resources required which is also verified through FPGA implementation.

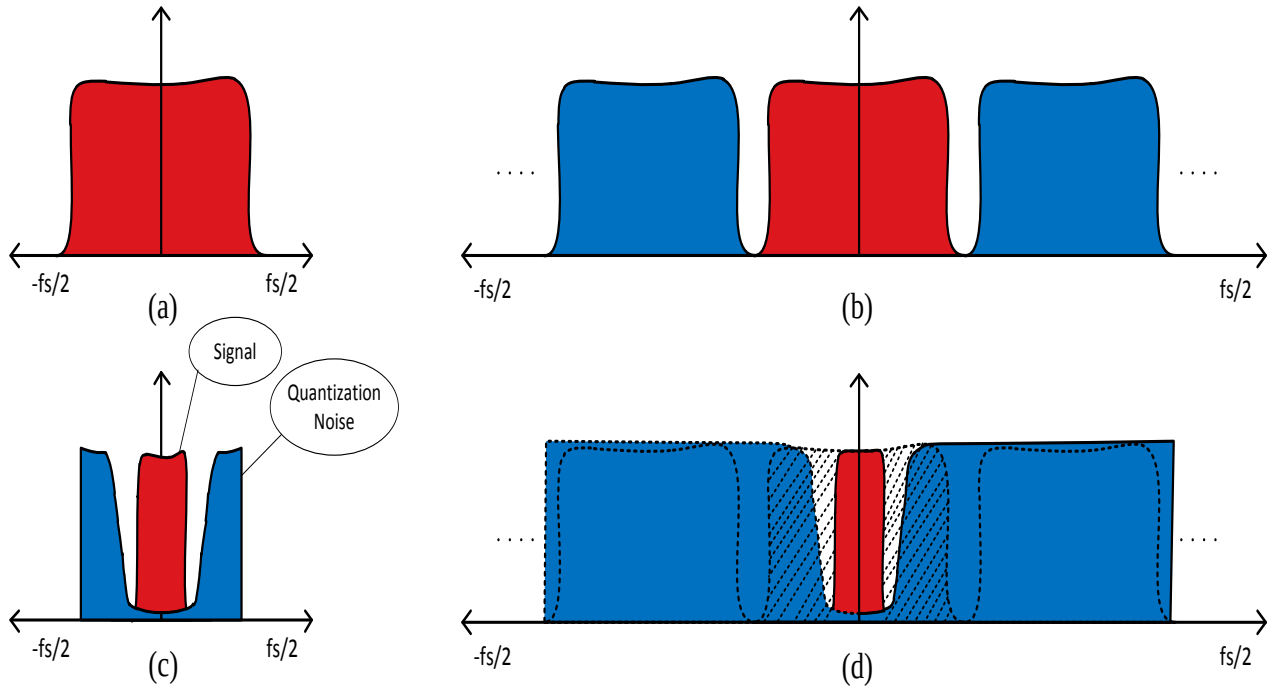


Figure 3-3. (a) Wideband signal, (b) Signal spectrum after oversampling, (c) Signal and noise shaping response of LP DSM, (d) Output of DSM with the upsampled wideband signal as input.

An identical low-pass FIR filter is employed in all the channels to filter the shaped out-of-band noise. The order of the filter, window type and the cutoff response/roll of factor have very little impact on the resolution of the architecture. It has been found that, the resolution varies less than 1 bit if a low order low-pass filter is employed instead of a very high order sharp cutoff response low-pass filter.

The overall operation can be summarized through the following expression.

$$W(z) = X(e^{j\omega_c} z) \quad 0 < n < M - 2 \tag{3-5}$$

$$Y(z) = \sum_{n=0}^{M-2} \left[\{P(e^{-j\omega_C} z)\} \right] \tag{3-6}$$

Where, $Y(z)$ is the final output, and $P(z)$ is the filtered output of DSM and is given by:

$$P(z) = W(z)H(z)F(z) \tag{3-7}$$

$H(z)$ and $F(z)$ is the frequency response of DSM and low-pass filter respectively. As it can be interpreted from (3-6), the proposed structure reduces the complexity of the FBD design considerably. In the following sections, simulation and FPGA implementation results supporting these statements are presented.

3.3 Simulation Results

In this work, MATLAB and SIMULINK were extensively utilized for the simulation of the proposed low complexity FBD. To demonstrate the architecture performance discussed earlier a four channel FBD was designed and simulated. An LTE signal with 2MHz bandwidth was considered for the proof of concept. An OSR of 8 has been employed when designing the proposed architecture. The clock speed required for the proposed FBD modulator was 16 MHz.

As the simulated proposed model has 4 channels and has an OSR of 8 the overall performance should be equivalent to a modulator with OSR of 32. Table 3-1 shows the simulation results of the SNDR for proposed modulator and second order DSM.

Table 3-1. Comparison of Simulated SNDR of FBD modulator and non FBD modulator for LTE signal.

Architecture	Channels	BW (MHz)	OSR	Clock (MHz)	SNDR (dB)
Proposed FBD DSM	4	2	8	16	45.58
2^{nd} Order DSM	1	2	32	64	46.9

The results demonstrate that the clock speed was significantly reduced with very negligible SNDR degradation.

A comparison of complexity between the conventional QMF FBD and the proposed FBD architecture is shown in terms of resources allocated in Table 3-2. It can be observed that as the complexity of the conventional QMF FBD model is higher the number of resources allocated is very high, whereas the numbers are substantially low for that of the proposed model. The proposed model shows significant complexity reduction in term of resources employed.

An SNDR degradation comparison between the MATLAB simulation and FPGA implemented model was also done which shows in Table 3-3.

Table 3-2. Resource utilization comparison for Conventional QMF FBD and Proposed FBD model.

Model	Slices	FFs	BRAMs	LUTs	Mults/DSP48s
Conventional QMF FBD Model	6037	18394	12	11233	984
Proposed FBD Model	1904 (68.46%↓)	1834 (90%↓)	0 (100%↓)	2832 (74.78%↓)	104 (89.43%↓)

Table 3-3. SNDR degradation comparison between MATLAB simulated and FPGA implemented model.

Model	SNDR(dB)
MATLAB/Simulink	45.58
Xilinx Sysgen (Fixed point implementation)	45.33

Figure 3-4 shows the input and output spectrum of the proposed FBD architecture.

Effect of different filter length on SNDR degradation was also simulated which shows in table 3-4. It is observed that there is a minimal degradation of SNDR when the order of the filter (no. of taps) in reduced. With the Chebyshev window and only 200 taps, a very promising performance has been achieved.

Table 3-4. Performance comparison for different filter types.

Filter Type	Fstop/Cut-off	Filter Order	SNDR
LP-equiripple	$1.016\times\pi/8$	11231	45.79
LP-equiripple	$1.35\times\pi/8$	463	45.09
Chebyshev	$1.1\times\pi/8$ [Cut-off:0.15]	200	45.25

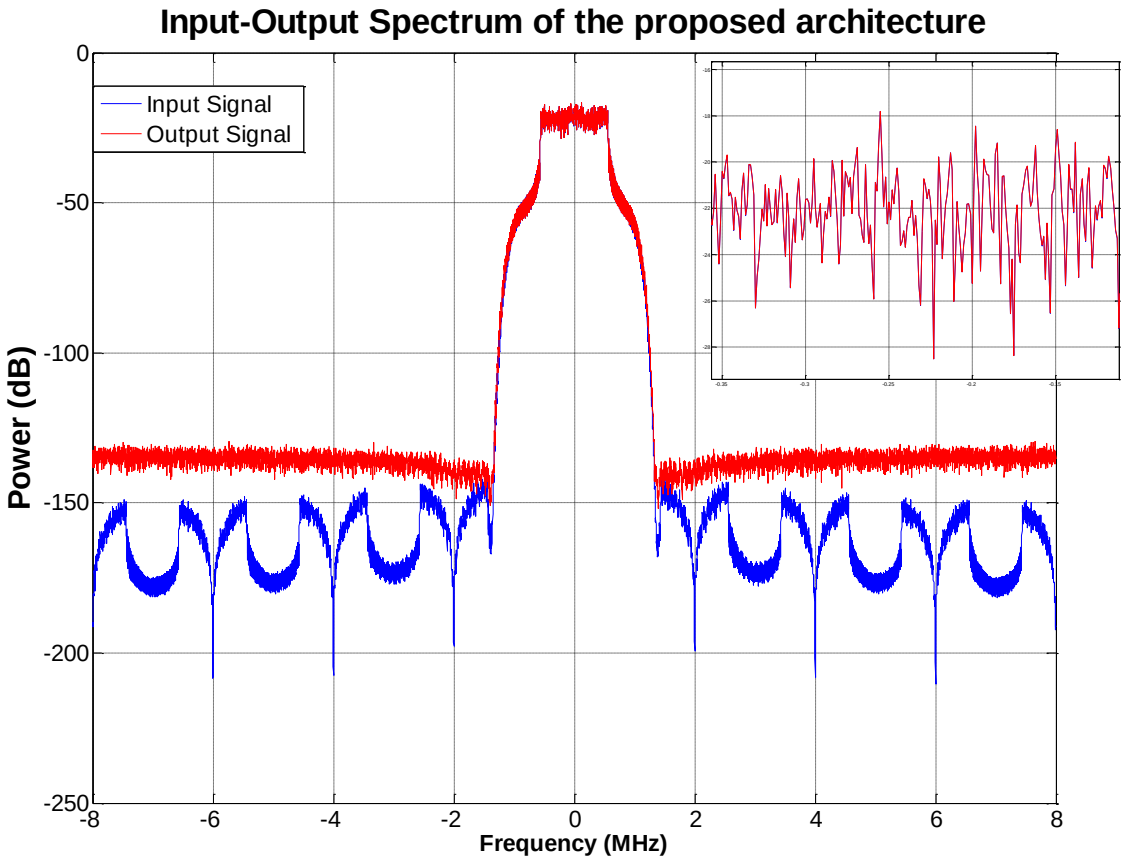


Figure 3-4. Input-Output Spectrum of the proposed FBD architecture simulation.

3.4 FPGA Implementation

The Xilinx System Generator and Simulink were employed to model and implement the design on to the FPGA. Xilinx System Generator is a division of the ISE® Design Suite and provides Xilinx Blockset such as adders, multipliers, registers, filters, memories etc. in the Simulink environment for application specific design. Parameters and constraints that are required to be considered while implementing FBD based DSM on FPGA were the bandwidth of the signal (BW), sampling frequency (f_s), clock of FPGA (f_{FPGA}), input signal for complex multipliers, filter length and fixed point data length calculation for each stage.

The proposed model for the FBD based delta-sigma modulator has four branches and the signal is upsampled before it is fed to the parallel branches. A modulator consists of delay blocks, adder, subtractor and a comparator as quantizer. Each branch also has a complex multiplier as mixer and an FIR for low-pass filter. Figure 3-5 shows a single channel of the four channel FPGA implementation.

3.4.1 FPGA Clock

When implementing a model in an FPGA the first thing that needs to be considered is determining the highest frequency component in the whole system chain, as the FPGA clock (f_{FPGA}) or the system clock is always equal to or greater than the highest frequency in the system. All the other clocks for different components are the ratio to the FPGA system clock if there is any other rate changing operation happens in the system.

Bandwidth (BW), sampling frequency (f_s), and oversampling ratio (OSR) play a great role in determining the FPGA clock. An increase in BW will also change the other parameters as well as increasing the f_{FPGA}. If there is a multiplexer or up-sampler in the system the output frequency needs to be considered. In this implementation the oversampling/up-sampling is part of the architecture so the output frequency of the up-sampler was taken into consideration.

Finally, the maximum clock of the FPGA system is one of the major factors to take into consideration. The FPGA clock delivering a good performance might not be the maximum usable FPGA clock. However, the operating FPGA clock must be less than the maximum usable FPGA clock. So the bandwidth, OSR and FPGA clock relationship for the proposed architecture becomes,

$$f_{FPGA} \geq OSR \times BW \tag{3-8}$$

For this particular implementation, the sampling rate of the signal changes only once during the up-sampling of the signal at the very beginning of the chain. So that is the highest clock of this system. Additionally a rather low OSR of 8 was used for this architecture. Taking a 2MHz bandwidth signal as an example, the FPGA clock will be only 16 MHz, which is considerably low compared to other different architectures.

3.4.2 Fixed Point Arithmetic Application

When a model, component, or filter is simulated in MATLAB or Simulink, it uses a very high degree of precision for calculation namely double precision floating point. This does not pose much of a problem in software simulations, as computers have larger memory and more bits for processing a calculation with a very high level of precision. However, implementing a model on hardware is different due to the finite number of bits. FPGA and other DSP processors employ fixed point arithmetic for implementation to deliver a certain level of precision. This reduction in precision arises some quantization error and differs from the simulated values. FPGA utilizes 2's complement fixed point rational number for data representation and calculation.

The range of values an N-bit binary word interpreted as 2's complement fixed point rational can take is given by [55]:

$$P = \{ p / 2^b \mid -2^{N-1} \le p \le 2^{N-1} - 1, p \in \mathbb{Z} \} \tag{3-9}$$

Where, P consists of 2^N elements. This kind of representation is denoted as $A(a,b)$; here $a = N - b - 1$. An N-bit binary number x can be written as

$$x = (1/2^b)\left[-2^{N-1} x_{N-1} + \sum_{0}^{N-2} 2^n x_n \right] \tag{3-10}$$

Where, x_n is the n bit of x. The range of $A(a,b)$ representation,

$$-2^{N-1-b} \le x \le +2^{N-1-b} - 1/2^b \tag{3-11}$$

From (3-10) and (3-11), the most significant bit (MSB) is the signed bit and $A(a,b)$ representation requires $a+b+1$ bits.

There are some bit growths for every arithmetic operation. For addition of two M bits requires $M+1$ bits to represent the output. So there is a bit growth of 1. Multiplication of two signed numbers $A_1(a_1,b_1)$ and $A_2(a_2,b_2)$ results in,

$$A_1(a_1,b_1) \times A_2(a_2,b_2) = A_3(a_1+a_2+1, b_1+b_2) \tag{3-12}$$

Dividing $A_n(a_n,b_n)$ by $A_d(a_d,b_d)$ gives,

$$\frac{A_n(a_n,b_n)}{A_d(a_d,b_d)} = A(a_n+b_d+1, a_d+b_n) \tag{3-13}$$

During the implementation, the bit growth for each operation in each branch has been analyzed and word length was calculated for each component. However, the maximum length of the bit-width is limited for the whole system and therefore each component.

For internal quantization and overflowing of bits, truncation and saturation were employed. Nonetheless, 'Rounding off' option for overflowing of bits, was not taken because it arises output rounding off noise, affects SNDR and occupies more internal resources of FPGA.

3.4.3 Resource Optimization

After construction of the whole system, input bit length and bit growth after each component has been carefully analyzed and checked for appropriate bit length. At this stage the

main challenge was optimizing for delta-sigma modulator feedback loops because of the bit growth. In the inner feedback loop the bit growth is very high (over 4000 bits) which needs to be optimized.

As delta-sigma modulator has more than one feedback loop, tracking and calculating bit growth for each component inside the loop is difficult. The steps followed for this procedure is as follows

1. There are four feedback loops in a second order DSM. Two of the loops are independent and the others are dependent. At first we start opening the feedback loops one by one starting with the outermost loop. This will change the output of the system which however is not of concern at this stage. Figure 3-5 shows the feedback loops of DSM and opening of the loops.

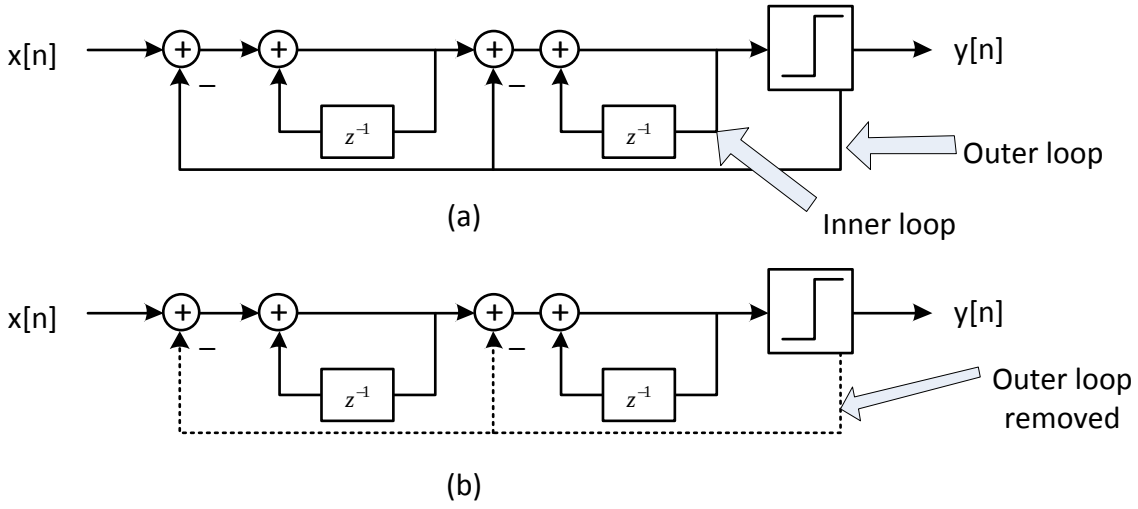


Figure 3-5. (a) Inner loops and outer loops of second order DSM, (b) Outer loops removed for bit growth investigation.

2. After opening each loop, the bit growth of the component in that open loop was investigated by adding output probe and collecting data from the inner loops. From the

bit growth data, the number of bits required to maintain the quality (SNDR) was determined for each adder.

3. We started connecting the outer feedback loops again one by one. After connecting each feedback loop the bit growth for that loop is checked and required bit length is calculated. For each loop the whole process was repeated couple of times to find out the appropriate bit length so that the bit length in the loop doesn't overflow.

Determining the bit length for FIR filter coefficients was also rigorous process. For FIR filters, at first the calculation was done with full precision. In the second stage the fixed point arithmetic as mentioned above was employed to find the proper bit length. In this process the precision of the coefficients also reduced from floating point to fixed point length.

To justify the resource calculation, all components of both conventional and proposed parallel FBD delta-sigma are optimized precisely in terms of bit width.

3.5 Conclusion

In this chapter a low complexity Frequency Band Decomposition based DSM parallel architecture for wideband A/D conversion is introduced. By employing the proposed technique, the design complexity is reduced and the FPGA resource is reduced considerably. The proposed architecture has been validated through simulation and FPGA implementation using an LTE signal.

The parameters considered and calculated for implementing this architecture on FPGA were discussed in detail. For a 4-channel proposed FBD delta-sigma modulator, the results showed an SNDR around 46 dB for an LTE signal with 2 MHz bandwidth and an OSR of 8 at

the output of FPGA, almost equal to a one channel delta-sigma modulator with 32 times oversampling.

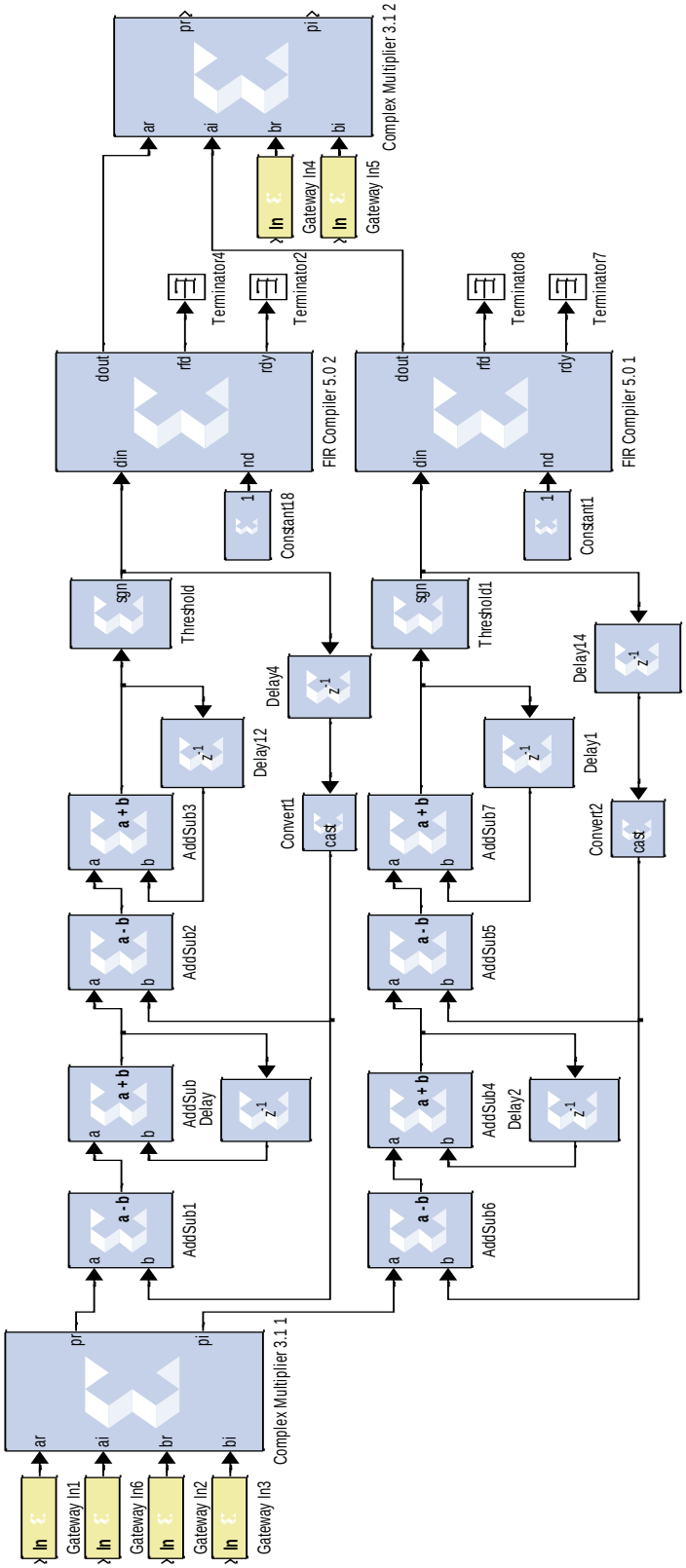


Figure 3-6. Single channel of the proposed 4 channel Frequency Band Decomposition based Delta-Sigma Modulator.

Chapter Four: Concurrent Dual Band Delta-Sigma Modulator for Spectrum Aggregation Transmitter Application

4.1 Introduction

With the convergence of different communication systems, the bandwidth requirement for next generation communications has increased to a great extent. Next generation mobile communication systems like IMT-advanced requires a very wide bandwidth of 100 MHz to provide mobile transmission data services at a rate of 1Gbps [2][53][54]. Integrating several separate frequency bands can be one such solution, for which flexible, reconfigurable, multi-standard all digital software defined radio SDR transmitter is great candidate [2][23][53]. All digital transmitter architecture incorporating DSM reported in literature [4][23][27] shows very promising performance for modern radio systems. The basic idea for delta-sigma modulator based transmitter was discussed in chapter 2. However, in this chapter we discuss about a new low complexity delta-sigma modulator for dual band spectrum aggregation transmitter application.

Concurrent dual band transmitter was presented in [53] which incorporates delta-sigma modulator to drive the PA. The architecture of DSM presented in [53] can easily get unstable for the second frequency. The second model presented by the same author [54], employs the idea of offset frequency as an IF stage for input signal, which mitigates some of the high speed requirements, however the approach still suffers from some stability and complexity problems of delta-sigma modulator.

In this chapter, a low complexity novel delta-sigma modulator architecture for the concurrent dual band spectrum aggregation transmitter [53][54] is presented. The novelty lies in flexibility, complexity and stability of the design of the DSM. The transmitter architecture that

was presented in [53] is modified for concurrent dual band application which addresses a solution for digital signal combining and PA issues by employing multiple switching amplifiers for multi-level signal. Nonetheless the main focus of this research work was to develop delta-sigma modulator suitable for concurrent dual band spectrum aggregation application which is also highly reconfigurable. A detailed method of calculation of frequency planning for noise shaping is provided. A reprogrammable and stable transfer function for desired noise shaping function is also proposed. This design of the DSM is inspired from Kitayabu et al paper [53][54]. Simulation results verify the concepts presented. Designing a digital combiner for generating bi-level signal to drive single PA for the concurrent dual band signal is left as future work.

4.2 Concurrent Dual Band Transmitter Architecture

Figure 4-1 shows a block diagram of the digital transmitter architecture for concurrent dual band application [53]. The architecture is similar to the transmitter presented in [3][4][23][27] and has three main stages:

a) Digital Signal Processing (DSP) stage.

b) Noise shaping and digital up-conversion stage.

c) Amplification, combining and filtering stage.

The digital signal processing (DSP) stage is responsible for transmitter settings, modulation of the signal that will be transmitted. The baseband IQ signal for each carrier f_1 and f_2 is generated from the DSP stage which is denoted as I_1, Q_1 and I_2, Q_2 respectively.

In the noise shaping and digital up-conversion stage, the IQ signals from the DSP stage is converted into constant envelop signal and the quantization noise generated in the process is shaped in such a way that the out-of-band noise of one signal doesn't affect the in-band noise of

the other signal after digital up-conversion. The noise-shaped constant envelop signal is then up-converted digitally using a 4×1 multiplexer and fed to the next stage.

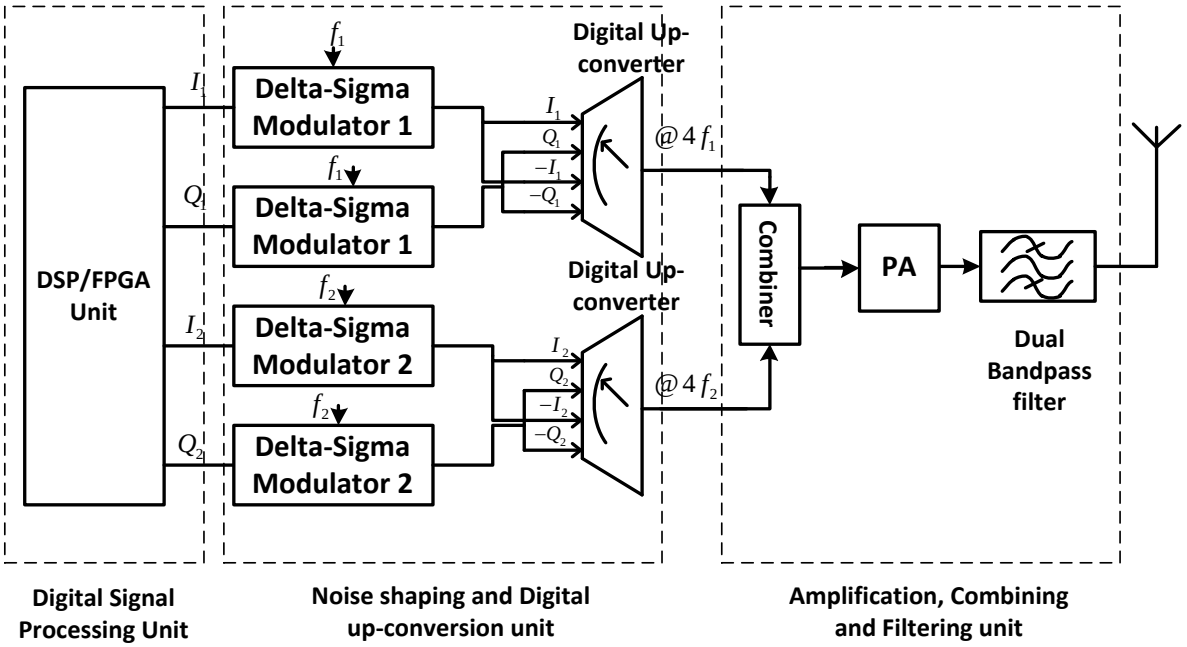


Figure 4-1. Concurrent dual band transmitter architecture block diagram [53].

The main difference between this transmitter and a single band transmitter is the noise shaping of the delta-sigma modulator. The noise shaping of DSM is designed such a way that two different frequencies can be transmitted together without quantization noise interference. The transmitter architecture presented in [53][54] combines the signals after digital up-conversion and feeds to the linear amplifier. However, adding the two signals together changes the bi-level signal to a multi-level signal which is not suitable for SMPA. Kitayabu et al proposed a control unit where the number of levels of the combined signal contributes to the number of PAs employed. In this method two types of quantizer namely 'mid-rise' and 'mid-tread' were utilized for two different DSMs which ended up with a multi-level signal after combining. To utilize this multi-level signal for power amplifier, the method employs a PA for each level which led to 9 PAs.

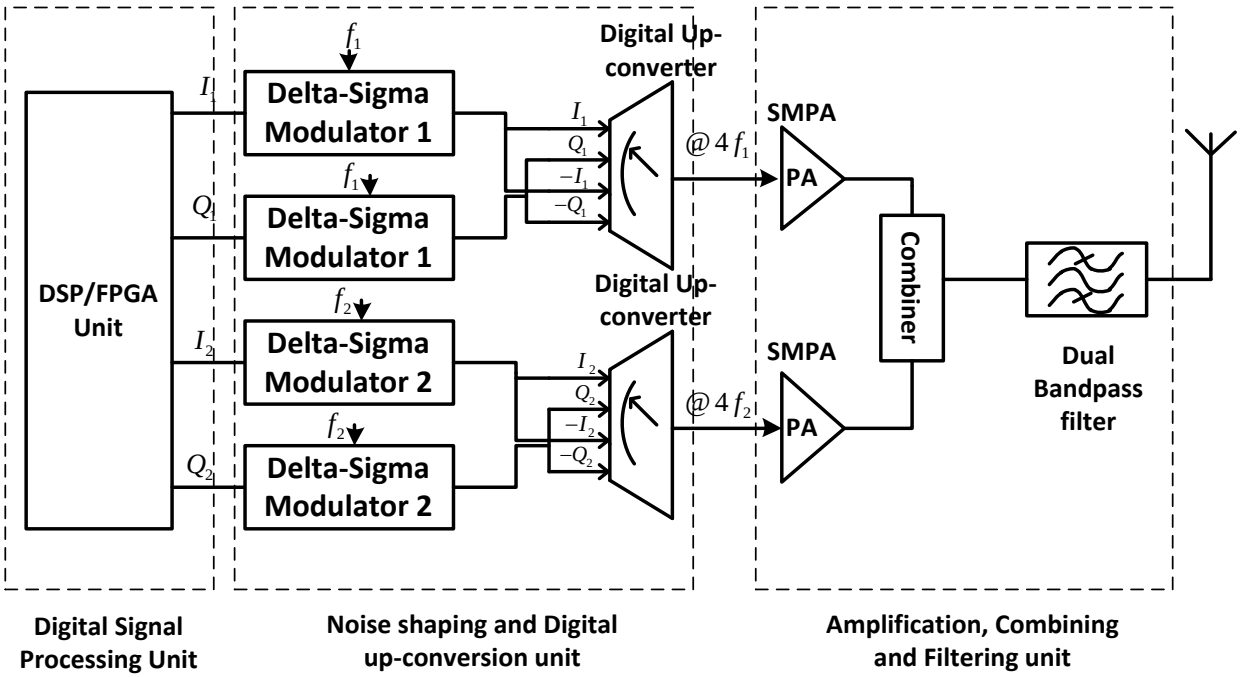


Figure 4-2. Proposed alternative concurrent dual band transmitter architecture block diagram.

Figure 4-2 shows a block diagram of proposed alternative model for transmitter architecture, where switching mode power amplifier (SMPA) is employed, which is directly driven by the output of digital up-converter. The output of the SMPA is combined in the analog domain with a combiner. However, combining signals in the analog domain has some issues such as requirement of high power combining and interaction effect of SMPAs on each other. In this work, mostly the design of DSM has been emphasized and the signal combining is left as future work.

4.3 Concurrent Dual Band Delta-Sigma Modulator and Spectrum Aggregation Idea

A low-pass delta-sigma modulator (LPDSM) generally utilized in a transmitter, pushes the in-band quantization noise to outside the band of interest to the higher frequencies. For band-pass delta-sigma modulator (BPDSM), the quantization noise is also shaped outside the band of interest and pushed to both the sides (high frequency and low frequency). However, in both the

cases if two signals with two different frequencies are intended to be employed concurrently, the out-of-band noise of each signal will overlap and interfere with each signal and increase the in-band noise and degrade the overall signal quality. Hence, these DSMs cannot be utilized for concurrent dual band application.

For concurrent dual band spectrum aggregation application, as two frequencies need to be transmitted, the noise transfer function of the dual band-pass delta-sigma modulator is designed such that it has two frequency notches/quantization null for two frequencies. Two transfer functions are designed for two frequencies, where each of them has the quantization nulls for both the signals. While designing the transfer function, the concept of digital up-conversion is also taken into consideration as both of the signals will be up-converted before addition. Figure 4-3 (a), shows how the out-of-band noise can degrade the signal if the noise is not shaped for concurrent dual band application. Figure 4-3 (b), shows the concept of the noise shaping in the concurrent dual band delta-sigma modulator. In this process the frequency notches will be translated to different higher frequencies according to their positions in the low frequency spectrum. The model presented here is reconfigurable for different frequencies. The following sections describe the frequency planning and reprogramming of the transfer functions according to the signal frequencies and the noise nulls.

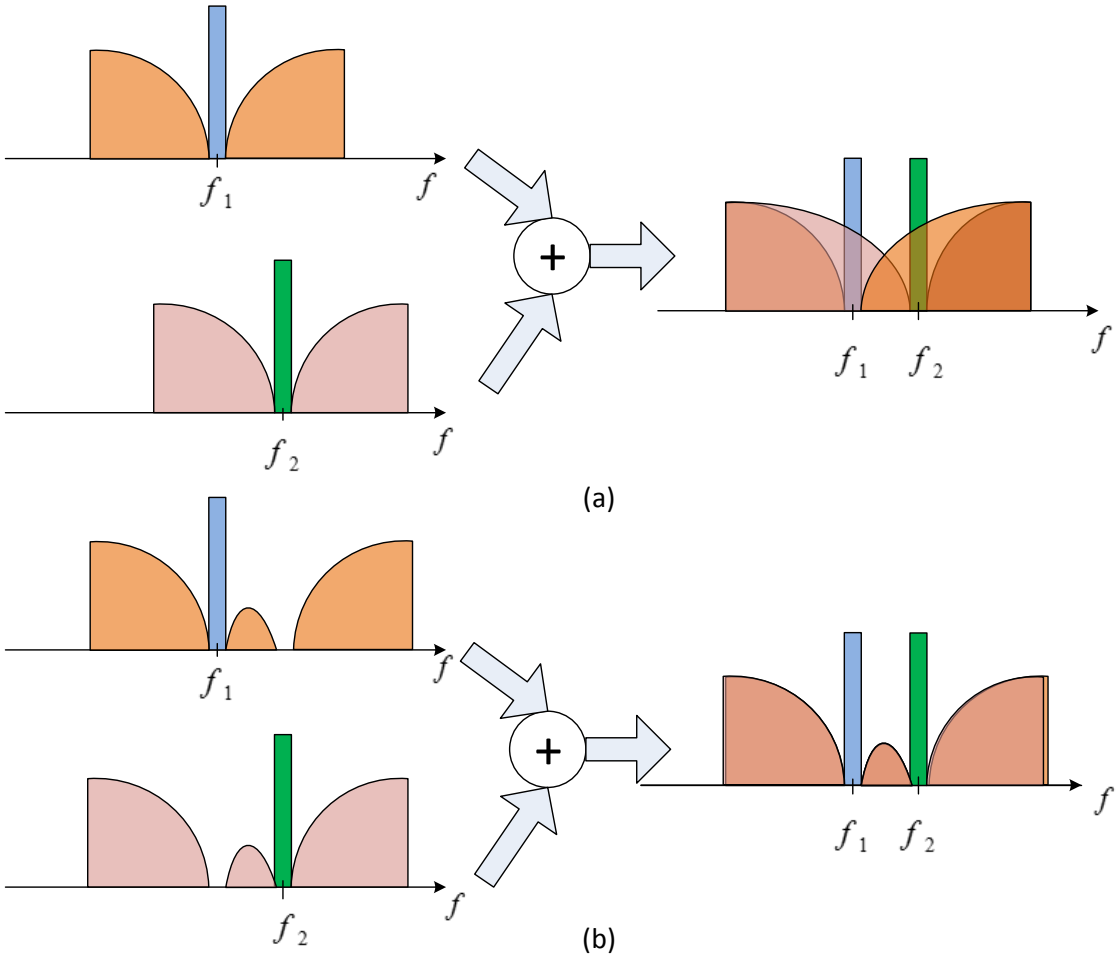


Figure 4-3. (a) Noise shaping of LPDSM and signal degradation while used for concurrent frequencies and (b) Appropriate noise shaping for the concurrent dual band-pass DSM [53][54].

4.3.1 Frequency Planning for Noise Shaping

If two frequencies, f_1 and f_2 are selected for concurrent application, where $(f_1 < f_2)$. Keeping in mind about M times digital up-conversion, where $M = 4$ in this case, the noise shaping notches has to be calculated so that at the output of one DSM, the first signal has the notch to fit the second signal and vice-versa. During the digital up-conversion, the quantization nulls gets

translated to the higher frequencies, and hence both the signals can be fit it in the same spectrum for concurrent transmission.

While calculating the zeroes or the quantization nulls for designing the transfer function, we always keep a zero at the baseband or '0' (zero) position and oversample the baseband signal accordingly to achieve the desired carrier frequency. The reason for keeping a zero at the baseband is that, the input signal of the DSM is carrier frequency baseband signal which needs to be converted to constant envelope. Therefore to obtain the original signal at baseband along with the shaped quantization noise at the output of DSM, a zero is kept at baseband then the other quantization null points are calculated. The baseband zero gets translated to the desired carrier frequency along with the signal at that position during the up-conversion process. Similarly if there is a quantization null at "π" position it also gets translated according to the change of sampling rate.

As mentioned above for the two frequencies f_1 and f_2 where $f_1 < f_2$, the Nyquist zone calculation is done to find out where the two signals fall into each other's Nyquist zone. When $f_1 < f_2/2$, which means the first frequency f_1 is in the first Nyquist zone of the second frequency f_2, the desired noise shaping notch position to fit in the first signal (f_1) for the second noise transfer function is calculated as,

$$x_2 = (\frac{f_1}{f_2/2})\pi \tag{4-1}$$

Where x_2 is the normalized frequency position in the normalized spectrum of the frequency f_2 for the noise shaping notch.

If $f_1 > f_2/2$, which means the frequency f_1 is in the second Nyquist zone of the frequency f_2, the notch position is calculated as,

$$x_2 = (\frac{f_2 - f_1}{f_2/2})\pi \tag{4-2}$$

Where, x_2 gives the second notch position, after the notch at zero, in the normalized spectrum of the second signal of f_2. The next quantization null frequency before and after f_2 can be found at,

$$X_{f_2} = f_2 \pm x_2 \times f_2/2 \tag{4-3}$$

To understand the calculation better, we take two frequencies $f_1 = 800MHz$ and $f_2 = 2GHz$ as an example. Here the frequency f_1 falls in the first Nyquist zone of f_2; hence the (4-1) should be employed to find x_2 which is 0.8π

Because we are programming the notches accordingly to fit both the signals together when added, so that at the notch of the second signal the first signal can fit in. The quantization null position for the first signal also has to be programmed in such a way that it can get translated at the frequency of the second signal when digital up-conversion is done.

When $f_1 < f_2/2$ i.e. the frequency of the first signal f_1 is inside the first Nyquist zone of the second signal f_2, the calculation of the position of the quantization null for the first signal becomes,

$$x_1 = (\frac{f_2/2 - f_1}{f_1/2})\pi \tag{4-4}$$

Here, x_1 is the desired normalized frequency position of the notch in the normalized spectrum of the frequency f_1 for noise shaping of the first signal.

Now, if $f_1 > f_2/2$ i.e. the first frequency f_1 falls in the second Nyquist zone of the second frequency f_2, then we have to consider two cases depending on Δf . Where Δf is given as,

$$\Delta f = |(2f_1 - f_2)| \tag{4-5}$$

The parameter Δf provides the difference or the distance between f_2 and the replica of f_1 at the second Nyquist zone, which helps to determine how much adjustment, is needed to get the desired notch position. If $\Delta f > f_1/2$, the desired frequency notch is at,

$$x_1 = (\frac{f_1 - \Delta f}{f_1/2})\pi \tag{4-6}$$

However, when $\Delta f < f_1/2$ the calculation becomes,

$$x_1 = (\frac{\Delta f}{f_1/2})\pi \tag{4-7}$$

In this process we can make sure that this quantization null will be translated at the position of the second signal with the digital up-conversion process. The actual notch positions for the first signal are located at,

$$X_{f1} = f_1 \pm x_1 \times f_1/2 \tag{4-8}$$

If we consider the same frequencies in the aforementioned example, two frequencies $f_1 = 800MHz$ and $f_2 = 2GHz$. Here the frequency f_1 falls in the first Nyquist zone of f_2, hence the (4-4) should be employed to find the required notch x_1 which is 0.5π However if

$f_1 = 1100MHz$, in this case f_1 falls in the second Nyquist zone of f_2 and therefore (4-5) and (4-7) need to be employed to find out the notch position x_1 which is 0.36π

In this technique of calculating frequency positions and quantization noise nulls the most important aspect to be take into consideration is the frequency spacing between the two signals. Where the signals stand in each other's Nyquist zones, is a very important factor for consideration. The equations above were derived considering the characteristics of the digital up-converter as it makes replicas of the delta-sigma modulated signal by M times the respective carrier frequencies.

The delta-sigma modulator was considered as fourth order in this segment, which means the transfer function has only two quantization nulls (four zeroes). Thus the calculation was done only for the second nulls as we always take the first noise null at zero. However if the order of the DSM is increased, the calculation for the intermediate quantization nulls has to be taken into consideration accordingly. The next section discusses the DSM architecture proposed in this research and how the quantization null calculation can be applied for programming the transfer function.

4.3.2 Modulator Architecture

Figure 4-4 (a) shows the architecture of the delta-sigma modulator proposed in this work. The modulator model is inspired from feed-forward DSM model. The major advantage of this model is that, it is highly flexible in terms of defining noise transfer functions. If we replace the quantizer with a noise source and an adder as in figure 4-4 (b), the input and output relationship of the DSM can be calculated as,

$$Y(z) = X(z) + H(z)E(z) \tag{4-9}$$

Where $Y(z)$, $X(z)$, and $E(z)$ are the z-domain representation of output signal, input signal, and the quantization noise respectively.

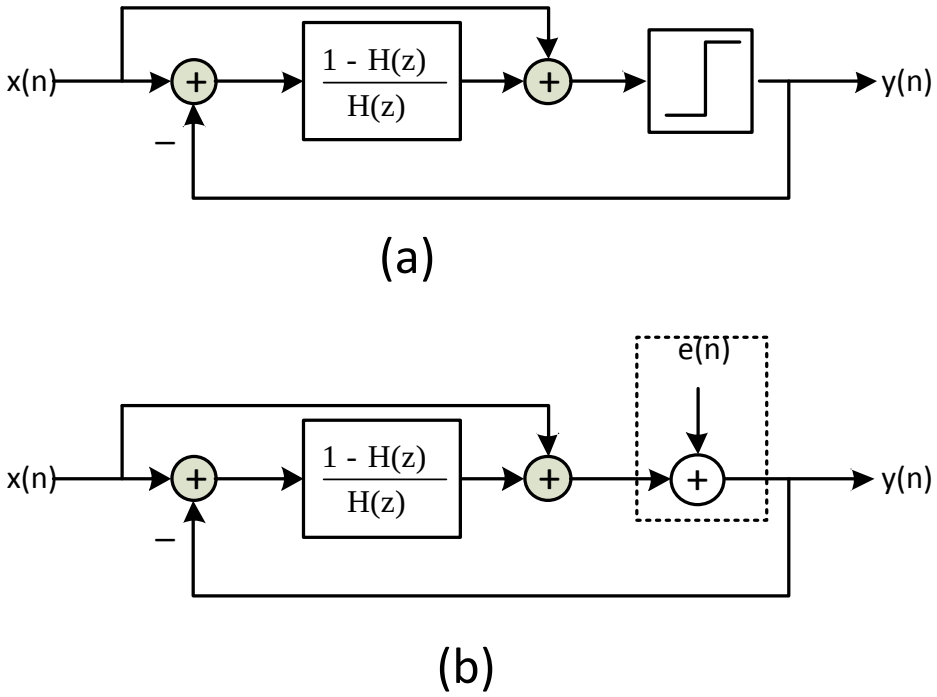


Figure 4-4. (a) Proposed DSM architecture for concurrent dual band operation. (b) Quantization noise modeling for proposed DSM.

From (4-9) the signal transfer function (STF) and the noise transfer function (NTF) is given by,

$$STF(z) = 1 \tag{4-10}$$

$$NTF(z) = H(z) \tag{4-11}$$

The order of the noise transfer function (NTF) is the order of the DSM in the proposed model. In this segment of the research we considered a fourth order NTF. The generalized noise transfer function (NTF) $H(z)$ is given by,

$$H(z) = (1 - 2\cos(\varphi_1)z^{-1} + \cos(\varphi_3)z^{-2}) \times (1 - 2\cos(\varphi_2)z^{-1} + \cos(\varphi_4)z^{-2}) \quad (4\text{-}12)$$

Where φ_1, φ_2 are responsible for the desired position of zeroes on the unit circle and φ_3, φ_4 are responsible for holding the zeroes on the unit circle and changing their position on the complex plane (between real axis and imaginary axis) which in-turn shapes the quantization null.

From (4-12), we can understand that, φ_1 and φ_2 provide two complex conjugate zeroes each on the unit circle according to the frequency notch calculated in the previous section. As we always keep a zero at the 'zero' position so $\varphi_1 = 0$. The frequency notches x_1 and x_2 calculated from the previous section directly taken as the value of φ_2. The value of φ_3 and φ_4 is always kept as '0' except for a special case where $\varphi_3 = \pi$ and the four zeroes are moved around the unit circle every $\frac{\pi}{2}$ distance.

The special case occurs when the desired notch positions are $0, \frac{\pi}{2}$, and π, i.e. the zeroes are $\frac{\pi}{2}$ distance apart and symmetric. In such a case φ_1 and φ_2 are kept the same value as, $\varphi_1 = \varphi_2 = \frac{\pi}{2}$ and $\varphi_3 = \pi$. In such a case the first segment of (4-12) gives the two notch positions of 0 and π.

From (4-12), it can be observed that the proposed NTF is a modular design, which means the order of the NTF can be easily increased by adding another modular segment of $(1 - 2\cos(\varphi_a)z^{-1} + z^{-2})$. However, the minimum number of modules can't be less than two. Every addition of the module increases the order of the system by two and provides a notch (two

zeroes) at position φ_a of the normalized frequency. The φ_a can also be programmed for desired position accordingly.

The denominator of the transfer function is always 1 which means that all the poles of the system are at the center of the unit circle which ensures the stability of the system.

In this research work, the two signals with carrier frequencies f_1 and f_2 considered are 800 MHz and 2 GHz. From (4-4) the desired notch position is calculated as $x_1 = 0.5\pi$ and the other required notch positions are 0 and π. From these values the first transfer function can be calculated as,

$$H_1(z) = (1 - z^{-4}) \tag{4-13}$$

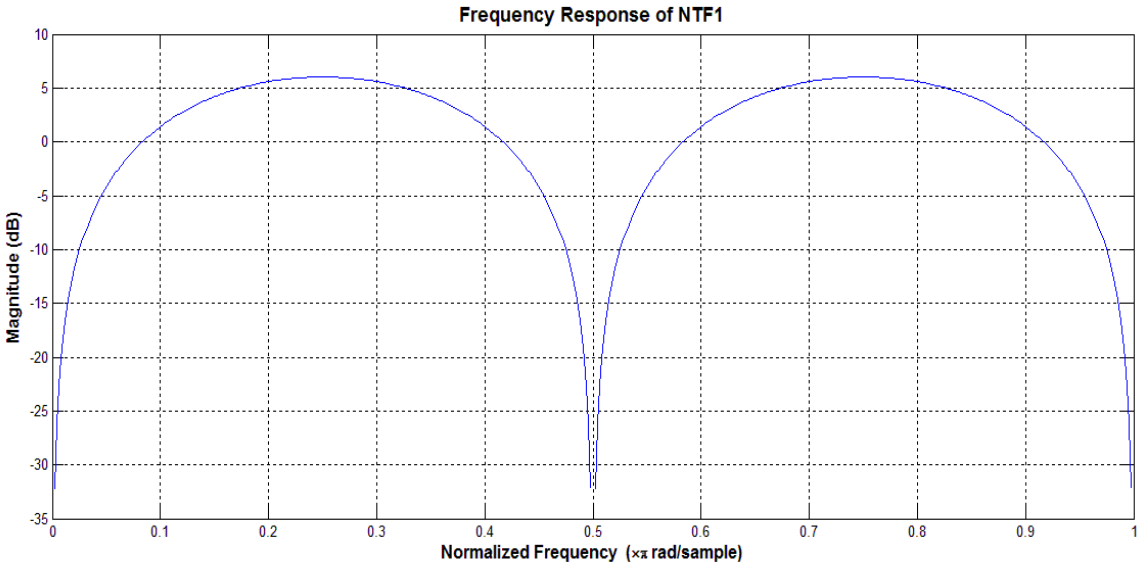
Where, $\varphi_1 = \varphi_2 = \frac{\pi}{2}, \varphi_3 = \pi$, and $\varphi_4 = 0$ are considered.

From (4-1) the desired notch position is calculated as $x_2 = 0.8\pi$ and the first notch position is at '0'. By equating these values in (4-12) the second transfer function can be calculated as,

$$H_2(z) = (1 - 2z^{-1} + z^{-2}) \times (1 - 2\cos(4\pi/5)z^{-1} + z^{-2}) \tag{4-14}$$

Where, $\varphi_1 = 0, \varphi_2 = 4\pi/5$, and $\varphi_3 = \varphi_4 = 0$ are considered.

Figure 4-5 and 4-6 depict the frequency response and pole-zero plots of the two noise transfer functions (NTFs) derived above.



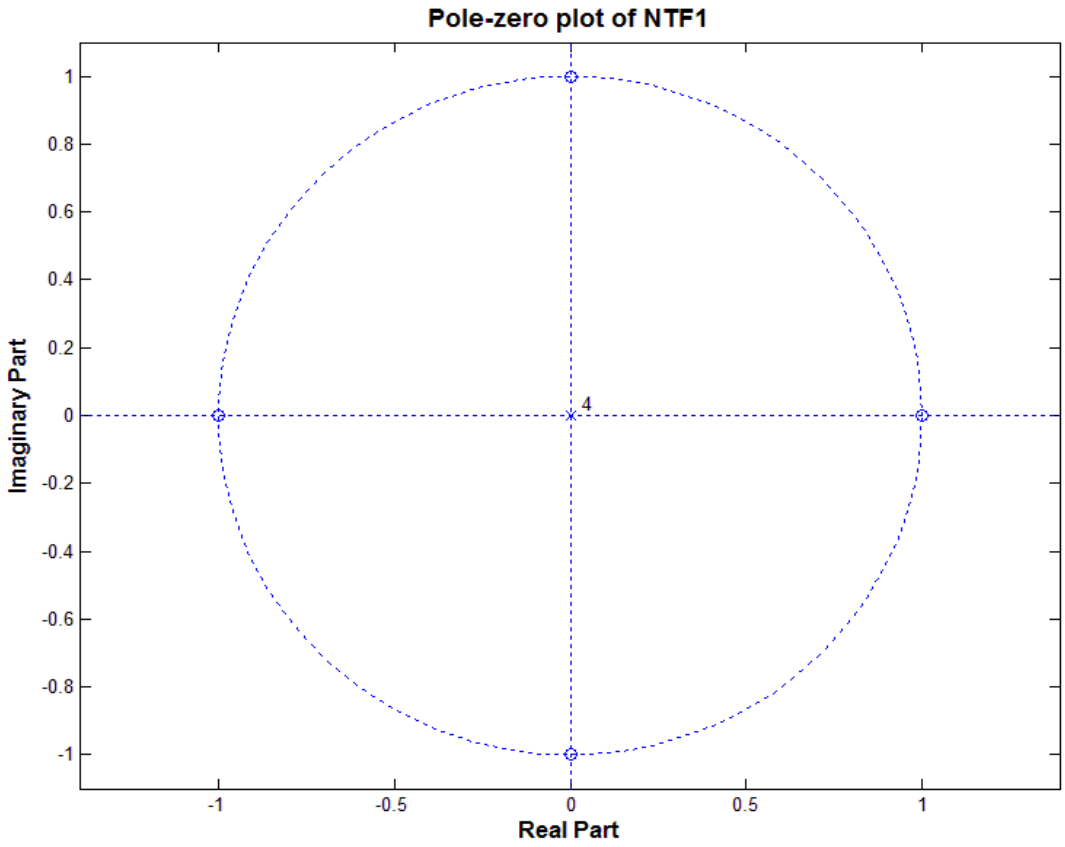
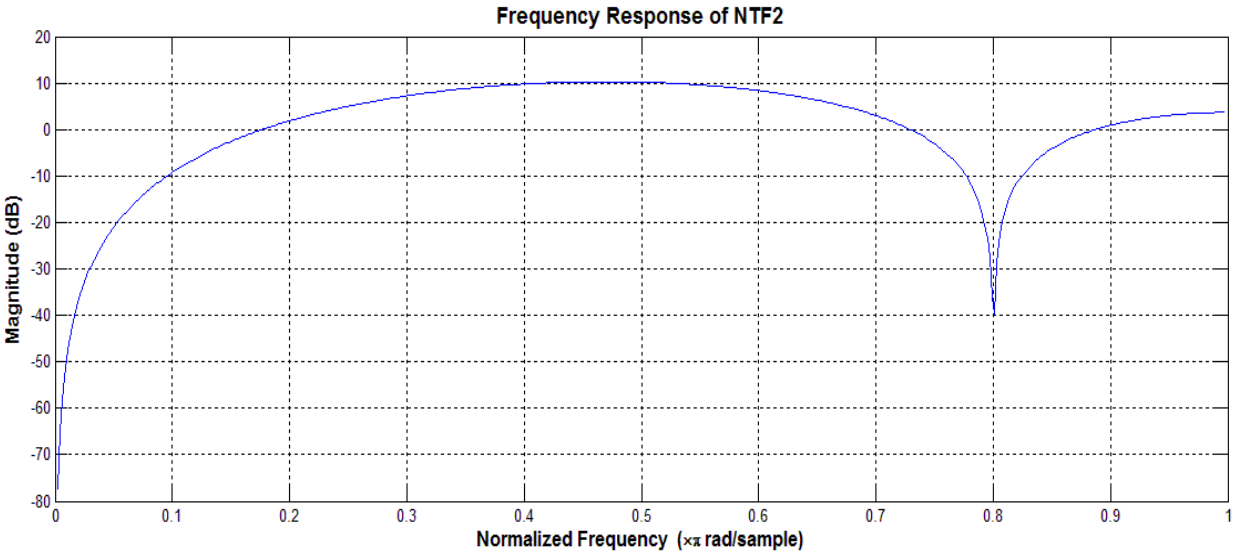


Figure 4-5. (a) Frequency response, and (b) Pole-zero plot of the first noise transfer function from (4-13).



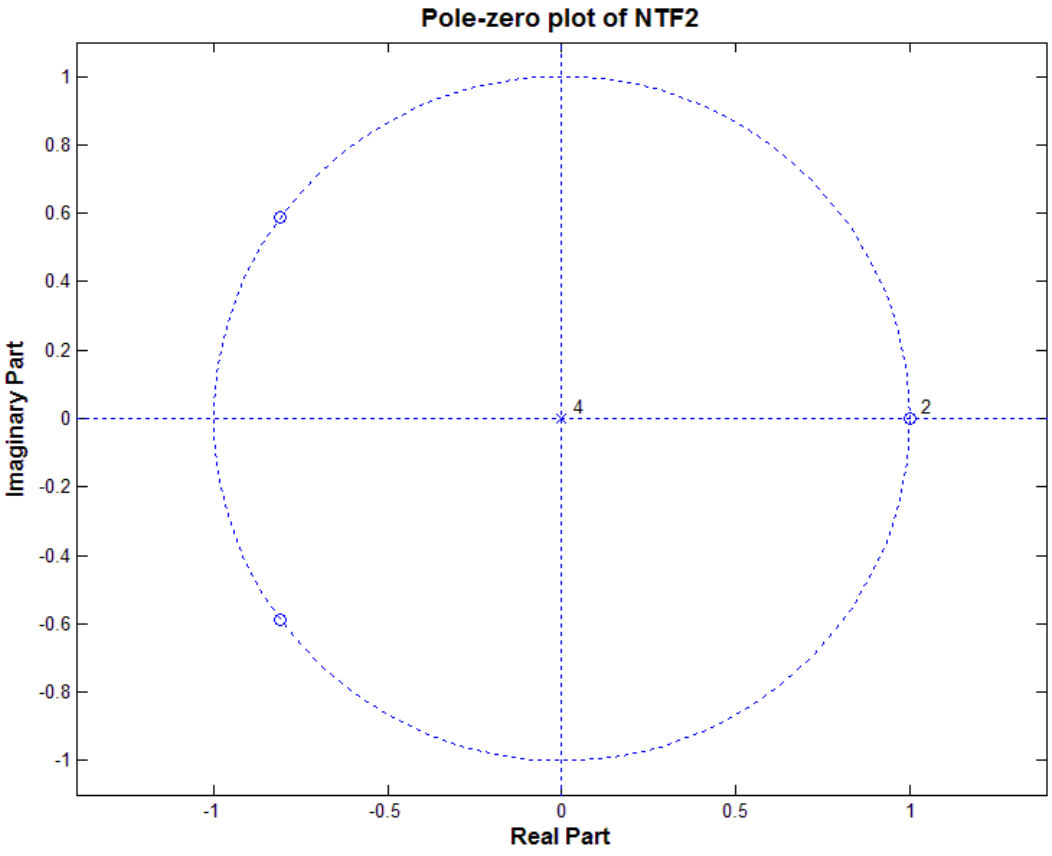


Figure 4-6. (a) Frequency response, and (b) Pole-zero plot of the first noise transfer function from (4-13).

4.4 Digital Up-conversion

Digital up-conversion is employed for up-converting the digital baseband signal to RF frequency. A single 4×1 multiplexer is used for the IQ modulation and up-conversion process [3][26][61]. The multiplexer's clock is 4 times the higher frequency of the signals and hence the highest clock in the system. Multiplexer's clock is responsible for the carrier frequency of the signals. The input of the multiplexer is formed by taking I , Q , $-I$, $-Q$. The operation is similar to multiplying the sequences [1, 0, -1, 0] and [0, 1, 0, -1] for I and Q signals respectively and adding together to generate the sequences $[I_1, Q_1, -I_1, -Q_1]$ and $[I_2, Q_2, -I_2, -Q_2]$. Figure 4-7 shows the up-converter and it's operation.

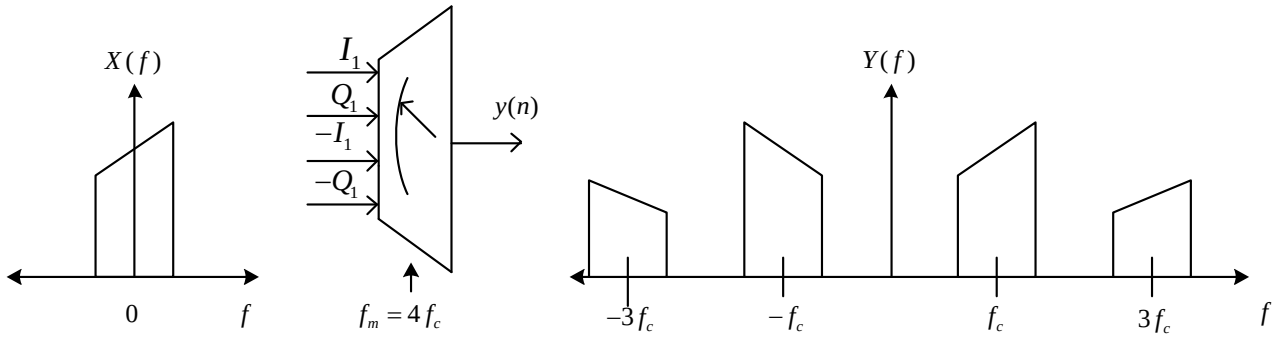


Figure 4-7. 4×1 **Multiplexer as digital up-converter [3].**

The up-converter replicates the output of the delta-sigma modulator in the same manner as shown above. The position of the signal and notches gets translated into the desired positions in the spectrum as calculated above. The input and expected output of the up-converter for the two signals mentioned above is shown in Figure 4-8. The outputs are held five times and two times respectively like sample and hold operation to achieve same sampling rate. The signals are then fed to two SMPA for the two signals respectively for amplification.

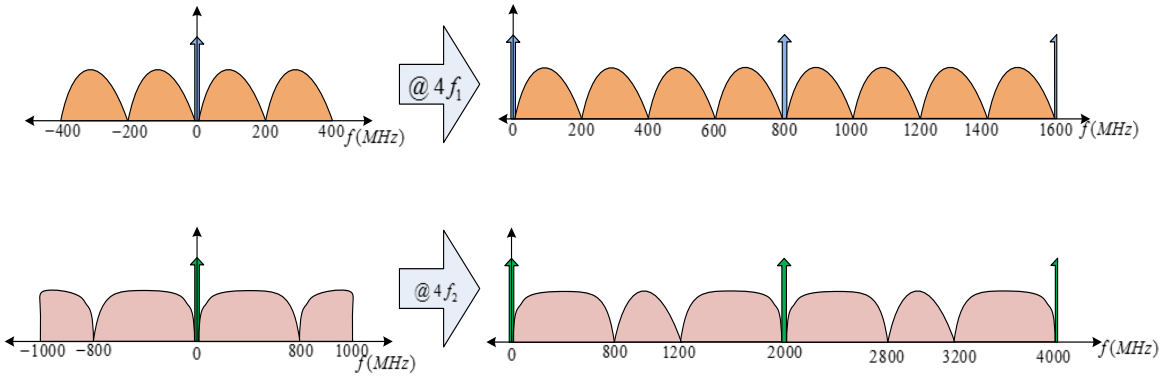
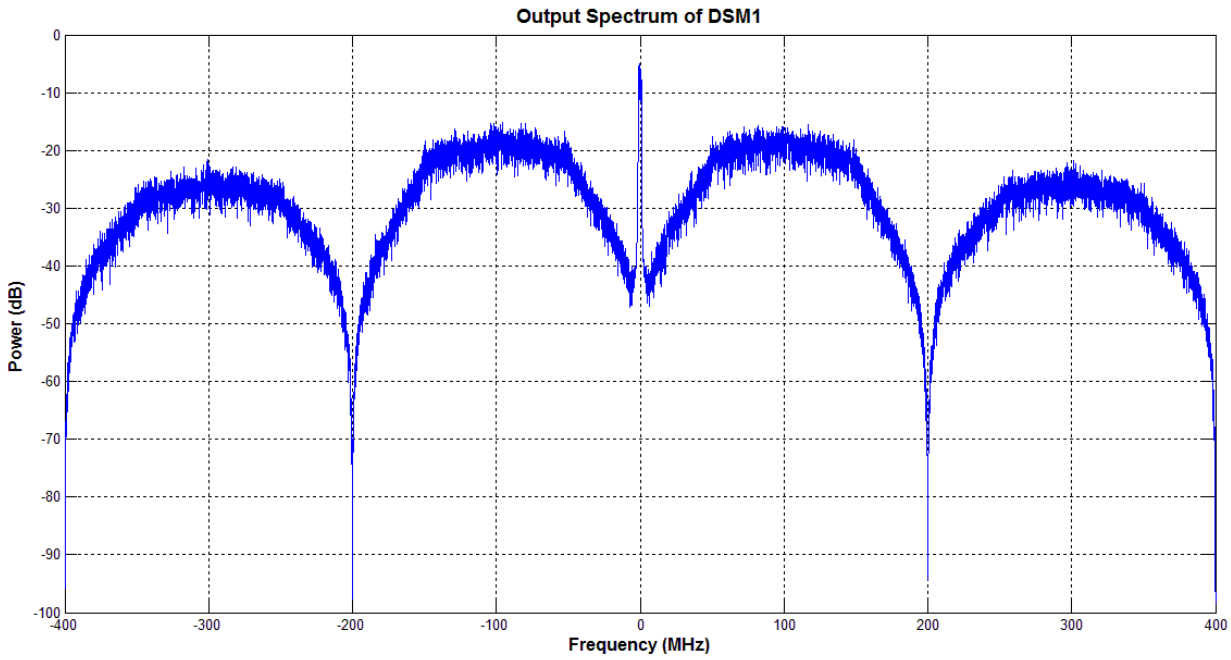


Figure 4-8. Input and output of digital up-converter for 800 MHz and 2 GHz signals.

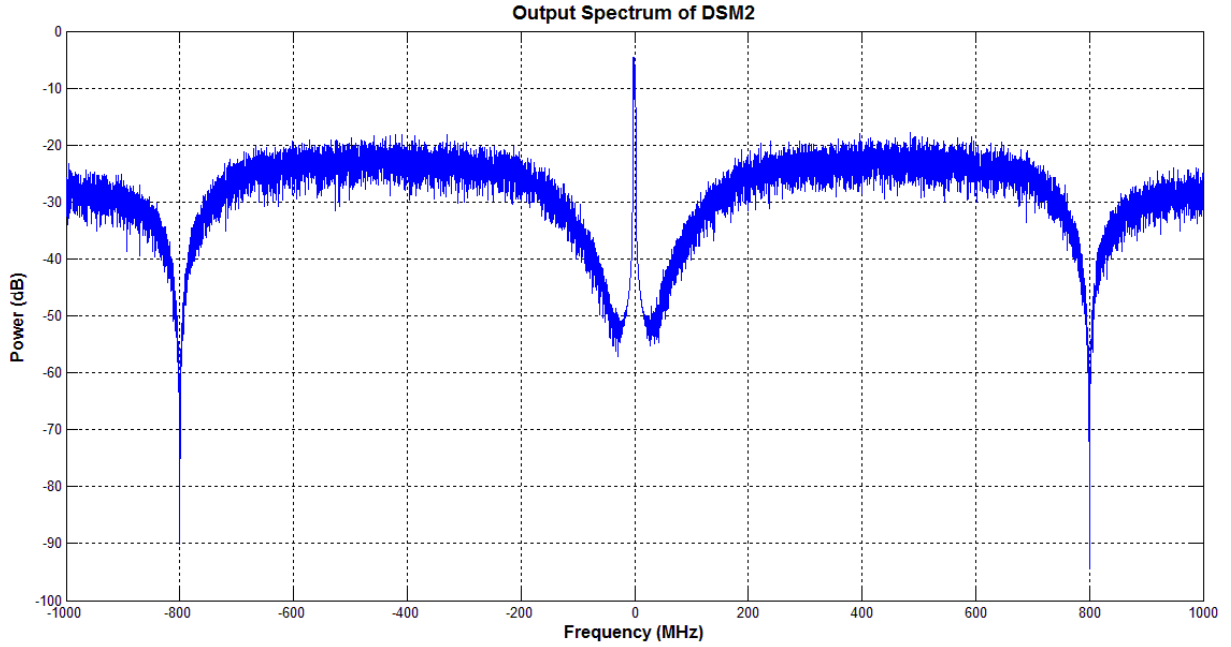
4.5 Simulation Results

In this section the simulation results are presented as a proof of the concept discussed above. In this simulation two baseband LTE signals with bandwidths 5MHz and 10MHz are considered. The carrier frequencies of the interest f_1 and f_2 are considered as 800 MHz and 2 GHz respectively. The baseband signals were oversampled 160 and 200 times respectively to achieve the carrier frequency baseband signals. Therefore the signals were sampled at their respective carrier frequencies.

The signals are then fed to the delta-sigma modulators designed above. The pass-bands of the first DSM for the 800 MHz signal were 0 Hz, 200MHz and 400MHz. Whereas, the pass bands of the second DSM for the 2 GHz signal were 0 Hz and 800 MHz. Figure 4-9 (a) and (b) shows the output of the DSMs respectively.



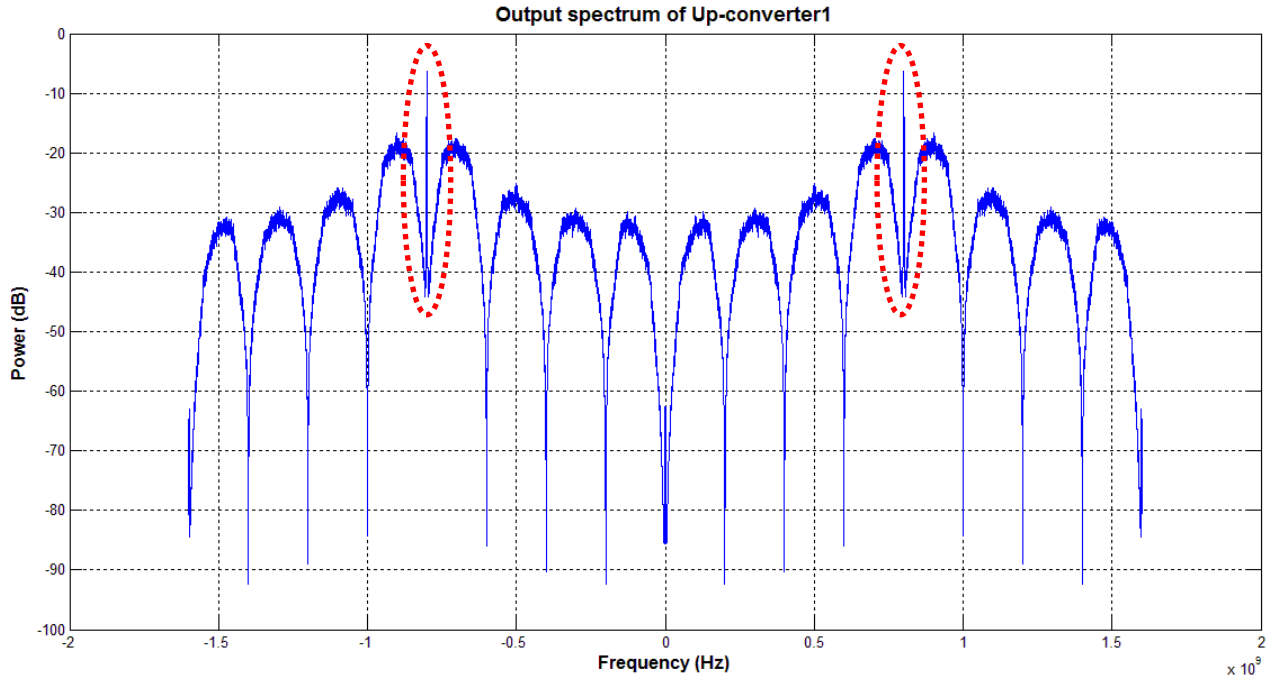
(a) Output spectrum of DSM1



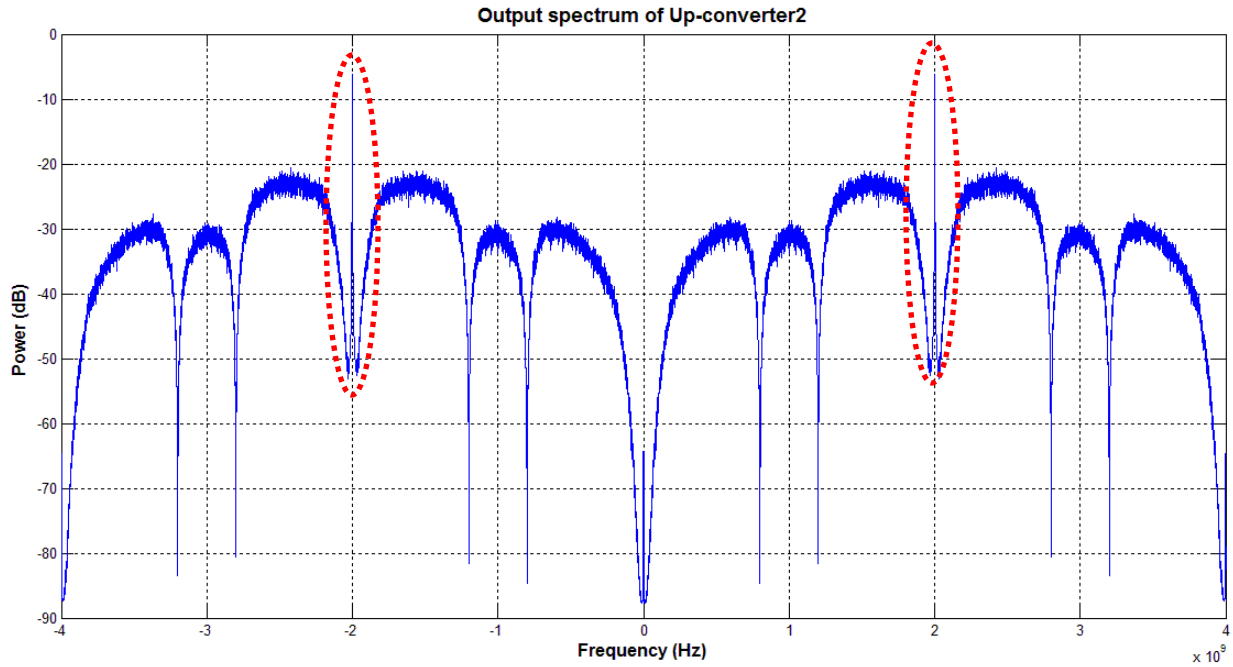
(b)Output spectrum of DSM2

Figure 4-9. The outputs of the (a) First DSM with 800MHz carrier frequency baseband signal, and (b) Second DSM with 2GHz carrier frequency baseband signal.

The clocks of the DSMs are taken as f_1 and f_2 respectively. The outputs of the DSMs are then fed through two digital up-converters. The output frequencies of the up-converters are 3.2 GHz and 8 GHz respectively. During the up-conversion process the baseband signals are translated to 800 MHz and 2 GHz signal. The frequency notch generated at 400 MHz of the first signal gets translated to 1.2 GHz at the first stage before it is held to achieve the same sampling frequency. The frequency notch at 800 MHz is found at the first Nyquist zone of the second signal, which also generates another frequency notch at 1.2 GHz in the second Nyquist zone and so on. Figure 4-10 shows the outputs of the digital up-converter. Both of the signals are then held five times and two times respectively to achieve the same sampling frequency to add together. In this process the frequency notch at 2 GHz can be seen at the spectrum of the first signal. The final clock frequency of the system becomes 16 GHz. Figure 4-11 shows the frequency spectrum of the two signals added together before filtering.



(a) Output spectrum of up-converter 1



(b)Output spectrum of up-converter2

Figure 4-10. Output spectrum of (a) First up-converter with 800MHz signal, (b) Second up-converter with 2GHz Signal.

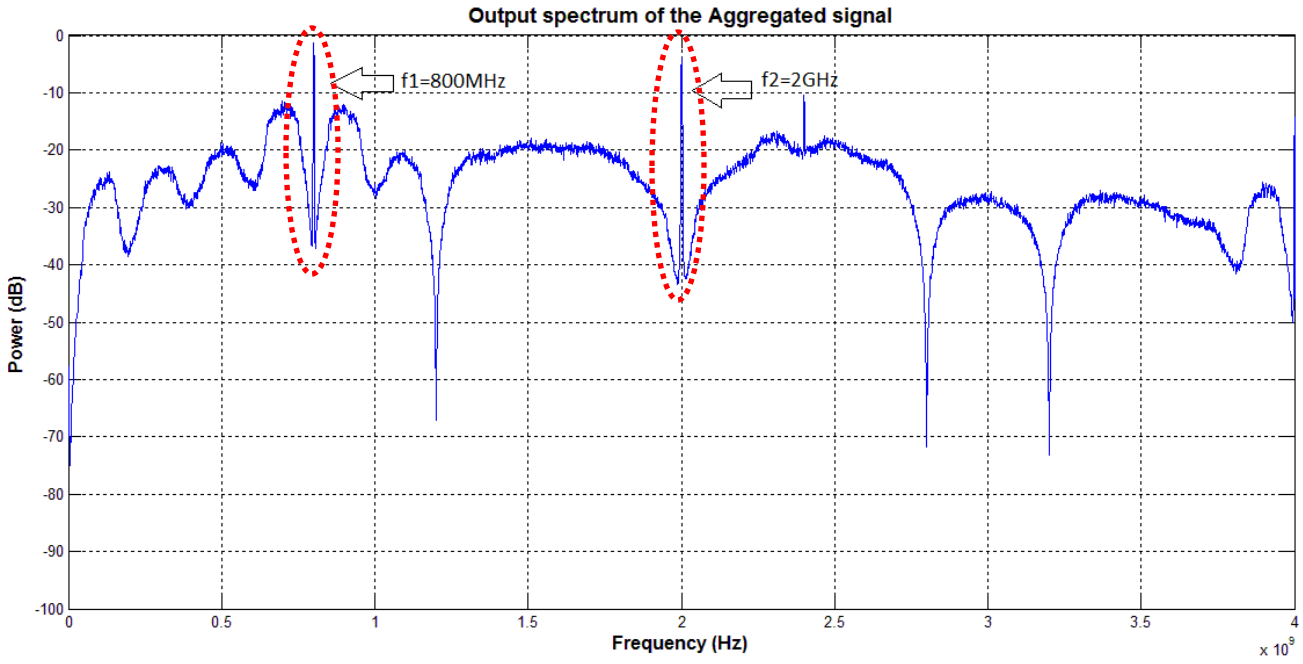


Figure 4-11. Frequency spectrum of the signals added together.

The peak-to-average-power ratio (PAPR) of the input and output signal is then calculated by,

$$PAPR = P_{Max} - P_{Mean} \tag{4-15}$$

PAPR of a signal decides how much power back-off is needed for the SMPA to operate. So less PAPR means less power back-off and more efficiency. The PAPR of the output signal is found to be 6.01 dB whereas that of the input signal is 7.78 dB. PAPR shows a little bit improvement, however the research on effective combining and amplifying is left as future work.

4.6 Conclusion

In this chapter an extensive analysis of designing a new low complexity delta-sigma modulator architecture for concurrent dual band transmitted is presented. With the technique presented non-contiguous bands of RF signal can be transmitter concurrently for spectrum aggregation application. The proposed methodology was validated through simulation with modern communication standard LTE signals.

A step by step design procedure for dual band-pass delta-sigma modulator was discussed. The design considerations were also laid carefully. Two LTE signals of carrier frequencies 800 MHz and 2 GHz were considered for the validation of the concept.

The design for effective methods of combining of the signal and amplification is left as future work.

Chapter Five: Conclusion

5.1 Summary

The growth of the wireless connectivity and convergence of different wireless technologies demands stringent requirements on ADC and DAC with reduced power and cost in wideband applications. Delta-Sigma modulators have demonstrated promising performance for high resolution but narrow bandwidth applications. Parallelism techniques for delta-sigma modulator opened a whole new range of ADCs and DACs. Three major parallel architectures namely time interleaved delta-sigma modulator (TIDSM), Hadamard modulated delta-sigma modulator (Π -DSM) and Quadrature mirror filter bank frequency band decomposition (QMF FBD) based ADC has been reviewed. Though TIDSM is a very popular architecture, it is prone to jitter noise and channel mismatch which needs to be compensated in the digital domain. Among these three techniques, FBD is insensitive of channel mismatch and jitter noise, hence this architecture is a natural choice for ADC.

In this thesis, a new low complexity wideband parallel ADC architecture has been proposed which increases the conversion bandwidth while maintains an acceptable medium to high resolution. The proposed approach addresses the complexity issues in the conventional QMF FBD analog-to-digital converters by employing a segmented frequency down conversion of the input signal and low-pass delta-sigma modulators (LPDSMs) for each channel resulting a less complex architecture.

In chapter three, the proposed low complexity frequency band decomposition based delta-sigma modulator was introduced and analyzed. The model presented consists of four channels parallel architecture, where a wideband input signal is fed to all the parallel channels simultaneously. Each channel frequency down-converted and processed small segments of the

input signal and at the end all the segments were shifted back and added together to get the original signal, which resulted in overall wideband signal handling capacity. A modern communication standard LTE signal was considered the simulation and implementation. The proposed model was implemented on FPGA through Xilinx System Generator and MATLAB Simulink for proof of concept. A step-by-step analysis of FPGA implementation was also presented. An extensive analysis of Fixed point implementation and resource optimization was also demonstrated. It was shown that the proposed architecture reduced the number of resource occupied by 70% on average than that of the conventional QMF FBD while maintaining a good SNDR of around 46 dB.

To support the wide bandwidth transmission requirements for next generation mobile communication systems like LTE-Advanced, a concurrent dual band delta-sigma modulator architecture for spectrum aggregation transmitter was proposed in this thesis. The architecture is based on dual band-pass delta-sigma modulator where the noise is shaped to fit in two frequency bands in a single spectrum without degrading the signals with out-of-band noise.

In chapter four, the proposed concurrent dual band delta-sigma modulator architecture for spectrum aggregation transmitter application was introduced and discussed. The transmitter architecture for the proposed DSM model was modified from single band to dual band for concurrent transmission application. An extensive analysis of the design of the DSM architecture was presented. A detailed method of frequency planning for shaping the quantization noise was discussed. The model shapes the quantization noise in such a way that the second frequency can fit at the quantization null of the first frequency and vice versa. Digital up-conversion technique and its effects has been discussed in detail. Simulation results with two LTE signals of carrier

frequency 800MHz and 2GHz was presented as a proof of concept. PAPR of the input and output signal was calculated and found some improvement for the proposed model.

5.2 Future Work

In this research, two different architectures were discussed for addressing various ADC and DAC issues in wideband receiver and transmitter systems. The proposed low complexity FBD can be a promising solution for receiver application. However, the utilization of low-pass filter in each channel changes the constant envelop signal and therefore the signal becomes unusable for driving SMPA for transmitter application. Extending the FBD architecture for transmitter application is left as future work for this project.

For concurrent dual band delta-sigma modulated signals, signal combining is a critical issue. Employing separate PAs for two channels before signal combining has been proposed as a temporary solution. In this case the signal combining happens in the analog part. However as adding the signals together in the digital domain changes the constant envelop of the signal and the signal don't remain bi-level any more. This makes difficult to employ the signals to drive the SMPA anymore. Therefore, designing an effective signal combiner and PA for this application is left as future work of this project.

5.2.1 Extending the FBD Technique for Transmitter Application

Harris et al. discussed about polyphase channelizer frequency division multiplexer based N-channel transmitter architecture in [56]. From the equivalency theorem we can understand that the operation of frequency down conversion and low-pass filtering can be treated same as the channelizer. Time interleaved technique in TIDSM architecture performs as a Time Division

Multiplexed (TDM) system. The output of the TIDSM can be directly fed to an SMPA as driving signal.

One idea to extend the proposed FBD model discussed in chapter three for transmitter application, an idea could be to feed the output of the low-pass filter to the TIDSM architecture to convert the signal into bi-level signal. This architecture is inspired from the same principle discussed in [56]. Output of each channel of FBD will be fed to TIDSM with a delay. A considerable improvement in SNDR along with the usability of the signal for transmitter system is expected with this technique

5.2.2 Design for Signal Combiner and SMPA for Concurrent Dual Band Transmitter

Kitayabu et al. presented a combiner and switching amplifier model in [54] which incorporates multi-level signals. After adding the signals together in the digital domain, the combined signal becomes a multi-level signal, which cannot be employed directly to the switching amplifier. The method proposes the utilization of a number of SMPAs i.e. one PA for each level of the signal. In this method the number of PAs becomes 9.

Paul Colantonio et al. proposed a harmonically tuned PA for concurrent dual band application in [57], where multi-frequency passive matching network facilitates the concurrent operability. In the proposed method an impedance buffer element is introduced to achieve a short or open circuit condition at the selected reference section of the matching network so that any impedance after the reference section towards the load gets ineffective.

Renato Negra et al. presented class-F load coupling network for concurrent dual band application in [58] where impedance conditions are synthesized up to three harmonics with no electronically tuneable elements. The PA shows reasonable performance in terms of drain efficiency for 1.7GHz and 2.14GHz frequency.

A digital logic circuit which will govern the signals combining without losing the bi-level signal for driving the SMPA could be developed as a solution to mitigate the number of SMPAs employed.

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