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Concurrent Dual Band Six Port Receiver

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Concurrent Dual Band Six Port Receiver

by

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Abstract

Receiver front-ends have always been a critical component in wireless communication system design. Its performance and characteristics determines the quality and fidelity of the communication systems. Proliferation of communication protocols and standards however, require that the front-ends should become more flexible, multi-standard and reconfigurable. In addition, to enable higher communication throughput, there have been proponents of concurrent dual-band receiver front-ends to receive signals in more than one band simultaneously. Typical architecture for this concurrent multiband operation uses the front-end stack-up technique, which builds parallel receiver paths with each path dedicated to one frequency band. This increases complexity, power requirement, size and cost. The Six-Port receiver (SPR) is a low power and low complexity alternative to conventional homodyne receiver, which is multi-standard, flexible and easily reconfigurable. This thesis proposes the use of the SPR for a concurrent dual-band operation without any component duplication in the frequency down-conversion path.

Acknowledgements

All thanks and praises is due to almighty Allah; the creator, sustainer and lord of the worlds. May his peace and blessings be upon the holy prophet Mohammed (SAW).

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Last but not least, I would like to thank my parents, my brother and sister for their support and encouragement, God knows I really needed it.

To my parentsé

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List of Symbols, Abbreviations and Nomenclature

Symbol	Definition
3G	Third Generation
4G	Fourth Generation
ADC	Analog To Digital Converter
AGC	Automatic Gain Control
AWGN	Additive White Gaussian Noise
BB	Baseband
BER	Bit Error Rate
BPF	Band Pass Filter
BS	Base Station
BW	Bandwidth
DAC	digital to analog converter
DB	Dual band
DBA	Dual-band Antenna
DC	Direct Current
DCR	Direct Conversion Receivers
DL	Downlink
DSP	Digital Signal Processing
EVM	Error vector Magnitude
FDD	Frequency Division Duplex
FE	Front-end
GPS	Global Positioning System

IC	Integrated Circuit
IF	Intermediate Frequency
IMD2	Second Order Intermodulation
I/Q	In-phase/Quadrature
LAN	Local Area Networks
LIF	Low IF receiver
LNA	Low Noise Amplifier
LO	Local Oscillator
LTE	Long Term Evolution
PAN	Personal Area Networks
PAPR	Peak to Average Power
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RFID	Radio Frequency Identification
Rx	Receiver
SDR	Software Defined Radio
SHR	Superheterodyne Receiver
SNR	Signal to Noise Ratio
SPR	Six Port Receiver
Tx	Transmitter
UE	User Equipment
VSA	Vector Signal Analyzer
WCDMA	Wideband Code Division Multiple Access

Chapter One: **Introduction**

In today's wireless communication systems, there are numerous communication standards with different protocols having different front-end transceiver requirements. Nonetheless, these standards are rapidly evolving to enable higher data rates, fidelity, power efficiency, network security and availability. A direct implication of this is a frequent upgrade or complete change of the supporting hardware and software requirement for the communication system when migrating to a new standard. The cost, manpower, operation downtime and other resource needed for this frequent change will not be justifiable at such high turnover. A second consideration will be for communication systems that transmit and receive concurrently in different bands using similar or different communication standards. This could be to support two or multiple communication services at the same time or in spectrum aggregation application. This has led the research community to look into transceiver solutions that will be generic and thus adaptable for different communication standards and protocols without a complete change in the hardware requirement. Going further, such solution should also be functional for concurrent multiband operation without duplicating the hardware requirements. Software Defined Radio (SDR) architecture by virtue of its flexibility and reconfigurabilty will be the ideal solution to these requirements. The wireless innovation forum (formerly SDR forum) defines the SDR as a radio in which some or the entire physical layer functions are software defined [1]. It is essentially a hardware platform consisting of DSPs and general purpose microprocessors on which software modules run to implement radio functions such as; generation of transmitted signal (modulation) at transmitter; tuning and detection of radio signal (demodulation) at the receiver. The software running on this generic hardware platform is

modifiable and reconfigurable to suit multiple standards at any frequency over which the radio was designed [2]. Fig 1.1 shows an ideal SDR receiver and transmitter.

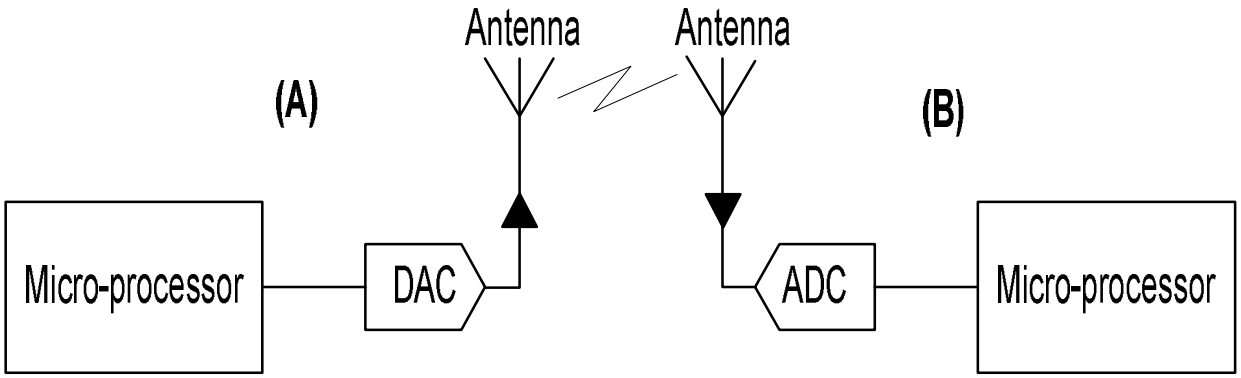


Figure 1.1 SDR transmitter and receiver

As shown in fig 1.1, the user data is mapped to the desired waveform in the microprocessor. The digital samples are then converted directly into an RF signal, converted to an analog signal with the digital to analog converter (DAC) and sent to the antenna. The transmitted signal enters the receiver at the antenna, is sampled and digitized by the analog to digital converter (ADC), and finally is processed in real time by a general purpose processor [1]. To implement the receiver subsystem as depicted in fig 1.1, the sampling rate of the input Analog-to-Digital converter will be at least twice the received radio frequency (RF) and the processor used must be fast enough to process the digitized signal in real time. To implement the transmitter, the digital to analog converter must also have a sampling rate of at least twice the RF frequency [3]. An ideal SDR refers to both transmitter and receiver component. However, the focus of this thesis is on concurrent reconfigurable receiver architectures for communication systems. Hence, further analysis will be specific to SDR receivers. The ideal SDR receiver is an elegant solution. However, there are challenges with its direct implementation. Most antennas are mechanical

structures and are difficult to tune dynamically, this will limit the bandwidth of operation of the SDR. Secondly, by Nyquistôs theorem, the ADC sampling must be at least twice the highest frequency of the band over which the antenna captures electromagnetic waves. Such frequencies will be in tens of gigahertz. This sampling frequency is not achievable with the current state of the art technology. Also, the ADC digitizes the entire signal within the reception range of the antenna. Typical interferers have a much higher power level than the desired signal, thereby placing a heavy requirement on the number of bits (dynamic range) of the ADC. Lastly, to ensure a real time operation of the receiver, the required speed of operation for the DSP to accommodate the very high sampling rate of the ADC is also not achievable with the current technological state [2]. For these reasons, modern implementations of software defined radio involves an initial band pass filtering followed by a frequency down conversion to a lower intermediate frequency (IF) before digitizing the signal. Down-converting the RF signal to a much lower frequency enable easier and more efficient digitization and processing of the signal. The most common method of frequency down conversion is mixer based, which involves mixing the RF signal with a local oscillator (LO) signal with a mixer [4]. Sub-sampling is another method used for this frequency down-conversion. The six port receiver (SPR) is another architecture that does frequency down-conversion using the combination of a six port wave correlator circuit and four envelope detectors. Down-conversion eases the requirement on the ADC and other components of the SDR. After downconversion, the channel selection filter removes or reduces the interferers. This reduces the dynamic range requirement and power requirement on the ADC. The much lower IF frequency also reduces the sampling frequency requirement on the ADC. Fig 1.2 depicts a realizable implementation of a SDR receiver.

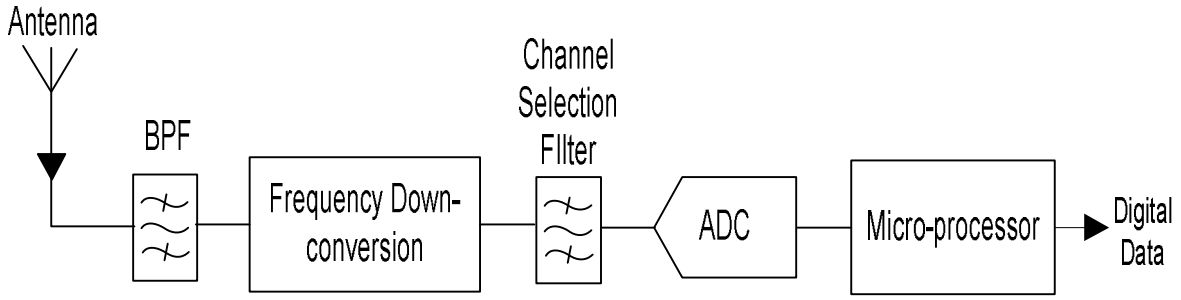


Figure 1.2 Realizable implementation of a SDR receiver.

The frequency down conversion block can be implemented in number of ways and combinations as earlier noted. Modern receiver architectures can be broadly divided into three main topologies; the superheterodyne receiver (SHR), low IF receiver (LIF) and the direct conversion receiver (zero-IF, homodyne receiver). The six port receiver (SPR) is one type of direct conversion receiver. This thesis explores the use of a SPR in real communication systems and its implementation for concurrent dual-band applications. The following section describes different modern receiver architectures, describing their structure and discussing their advantages and drawbacks.

1.1 Modern Receiver Architectures

The several communication standards with varying bands of operation in today's wireless environment impose the conditions of being multimode and multiband with a high degree of flexibility on the receiver front-ends (FE). Multimode property is mainly affected by the digital baseband (bb) processing while the multiband property is largely dependent on receiver components such as mixers, amplifiers, filter, diplexers, combiners etc. [5]. As such, modern receiver architectures are designed towards meeting these requirements.

1.1.1 Superheterodyne Receiver (SHR)

The SHR has the strongest commercial presence of all receiver architectures. It uses two or more stages of frequency down-conversion to convert the RF frequency signal to baseband going through one or more IF frequency stages. It is used for most high-end receivers. The filters used after each frequency conversion stage reduces the LO leakage and the amplitude of undesired signals such as the image frequency and potential interfering signals which can otherwise lead to intermodulation product which degrades the signal quality. The interference, leakages and intermodulation products are typical challenges in direct conversion receivers as will be discussed in a following section [4]-[6]. Fig. 1.3 shows a block diagram of the SHR.

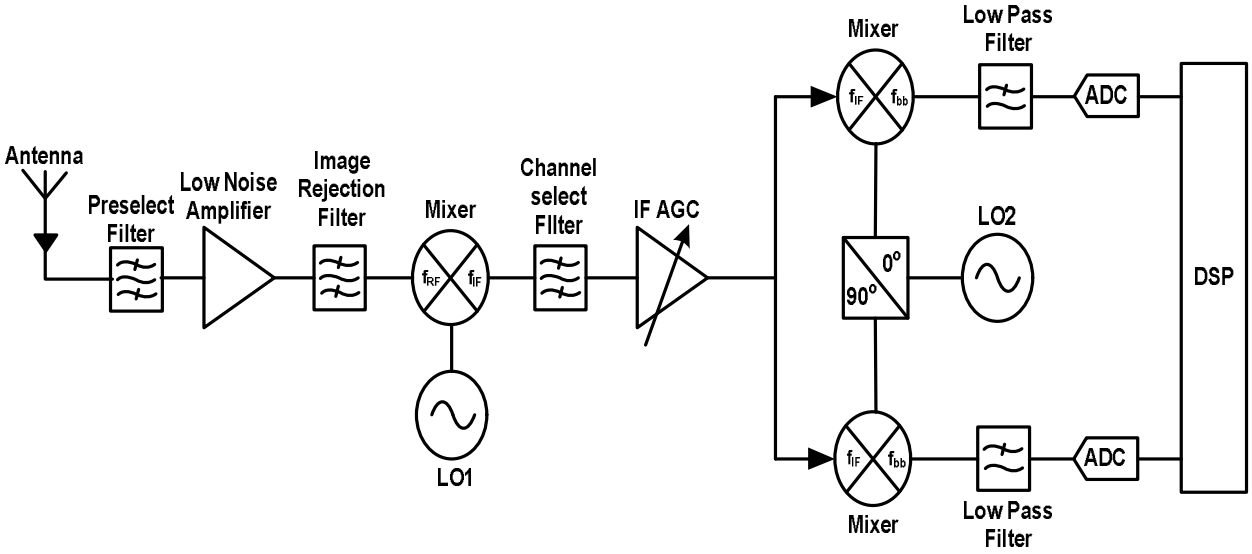


Figure 1.3 Superheterodyne Receiver

Referencing the two-stage down-conversion architecture of fig 1.3, there is a preselect filter for band selection, a low noise amplifier (LNA) to improve sensitivity, an image rejection filter at the RF stage. At the IF stage, there is a channel selection filter, typically a surface acoustic wave (SAW) filter, which is usually bulky and off-chip and an automatic gain control (AGC)

amplifier. At baseband, there is a low pass filter to further improve selectivity. However, this web of filters and amplifiers increases the complexity, size and power requirement of the receiver. The bulky off-chip IF channel selection filter limits it suitability for integration. Also, the IF filters and amplifiers are frequency restrictive with defined channel bandwidth peculiar with the signal standard and are mostly not tunable. To use the SHR in SDR applications will mean having a large bank of fixed filters to cover the broad range of possible channel bandwidths encountered in the SDR application. This is not a very practical solution.

1.1.2 Direct Conversion Receivers (DCR)

The DCR is also known as Homodyne or Zero IF Receiver. In itsô most basic structure works by directly converting the received RF signal to baseband without any intermediate frequency (IF) stage. In this architecture, the LO frequency is set to the signal RF centre frequency and its phase is locked to the signal carrier phase. Eliminating the IF stage and the image rejection filter reduces the complexity, power requirement and size of the receiver. The small size improves its on-chip integration and hence will be a natural solution to SDR applications. It however has certain drawbacks which affects it performance. Typical challenges include second order intermodulations (IMD2), dc offsets, quadrature imbalance and in-band local oscillator (LO) leakage and radiation that are not present when using the superheterodyne architecture. Additionally, the lack of an IF stage may result in an increase of the low frequency flicker noise appearing at the centre of the band (1/f noise). As a result, physical implementations of direct conversion receivers have repeatedly proven to be a compromise between performance and the level of on-chip integration [5]-[7]. Fig 1.4 show a typical DCR.

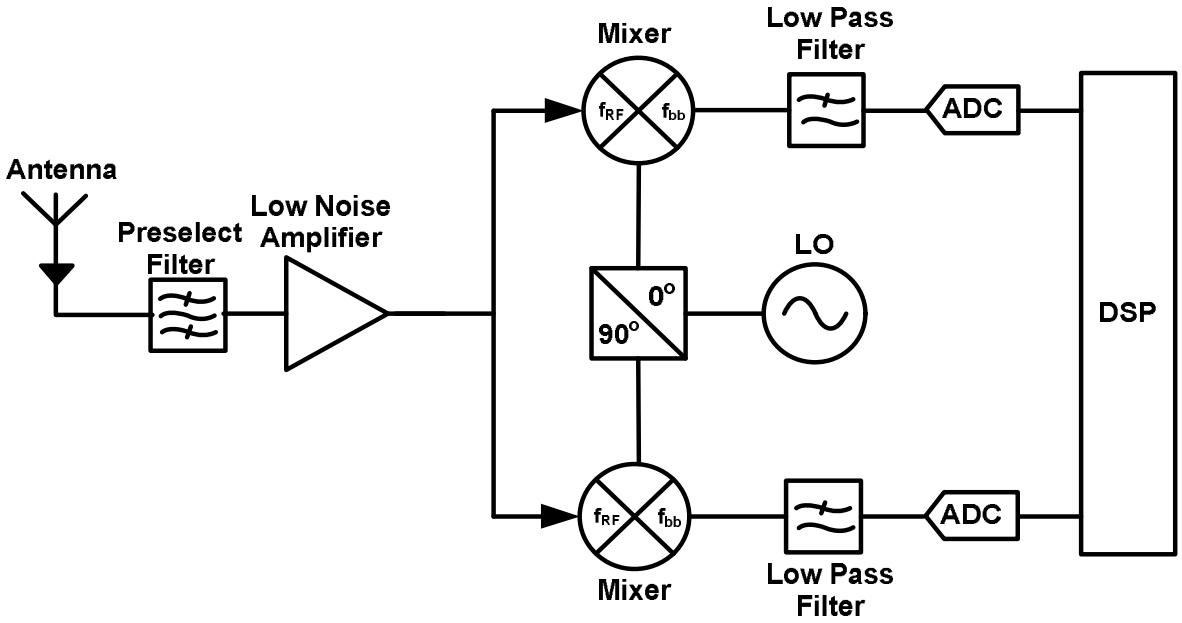


Figure 1.4 Direct Conversion Receivers

Much work has been done in seeking ways to mitigate these drawbacks [6]-[9]. A common technique is the use of a DC notch to remove the DC offset at baseband near zero. While this is not critical in broadband signals, for narrowband communication systems such as in voice communication, the notched DC component of the signal is a high proportion of the whole signal thereby causing intense impairment of the received signal. Advancement in research has however solved some of these limitations. C. Andrews and A. Molnar [10] reported a mixer-first, LNA-less architecture. This architecture leverages on the passive mixersô transparency (translating impedance from one side to the other) to translate a low-pass filter on the baseband to a band-pass filter on the RF port to achieve good selectivity, and noise figure. D. Murphy et al. [11] presented a noise cancelling wide-band receiver that employs two separate passive mixer-based down-conversion paths to improve noise performance. This architecture also uses the passive mixersô transparency to achieve RF band-pass filtering to remove out-of-band blockers.

However, none of these works investigates the design of concurrent dual-band receiver. It would be interesting to study how matching using impedance translation will be done in the case of a concurrent multi-band application.

1.1.3 Low-IF Receivers (LIF)

The LIF receiver combines the advantages of both the SHR and the DCR approaches. It uses a low IF frequency instead of Zero-IF to cope with the drawbacks of the DCR while preserving a structure that does not require IF SAW filters. By using a low IF frequency which ranges between half to two times the channel bandwidth, the DC offset problem peculiar with the DCR is alleviated. Secondly, it is more feasible to sample the low IF signal after the first mixer stage with a high resolution analog-to-digital convertor (ADC). In this architecture, the image band is quite close to the desired band at RF, thus, filtering it is quite challenging. The image problem is solved using a complex band-pass filter usually referred to as complex polyphase filter. After frequency down-conversion, the desired signal and the image fall in the same frequency band. However, the phase relation between the Inphase (I) and quadrature (Q) signals is different for the wanted signal (+90°) and the image signal (-90°), which could make the discrimination between the wanted signal and the image signal. An I/Q signal with +90° phase relation is said to have positive frequency components while that with -90° phase relation is said to have negative frequency components. Unlike real filters, the polyphase filter is able to distinguish between positive and negative frequency components thus rejecting the image signal [12].

The IF signal is digitized and the remaining receiver operation is done in the digital domain. The DSP uses a numerically controlled oscillator to down-convert the IF signal to baseband and further processing is done to recover the transmitted data. Digitizing at IF places a high sampling

speed requirement on the ADC and the DSP speed as compared to the DCR. This is even more critical because the I and Q baseband channel must be processed concurrently in the DSP section of the receiver. Fig 1.5 shows a typical LIF receiver.

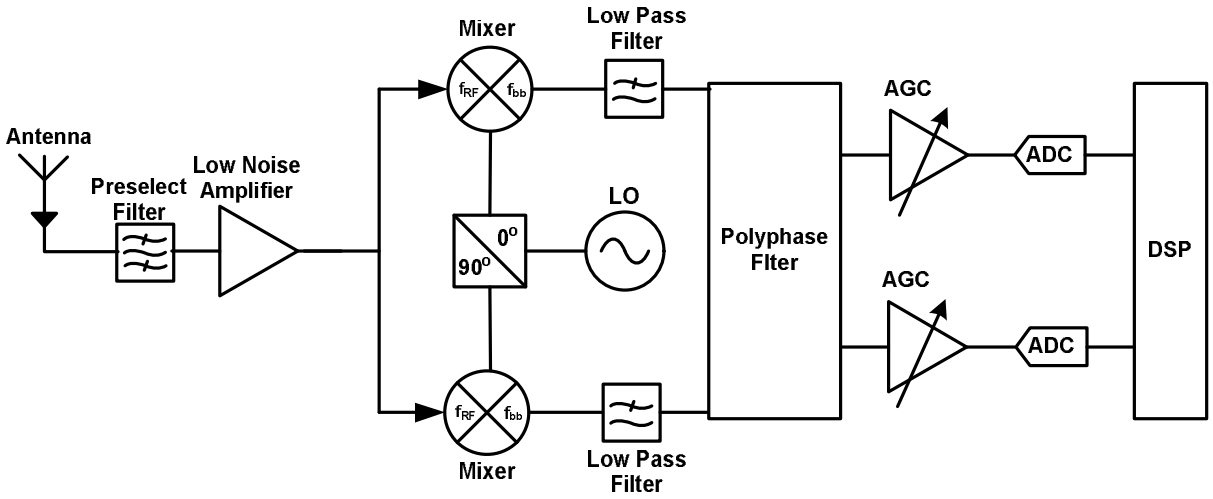


Figure 1.5 Low IF Receiver

1.1.4 Subsampling Receiver

The subsampling receiver as shown in fig. 1.6 uses a sample and hold circuit to down convert an RF signal to an initial low frequency band. The sample and hold circuit, sometimes referred to as a sampler or a subsampling mixer is clocked at a frequency much lower than the RF frequency. The down-converted signal is thereafter digitized and the final down-conversion is done in the digital domain. Channel selection in a subsampling receiver is done in the digital domain which makes about the required flexibility for SDR application.

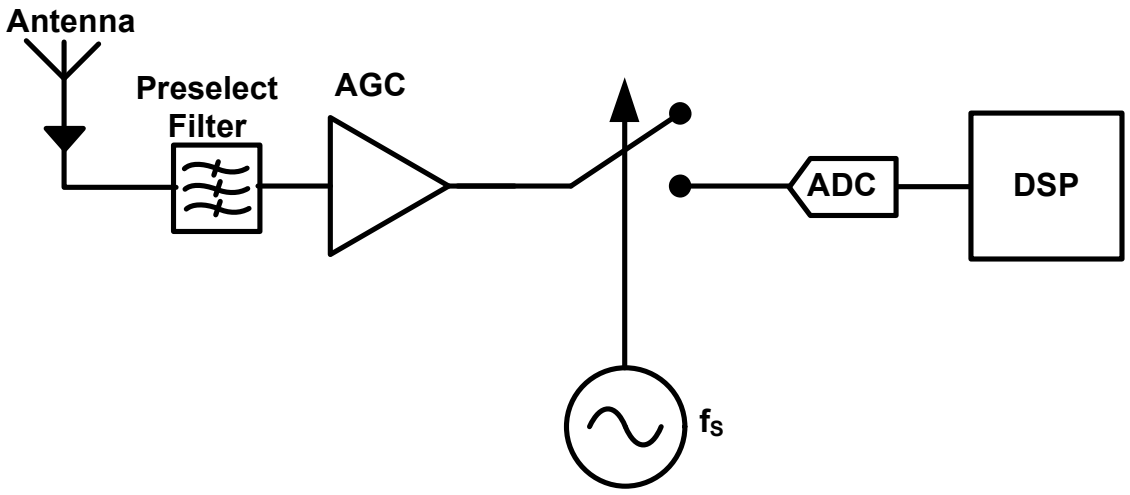


Figure 1.6 Subsampling receiver

However, in order to guarantee acceptable noise floor, the ADC has to run at a relatively high speed (over-sampling gain). Also, the AGC is applied at RF which consumes more power than in other architectures where they are placed at IF or BB. The subsampling receiver also suffers from high noise figure due to jitter noise and noise folding [13].

1.1.5 Six Port Receiver (SPR)

The six port receiver is a relatively newer receiver architecture which is yet to gain much commercial trust in terms of application. It was proposed in [14] [15]. Its structure consists of a passive six port wave correlator circuit and four envelope power detectors. The most commonly used envelope power detectors are diode power detectors. Four of the six ports of the wave correlator circuit are terminated by envelope power detectors while one of the remaining two ports receives the transmitted RF signal and the other, a generated LO signal. Fig 1.7 shows the schematic diagram of a SPR, the SPR has a band preselect filter, an LNA and the frequency conversion stage (consisting of the six-port wave correlator and the diode detectors). Channel

selection and filtering is done in digital baseband thus making the receiver very flexible. The transmitted I/Q data is received from the linear combination of the four power detectors. It is a homodyne receiver as there is a direct conversion from the RF stage to baseband without any IF stage.

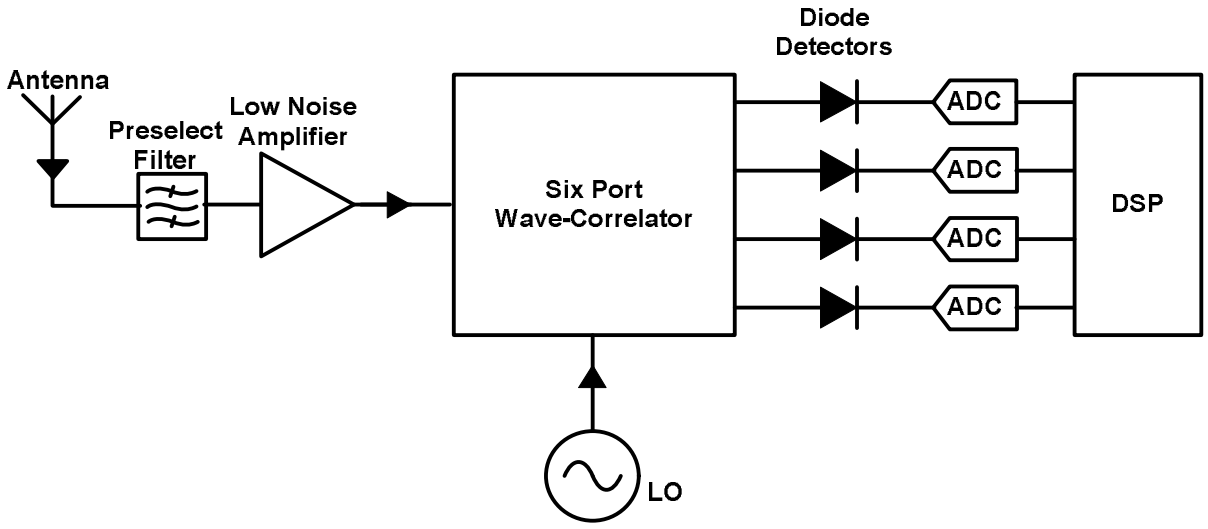


Figure 1.7 Six-Port Receiver

The SPR is a good candidate for SDR applications. It is broadband and the I/Q estimation is done in the digital domain which makes it easily adaptable for different standards. It however suffers from, DC offset and I/Q imbalance which is typical for direct conversion architecture. Another major drawback of this architecture is the non-linearity of the diode detectors used which degrades the performance of the receiver. The diode detectors are also notorious for the limited linear dynamic range. This limits the dynamic range of the entire receiver. A lot of research have been done and are ongoing to optimize the performance of the SPR [18]-[20] and extend its application [20]-[27], as it promises to be a good solution for SDR applications. Recent

achievements in solving the linearity and dynamic range drawback of the SPR have extended its application. The SPR is most desirable at very high frequency (millimeter wave) applications where the design of switching based mixers is challenging [20], [36]. In this work, its application for concurrent multi-band use will be investigated.

1.2 Receiver Architecture Comparison

The ideal SDR as described is not realizable with the current technological state. Hence, different architectures have been employed in modern communication systems to proxy the ideal SDR. It should be noted that the comparison made here is not to determine the best architecture as each architecture has its peculiar application where it is most well suited. Rather, to highlight their advantages and drawbacks in the perspective of a concurrent dual-band receiver operation and design. The superheterodyne receiver (SHR) has superior sensitivity, selectivity and dynamic range due to the multi-stage frequency downconversion and the use of SAW filters for accurate channel selection. It is the most employed in high end receiver designs where robustness against interference and a very good signal quality are required. It relies on tedious frequency planning and bulky filters at different stages along the receiver paths to correct image problems and for channel selection to attain this quality. To use the SHR in concurrent dual-band and in SDR application will imply having a large bank of off-chip IF filters with each one dedication to a particular standard. This will increase the cost, power requirement and size of the receiver.

The direct conversion receiver is well suited for SDR applications. With only one stage of frequency conversion and no SAW filters for channel selection, it has a simple structure, which can be integrated in a single chip. New research in design of DCR such as those mentioned in

section 1.1.1 has also improved the performance of the DCR as regards dynamic range and noise figure (NF). These advanced architectures use noise cancelling techniques and impedance translation [10], [11] to improve noise performance and channel selectivity of the receiver. This improvement however comes with increased complexity in the structure. Design of switching mixers at millimeter wave frequency is challenging with respect to the input matching at the RF port of the mixer. Also, jitters are more pronounced at these frequencies with resultant high phase noise. This results in blocker degradation of the receiver.

In the low IF receiver architecture, impairments due to $1/f$ noise, DC offset, self-mixing, LO leakage etc. are greatly reduced and it lends itself to easy integration like in the DCR. The sampling frequency requirement on the ADC is however high because the signal is digitized at IF. The polyphase filter in the structure is implemented in the digital domain and the digitized I and Q data at IF are processed concurrently thereby placing a stringent condition on the processor speed.

The noise figure of the subsampling is its main undoing. This limits its use to cheap low end receivers with low data transfer rate. New architectures based on the subsampling technique are being investigated though to mitigate this problem.

The six port receiver is a relatively new receiver technique as compared to other architectures. It is a homodyne receiver thus well suited for SDR applications, being reconfigurable, multistandard and broadband. The six port correlator has a low power requirement since it uses passive components and generally does not require high power for the LO and RF signals [20]. Similar to DRC receiver, channel selection is done in baseband hence making the receiver highly flexible at the cost of a loss in Dynamic range. in addition, the typically short dynamic range of the envelope power detectors reduce the dynamic range of the SPR even further. The non-

idealities in the design of the passive six port circuit also lead to DC offset and I/Q imbalance. However, as will be seen in chapter two, the SPR uses four diode detectors at its output enabling suitable calibration to correct the DC offset and I/Q imbalance. Circuit integration can be another challenge due to the size of the wave correlator. For this, suitable technologies such as LTCC and MMIC can be utilized to design smaller wave correlator suitable for miniaturized circuit integration. The SPR becomes an interesting option at millimeter wave applications when the design of traditional switching-mixers is challenging and also for concurrent dual band receiver applications as will be explained in the following section. This work uses this receiver architecture coupled with suitable calibration technique to design a novel model for a concurrent dual-band receiver which is well suited for SDR applications.

1.3 Concurrent Multiband Receivers

Modern communications systems provide numerous wireless applications and services. Applications such as GPS, voice communication, data transfer, WiFi, Bluetooth, personal area networks (PAN), near field communication (NFC), RFID etc. operate using different protocols in different frequency bands. This diverse range of modern wireless applications and services necessitates transceiver front-ends with wider bandwidth and flexibility to maintain the plurality of the services. Spectrum aggregation which is one of the techniques used to increase communication throughput needs a receiver that is able to concurrently receive and process signal in multiple bands [27]. In addition, multitasking is an incentive to customers in todayôs wireless communication services, being able to simultaneously use more than one wireless service. Of course, the first point of call is to design terminals with SDR potential for flexibility, reconfigurability and easy evolution. The concept of concurrent multiband operation in RF

engineering takes it further to improve the overall communication throughput and also to use more than one communication service at a time. In literature, there are two distinguishable categories of multiband receivers: non-simultaneous receivers and simultaneous receivers (concurrent receivers). To address the multitasking and or spectrum aggregation requirement, the concurrent case is desired. State-of-the-art concurrent multi-band receiver architectures utilize the front-end stack-up technique, which is achieved by building several individual receiving paths with each path dedicated to receiving only one signal [5].

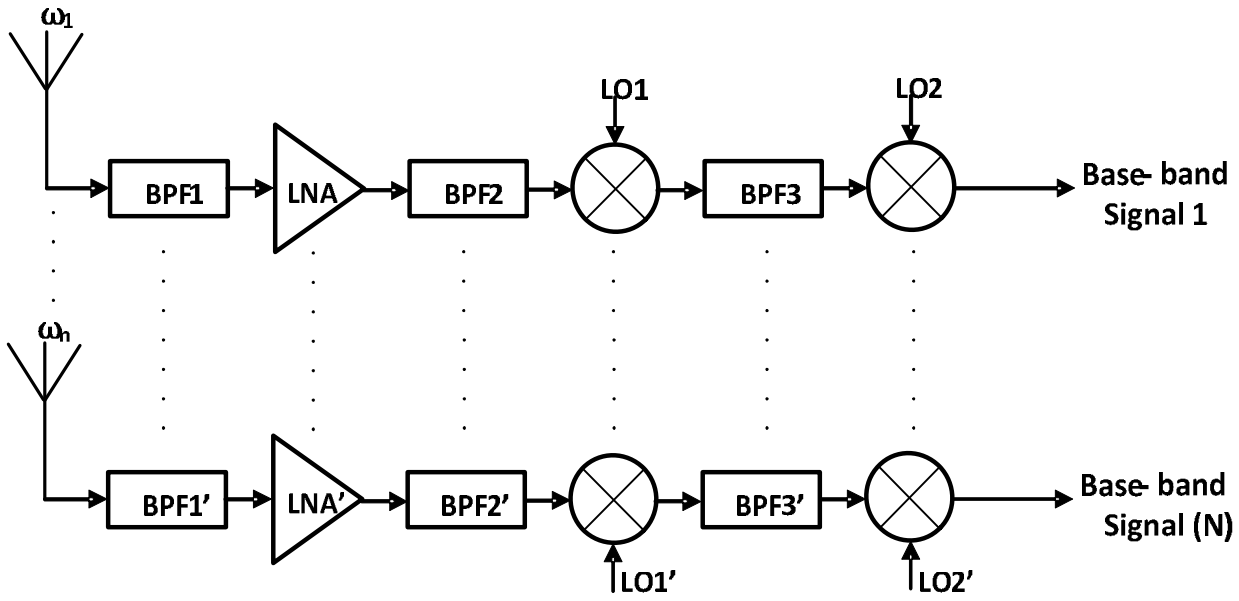


Figure 1.8 Front-end stack-up technique in Multiband Receiver Design

While the front-end stack-up technique having N separate receiver paths for N different signals has very good performance, it makes for a complex structure with higher cost, size and power requirement. Consequently, a lot of research has been done and are ongoing, which are aimed at reducing component duplications in the transition from single to concurrent multiband operation. Typically, the first hurdle is a concurrent dual-band receiver structure. There has been success in

the design of a dual-band antenna [30], dual-band low noise amplifiers [29, 31], and dual-band filters [32]. However, not a lot of progress has been made in the frequency conversion stages of the receivers (mixers). Fig 1.9 shows the conceptual evolution of a concurrent dual-band receiver, starting with two totally independent heterodyne receiving paths, and leading to an efficient concurrent dual-band receiver.

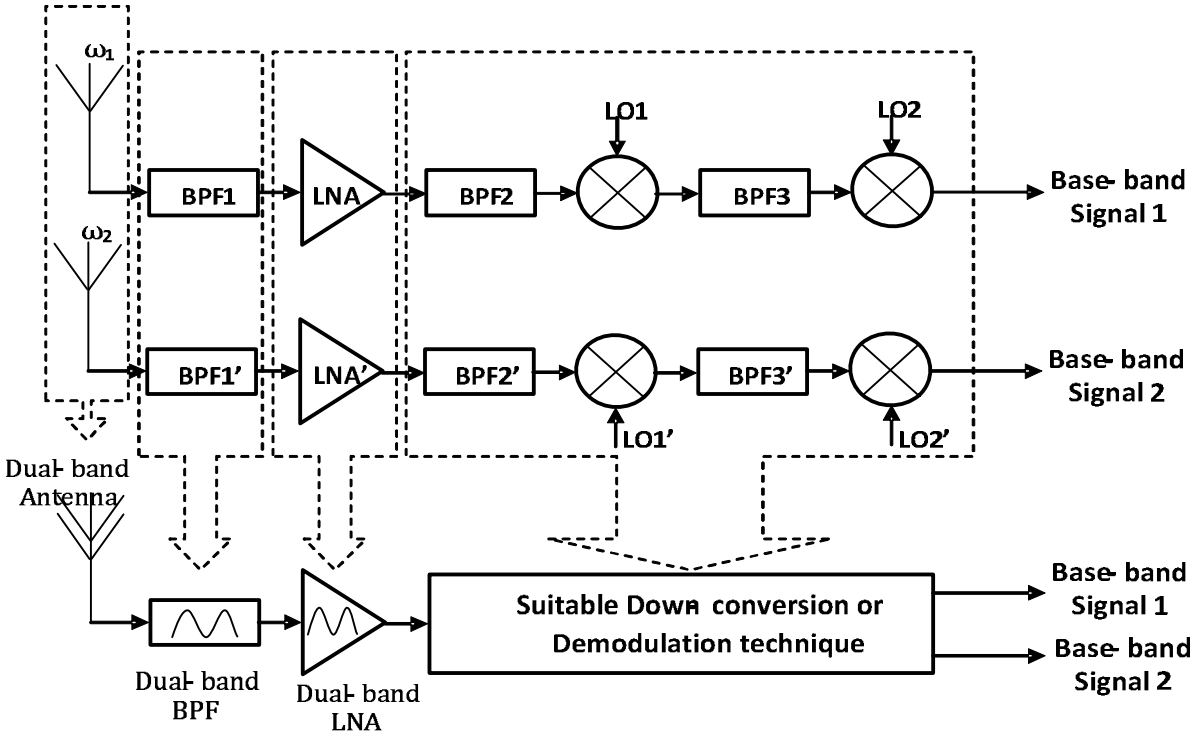


Figure 1.9 Evolution of dual-band receivers from single-band receivers

C. F. Jou et al [33] proposed a single mixer solution for the frequency translation in the receiver front end. This however has fixed frequency bands for LAN applications, thus limiting its flexibility and reconfigurability which is required for SDR applications. Consequently, an alternative receiver structure which is able to concurrently receive dual-band signals is required. Such receiver should be flexible, broadband and reconfigurable to avail itself for use in SDR

applications. In [34], we reported a novel concurrent dual-band six port receiver which shows good performance when tested with real communication signals (WCDMA and LTE). Details of this are provided in chapter four. A similar work was reported afterwards in [35] which uses a mixer based DCR architecture in a spectrum aggregation system to receive signals in three bands concurrently. In this work, three signals (QPSK, 8PSK and 16QAM) with 100KS/s symbol rate were received with error vector magnitudes of -22dB (7.9%) in the first and second band and -25dB (5.6%) in the last bands. The works reports that the main contributors to the high EVMs are intermodulation products and spurs at the output of the mixer. Spurious degradation is typical with mixer based receivers because of the mixing of fundamental and harmonic products generated which is even more pronounced in concurrent multi-band operation when more than one RF signal and LO signals are involved. This thesis explores the SPR technique and its application as a concurrent dual-band frequency downconverter in real communication systems. It proposes a new concurrent SPR model which does not duplicate any hardware resource and leverages on the broadband, low power and reconfigurable properties of the SPR for SDR applications.

1.4 Thesis Contribution

The contributions of this work to the RF engineering community can be summarized below, details of which are given throughout the thesis.

I. A performance analysis of a six port receiver in a 3G (WCDMA) communication system was done, and detailed in chapter three. The communication system includes a multi-path fading channel with four signal paths and an additive White Gaussian noise. A bit error rate (BER) profile for two different calibration technique were plotted and analyzed to

ascertain the viability of the SPR front end in the communication system. The receiversô performance for a 4G (LTE) communication system was also investigated.

II. Conventional dual-band receivers are designed using the front-end stack-up technique which increases the size, cost and power requirement of the receiver. A mathematical model for a concurrent dual-band SPR was developed. The receiver uses the same hardware requirement as the single band SPR without duplicating any component in the downconverter path. Leveraging on the advantages of the SPR FE which is broadband, multistandard and easily reconfigurable, the receiver is found to be well suited for concurrent dual-band SDR applications.

III. Considering the inherent imperfections of the SPR, a suitable calibration technique was developed for the dual-band SPR to mitigate the nonlinearity, low dynamic rate, LO leakage, DC offset and all other imperfections which will otherwise adversely affect the performance of the receiver.

The work carried out for this thesis resulted in the following peer-reviewed publications:

1. A.O. Olopade, A. Hasan and M. Helaoui, ñConcurrent Dual-band Six-Port Receiver for Multi-standard and Software Defined Radio Applicationsò IEEE Transaction on Microwave Theory and Techniques, in press.
2. A.O. Olopade and M. Helaoui, ñPerformance Analysis Of A Six Port Receiver In A Wcdma Communication System Including A Multi-Path Fading Channel,ò Journal of Electrical and Computer Engineering, in press

1.5 Thesis Outline

This thesis is outlined as follows; the first chapter discussed the need for a universal front end solution in the form of a software defined radio (SDR) to cope with the continuous proliferation of wireless communication standards. It outlines the different modern receiver architectures including the six port receiver architecture, their advantages and limitations with regards to SDR applications. The need for concurrent multiband receiver architectures is established and the state-of-the-art architecture for concurrent multiband receivers and it drawbacks are discussed. This chapter finally outlines the contributions of this thesis. Chapter two gives a detailed description of the six port receiver, its structure, limitation and calibration for error correction. Chapter three explores the use of the SPR in real communication systems with a MATLAB model of a 3G (WCDMA) communication system and a 4G (LTE) communication system using a SPR front-end. A new concurrent dual-band SPR model is described in chapter four with its calibration and suitable measurements taken to validate its performance. Chapter five concludes this work and makes recommendation on future works.

1.6 Conclusion

The need for a flexible, broadband and reconfigurable receiver front-end which will serve as a close substitute for the elusive ideal SDR was established. Furthermore, the need for multiband receiver to expand the capabilities of communication systems and to avail the use of multiple wireless services simultaneously was highlighted. A review and comparison of the existing modern single band receiver architectures was done with a view to understanding their positives and drawbacks. A comparison of the different architectures shows that the direct conversion receiver architecture seems to be the most suited for SDR applications. Afterwards, the front-end

stack-up technique, which is the prevailing architecture in modern multiband receiver designs, was discussed. This technique involves building several individual receiving paths with each path dedicated to receiving only one standard. Receivers designed with this technique are more complex in structure, have a bigger size and have high cost and power requirement. Hence a solution with a simple structure that can be used for concurrent signal reception is required, for which the first hurdle will be the design of a concurrent dual-band receiver. This work proposes a SPR model, which uses the same structure as the single band SPR but differs in the DSP baseband processing to recover two transmitted signals concurrently. A suitable calibration technique is developed for the receiver and its usefulness for real communication signals is demonstrated. The outline and the contribution of the thesis are also highlighted in this chapter.

Chapter Two: **Single Band Six Port Receiver (SPR)**

2.1 Introduction

In the previous section, we have briefly introduced the six port receiver. It is a direct conversion receiver which was first introduced by the work of J. Li [14, 15]. Prior to its use as a receiver, the six port technique was used to solve power measurement problems [17] and as an alternative network analyzer to determine the reflective coefficient of a device under test (DUT) from the ratio of the reflected wave to incident wave at the port [16]. It has also been applied in load-pull and source-pull measurements, device characterization, antenna measurement systems and radar systems [36]. A six port receiver comprises of a six port wave correlator and four envelope power detectors.

2.2 Structure of a Six Port Receiver.

The SPR is composed of the following subcomponents;

- Wideband Antenna: - the antenna should be wideband to cover the frequency range for SDR application for which the SPR is to be used.
- Broadband LNA and AGC: - these are basic components in any receiver architecture to enable a very good receiver sensitivity and dynamic range. They should also be broadband to cover the frequency range for which the receiver is to be used.
- Broadband Six port junction: - the six port junction is also called a wave correlator. It is a passive microwave junction with six ports. It has been constructed in a variety of ways in literature. Fig. 2.1 shows a design based on a symmetrical five port ring junction and a directional coupler, while fig. 2.2 shows a structure designed with a Wilkinson divider and three directional couplers.

Application of the six port technique in receiver application is essentially in the frequency down conversion stage which comprises the six port wave correlator and the diode detector. Other fundamental components of receivers such as the LNA, channel selection filter etc. are also vital components. It should however be noted that subsequent reference to the ñsix port receiverò in the thesis refers to only the frequency down-conversion stage of the receiver. This nomenclature is commonly used in research papers using the six-port wave correlator for frequency down-conversion.

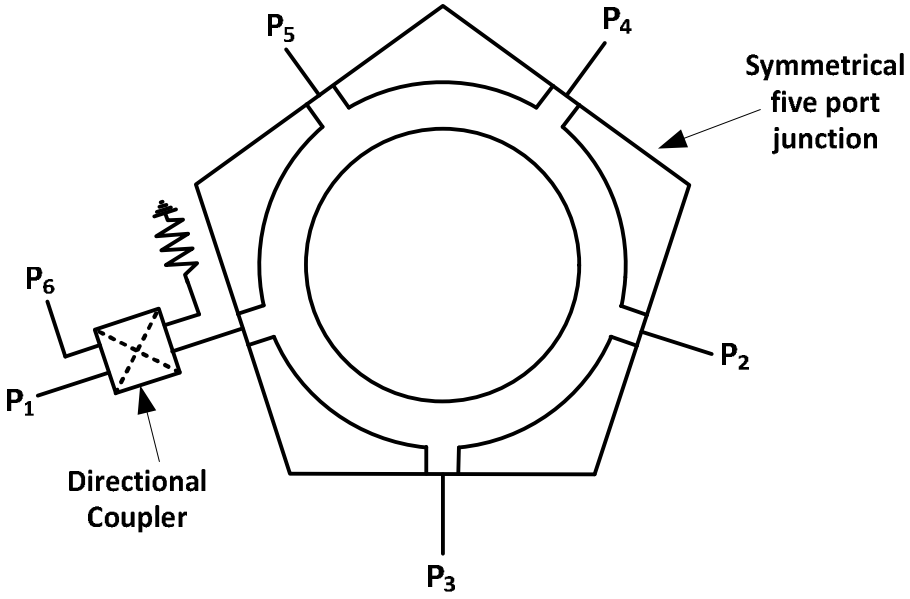


Figure 2.1 a symmetrical five port ring junction and a directional coupler based six port wave correlator

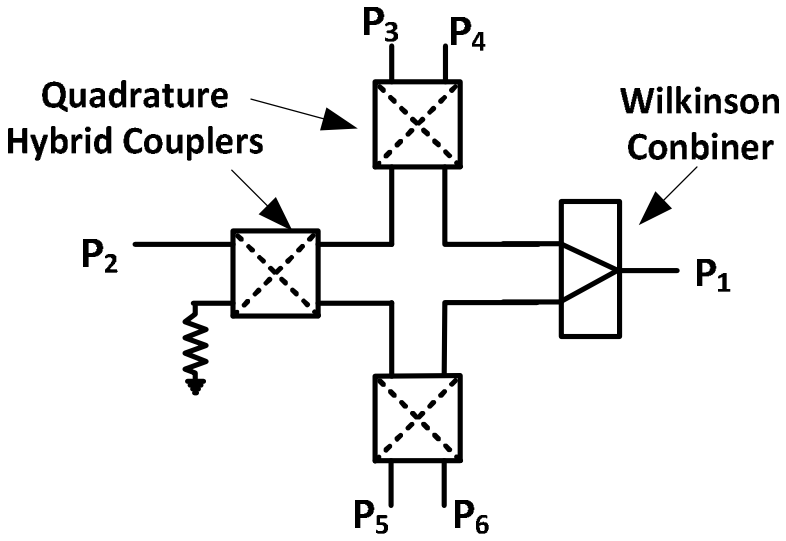


Figure 2.2 Wilkinson divider and directional couplers based six port wave correlator

The second structure with a Wilkinson divider and directional coupler was used in this work because it has better isolation between ports 1 and 2 and it also enables a linear calibration for the receiver. It also avails itself for a broadband or dual-band design more easily to compare with the five port ring junction structure.

- High dynamic range wideband power detectors: - the most commonly used power detectors in the SPR is the diode detectors. They are small in size and have low power requirement. The power detectors generate a voltage output in response to the power of the incident microwave signal at its input. The detectors have a square law relationship between the output voltage and the input RF power. The range of power for which this relationship holds is referred to as the linear range or the square law region of the detector.

- Analog-to-digital converters (ADC): - four ADCs are used in the SPR, they digitized the baseband output of the power detectors for further processing in the DSP. This enables the multi-standard property of the SPR.
- Digital Signal Processing (DSP): - this is the last and final stage of the SPR. It uses a set algorithm that combines the measured voltages from the power detectors to estimate the transmitted I/Q data.

The power detectors generate voltages in response to the microwave power at their input ports. The input power range, over which the voltage generated by a power detector is proportional to its input power, is called the linear range of the power detector. The diode based power detectors are notorious for their limited linear dynamic range. When these detectors are used in a SPR system, they limit the dynamic range of the whole receiver system

2.3 Theory of the SPR

We discussed the structure and components of a SPR in the previous section, it comprises of a six port wave correlator and four envelope power detectors. Fig 2.3 shows a SPR structure using three quadrature hybrid couplers and a power divider for the wave correlator circuit and diode power detectors (D3 to D6) for the envelope detectors. The LO and RF signals have the same center frequency for homodyne operation and are fed through ports P1 and P2 respectively while the power detectors are connected to ports P3 to P6. The SPR operates using an additive mixing of the RF and LO signals in the SPR wave correlator and then a square law processing by the diode power detectors. The wave correlator has pre-defined phase-shifts and attenuations for the

LO and the RF signals such that these two input signals generate different amplitudes and phases at the four output ports [37].

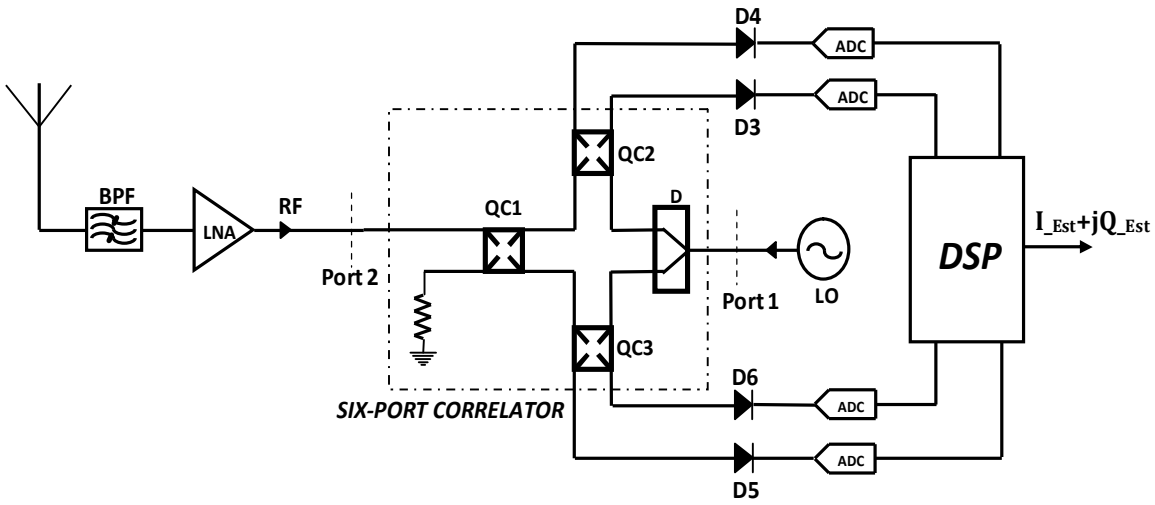


Figure 2.3 Typical Six Port Receiver Architecture

The I/Q information can be recovered from the four diode measurement at the output ports. Equation (1) gives the diode output power (Pi) expression in terms of the S-parameters of the six port wave correlator.

$P_i = |S_{i2}a_2 + S_{i3}a_3|^2$ for i = 3,4, ... 6 (2.1)

Where

$a_2 = \frac{1}{\sqrt{2}}|a_2|e^{j\phi_2}$ is the LO signal

and $a_3 = \frac{1}{\sqrt{2}}|a_3|e^{j\phi_3}$ is the RF signal.

Expanding equation (2.1) gives;

$P_i = |S_{i2}|^2|a_2|^2 + |S_{i3}|^2|a_3|^2 + 2|S_{i2}||S_{i3}||a_3|\cos(\phi_{i2} - \phi_{i3} - \phi_3) -$

$2|S_{i2}||S_{i3}||a_3|\sin(\phi_{i2} - \phi_{i3} - \phi_3)$ for i = 3,é ,6 (2.2)

Where I and Q are the transmitted I/Q data, $\emptyset_{32}$ is the phase relationship between ports P_i and port 2 and $\emptyset_{31}$ is the phase relationship between ports P_i and port 1.

Equation 2.2 can be expressed in matrix form of all diode power measurements P_3 to P_6 as;

$$\begin{bmatrix} P_3 \\ P_4 \\ P_5 \\ P_6 \end{bmatrix} = \begin{bmatrix} c_{31} & c_{32} & c_{33} & c_{34} \\ c_{41} & c_{42} & c_{43} & c_{44} \\ c_{51} & c_{52} & c_{53} & c_{54} \\ c_{61} & c_{62} & c_{63} & c_{64} \end{bmatrix} \begin{bmatrix} I^2 + Q^2 \\ I \\ Q \\ 1 \end{bmatrix} \quad (2.3)$$

Where $c_{31} = |S_{32}|^2|c_{31}|^2$

$c_{32} = |S_{32}|^2$

$c_{33} = 2|S_{32}||S_{31}||c_{31}|\cos(\emptyset_{32} - \emptyset_{31} - \emptyset_{31})$ and

$c_{34} = 2|S_{32}||S_{31}||c_{31}|\sin(\emptyset_{32} - \emptyset_{31} - \emptyset_{31})$

The matrix $[R]_{4X4}$ is dependent on the S-parameters of the six port wave correlator and the amplitude of the LO signal. From equation 2.3, the transmitted I and Q data can be recovered from a linear combination of the four diode output as expressed in the following equations.

$$I_{EST} = \sum_{i=3}^{6} \alpha_i P_i \quad (2.4a)$$

$$Q_{EST} = \sum_{i=3}^{6} \beta_i P_i \quad (2.4b)$$

Equations (2.4a) and (2.4b) can be expressed in matrix form as below;

$$\begin{bmatrix} I_{EST} \\ Q_{EST} \end{bmatrix} = \begin{bmatrix} \alpha_3 & \alpha_4 & \alpha_5 & \alpha_6 \\ \beta_3 & \beta_4 & \beta_5 & \beta_6 \end{bmatrix} \begin{bmatrix} P_3 \\ P_4 \\ P_5 \\ P_6 \end{bmatrix} \quad (2.5)$$

where α_i and β_i are the calibration constants of the six-port receiver, I_{EST} and Q_{EST} are the estimated in-phase and quadrature component of the received signal, and P_i (for i = 3, ...,6) are the diode output powers for all four detectors.

2.4 Limitations of the SPR

As mentioned earlier, the ideal six port wave correlator has specific pre-defined phase and amplitude relationship for optimum performance in the demodulation process of the receiver. These conditions must be constant and valid over the entire bandwidth of operation of the SPR [7].

- The conditions on the wave correlator are:

1) $|S_{□□}| = |S_{□□}|$ and $|S_{□□}| = |S_{□□}|$
2) $|S_{□□}| = |S_{□□}|$ and $|S_{□□}| = |S_{□□}|$
3) $\angle S_{□□} = \angle S_{□□} + 90°$ and $\angle S_{□□} = \angle S_{□□} + 90°$
4) $\angle S_{□□} = \angle S_{□□} + 90°$ and $\angle S_{□□} = \angle S_{□□} + 90°$
5) $\angle S_{□□} - \angle S_{□□} - \emptyset_{□□} = 2n\pi,\ n = 0,1,2 \ldots,$
6) $\angle S_{□□} - \angle S_{□□} - \emptyset_{□□} = (2n + \frac{□}{□})\pi,\ n = 0,1,2 \ldots,$

where S_{ij} are the s-parameters of the wave correlator, and $\emptyset_{□□}$ is the initial phase of the LO signal.

In addition, all four diode detectors must operate within their square law region ($P_□ = K_□V_□$ i = 3,4..6) at all times and they must have identical response, i.e. $K_□$ is the same for i = 3,4, ... 6. The In-phase component of the RF signal is estimated from diode output D3 and D4 while the quadrature component is estimated from D5 and D6. However, a shift from the optimum conditions listed above will result in distortion, DC offset, and I/Q mismatch thus reducing the fidelity of the receiver.

The conditions on the wave correlator are very stringent to meet over a wide frequency band and the performance of microwave devices are best guaranteed at their design frequencies. This spells a shift from the ideal operating condition of the SPR. Also, the isolation between the RF and LO ports must be very high to guarantee good operation of the receiver. Imperfections in the wave correlator results in LO leakages, DC offset and I/Q imbalance. The diode detectors are notorious for their limited dynamic range; thus limiting the dynamic range of the whole receiver.

It has also been reported in [19, 38] that the diode detectors exhibit a frequency response, meaning that the input power-output voltage relationship of the diode is dependent on the frequency of the input excitation signal. These issues results in a heavy degradation in the performance of the SPR particularly when real wideband modulated signals are used in the communication system. This has prompted a lot of research work in proposing suitable calibration techniques to mitigate the hardware imperfections of the SPR. The calibration technique should be able to rectify the imperfections in the wave correlator construction, extend the dynamic range of the receiver and mitigate the frequency response of the diode detectors. The drawbacks of the SPR can be summarised under the following points;

- Non-flat frequency response of the quadrature hybrids couplers, power divider and connectors,
- Unequal power divisions for the power dividers and quadrature hybrids couplers,
- Deviation of phase differences from ideal for the hybrids in the whole band of operation
- Memory effects displayed by the diode power detectors
- Nonlinearities of the diode power detectors.

2.5 SPR Calibration

The main issues with the ideal SPR system have been discussed in the preceding section, these problems results in the degradation in the receiver performance. In an effort to mitigate these imperfections, some SPR designs have been proposed using quasi-ideal components and restricting the operation region of the receiver to the dynamic range of the diode detectors [18], [20-25] which results in a short receiver range. Depicted in fig. 2.4 below, it consists of a six-

port wave correlator, four diode detectors and two voltage difference amplifiers used to recover the transmitted I/Q data. The architecture is designed such that all the microwave devices are very close to ideal. This makes for a near perfect SPR. However, this performance is only guaranteed at the design frequency. A shift from the center frequency degrades the receiver considerably.

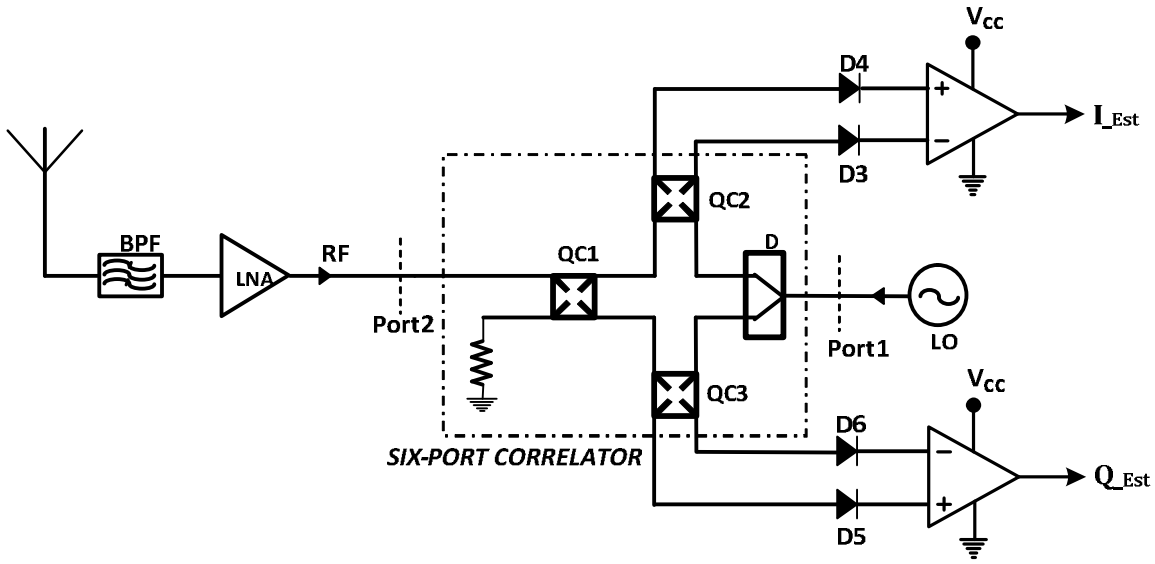


Figure 2.4 Typical Six Port Receiver Architecture

These techniques also do not take into consideration the frequency response of the diode detectors. Hence, a suitable calibration technique that mitigates all the outlined drawbacks is required. Calibration of the SPR usually involves sending and receiving a known training signal, which is similar in characteristics to the signal to be received and subsequently estimating the coefficients used to recover the unknown transmitted information.

2.5.1 Direct Linear Calibration

Equations (2.4a) and (2.4b) represents the estimation expression for the I and Q data to be received. $\alpha_{\hat{I}}$ and $\beta_{\hat{I}}$ are the calibration coefficients to be determined. The least square method is

used to estimate the calibration constants from the known training sequence and the measured voltage output of the diode detectors.

The direct approach is able to effectively correct the wave correlator non-idealities. It however does not correct the frequency response of the diode detectors and their notoriously short dynamic range. Hence, this linear calibration is sometimes used with a look-up table to compensate for the nonlinear distortion of the diode. This means that the calibration and estimation is done in two steps.

2.5.2 Memory Polynomial Calibration

Hasan et al. in [19] proposed a black box modeling technique for the SPR which simultaneously compensates for the six port wave correlator and diode detectors non-idealities. The technique uses a modified memory polynomial to model the frequency response of the diode detector and infuses this model directly into the SPR linear calibration such that the calibration is done in one step and corrects both wave correlator non-idealities and diode frequency response. Equation (2.6) gives the expression to estimate the transmitted I/Q using the memory polynomial technique.

$$I + jQ_{est}(n) = \sum_{p=1}^{N} \sum_{q=0}^{M} \sum_{d=0}^{p} A_{pqd} v_d^{p}(n-q) \qquad (2.6)$$

A_{pqd} are the complex predetermined calibration constants from a training signal. M is the memory depth and N is the nonlinearity order of the modified memory polynomial calibration model. It is a one-step calibration technique that has a higher DSP resources requirement but it was reported to have a significantly better performance than the conventional linear calibration technique. This calibration technique was used in this thesis work due to its good performance and ease of implementation.

The following section briefly describes the least square algorithm used to estimate the calibration coefficients from a training signal.

2.5.3 Least Square Technique

Equation 2.6 can be rewritten in matrix form as;

$$Z = \phi C \qquad (2.7)$$

Where ϕ is the sent training signal $I + jQ$

$C = [C_{103} \quad \dots \quad C_{003} \quad C_{113} \quad \dots \quad C_{013} \quad \dots \quad C_{003} \quad \dots \quad C_{006}]$ is a matrix of the complex I/Q estimation coefficient and Z given below is a matrix of the diode voltage output.

$$Z = \begin{bmatrix} V_1[n] & \dots & V_8[n], & V_1[n-1] & \dots & V_8[n-1] & \dots & V_1[n-m] & \dots & V_8[n-m] \\ V_1[n+1] & \dots & V_8[n+1], & V_1[n] & \dots & V_8[n] & \dots & V_1[n-m] & \dots & V_8[n-m] \\ & & & \vdots & & & & & & \\ & & & \ddots & & & & & & \\ V_1[n] & \dots & V_8[n], & V_1[n-1] & \dots & V_8[n-1] & \dots & V_1[n-m] & \dots & V_8[n-m] \end{bmatrix} \qquad (2.8)$$

Given a linear equation $y = \phi x$, where $\phi \in \mathbb{R}^{m \times n}$ for m > n. (over-determined set of linear equations)

The residue or error (r) in estimation of y is defined by $r = \phi x - y$

The least square approach seeks to find x_{ls} which minimizes the residue or error $\|r\|$

x_{ls} is referred to as the least-squares (approximate) solution of $y = \phi x$

Assuming A is a full rank matrix, minimizing the norm of the residual squared gives;

$$\|r\|^2 = x^T \phi^T \phi x - 2 y^T \phi x + y^T y \qquad (2.9)$$

Differentiating with respect to x and equating to zero gives;

$$\nabla_{\mathbf{c}} \|\mathbf{e}\|^2 = 2\mathbf{A}^T\mathbf{A}\mathbf{c} - 2\mathbf{A}^T\mathbf{y} = 0 \qquad (2.10)$$

This yields the normal equation

$$\mathbf{A}^T\mathbf{A}\mathbf{c} = \mathbf{A}^T\mathbf{y} \qquad (2.11)$$

Assuming $\mathbf{A}^T\mathbf{A}$ is invertible, we have;

$$\mathbf{c}_{LS} = (\mathbf{A}^T\mathbf{A})^{-1}\mathbf{A}^T\mathbf{y} \qquad (2.12)$$

$\mathbf{A}^{\dagger} = (\mathbf{A}^T\mathbf{A})^{-1}\mathbf{A}^T$ is called the pseudo-inverse of $\mathbf{A}$.

Applying this technique to the problem statement of equation (2.7), the complex calibration coefficients $\mathbf{c}$ can be estimated from the expression;

$$\mathbf{c} = (\mathbf{P}_{\mathbf{p}}^T)^{\dagger}\mathbf{P} \qquad (2.13)$$

where $(\mathbf{P}_{\mathbf{p}}^T)^{\dagger}$ is the pseudo-inverse of $(\mathbf{P}_{\mathbf{p}}^T)$.

2.6 Conclusion

In this chapter, a thorough review of the SPR system for SDR applications was discussed. The different components of the SPR, specifically, the available structures for the six port wave correlator circuit were outlined. The theory of the SPR technique was also explained giving the ideal conditions for its operation. We see that these ideal conditions are in practice quite stringent to achieve over a broad band and as such spells the limitations and drawbacks of the SPR. These limitations affect the performance of the SPR, resulting in issues such as LO leakage, DC offset, I/Q imbalance and a very short dynamic range for the receiver. Consequently, the calibration techniques utilized to correct or mitigate these limitations were discussed.

In the next chapter, a performance analysis of a six port receiver front-end in a modern communication system was carried out. The analysis was done using a WCDMA communication system, which includes a multi-path fading channel to show the practicality of using a SPR.

Chapter Three: **Performance Analysis of a Six Port Receiver in a WCDMA Communication System Including a Multi-Path Fading Channel**

3.1 Introduction

In chapter two of this thesis, we discussed the six port receiver (SPR) technique, giving details on its structure, its ideal operating conditions, limitations, and calibration methods to mitigate these limitations. This chapter seeks to analyze the practicality of the SPR front-end in real communication systems.

Third generation (3G) mobile communication systems introduced in recent years is a huge step in increasing wireless transmission capacity, fidelity and efficiency. Currently, there are fourth generation (4G) communication systems and the proliferation of these standards is still ongoing. As discussed earlier, the increasing number of cellular standards together with the variety of frequency bands these standards use in different regions of the world demands a high degree of reconfigurability. The idea of reconfigurability applies not only to the baseband processing, but also to the RF front-end. The implication is that the receiver front-end (FE) is required to have a wide bandwidth to support a high data transmission rate and it should also be multi-mode and multi-standard to support a fast and constantly evolving modern communication systems. Essentially, it should be forward and backward compatible. Power requirement, fidelity, size and cost are also paramount properties to consider in a receiver front-end design. The SPR can conveniently be design over a broad band thereby supporting high data rate and it is reconfigurable. However, the high speed 3G and 4G communication systems are more sensitive to distortions and channel effects. The implication in that a slight shift from the ideal condition in the receiver of transmission medium degrades the received signal considerably. The following section gives a brief description of multipath fading effects in communication systems.

3.2 Multipath Fading

A Multipath fading refers to the phenomenon whereby the signal transmitted from an antenna is propagated to the receiver via two or more paths, each of which may have differing lengths and associated time delays. The fading results from the constructive and destructive combination of randomly delayed, reflected, scattered, and diffracted signal components. A component to the multipath effect is the Doppler shift which arises from the relative motion between the transmitter and receiver typical in a mobile environment. This type of fading is relatively fast and is therefore responsible for the short-term signal variations. Figure 3.1 shows a schematic of a multipath fading channel with five paths.

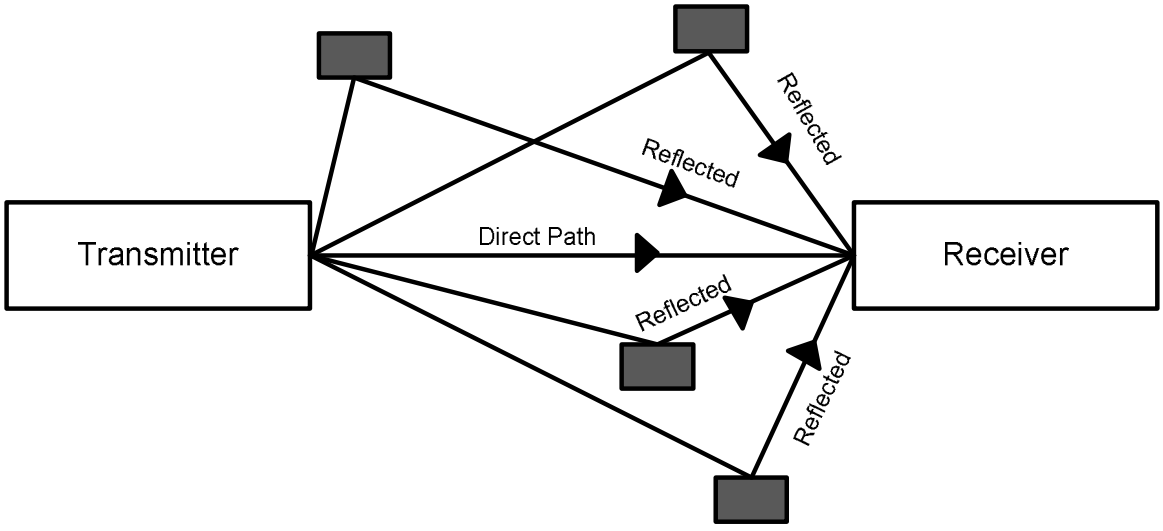


Figure 3.1 Multipath Channel.

Depending on the nature of the radio propagation environment, there are different models describing the statistical behavior of the multipath fading envelope. Two of such models are described below;

3.2.1 Rician Channel

In the Rician multipath fading channel, there is one of the paths, usually the line of sight that is much stronger than the others. In the Rician fading, the amplitude gain of the transmitted signal (x) arriving at the receiver is defined by a Rician probability distribution function P(x) given by;

$$P(x) = \frac{2x(K+1)}{\Omega} e^{-K-\frac{(K+1)x^2}{\Omega}} I_0\left(2x\sqrt{\frac{K(K+1)}{\Omega}}\right) \quad (3.1)$$

where I_0 is the 0th order modified Bessel function of the first kind. K is the ratio between the power in the direct path and the power in the other scattered paths. q is the total power from both paths and acts as a scaling factor to the distribution.

3.2.2 Rayleigh Channel

This defines a channel where there is no dominant line of sight between the transmitter and receiver. It reasonably models the fading effects of heavily built-up urban environment on signal propagation with signals reflected off buildings and other tall objects. In the Rayleigh fading channel, the amplitude gain for a transmitted signal (x) is characterized by a Rayleigh probability distribution function P(x) given by;

$$P(x) = \frac{2x}{\Omega} e^{-\frac{x^2}{\Omega}} \quad x \geq 0 \quad (3.2)$$

Where q is the total power from all paths.

One of the 3G mobile communication standards is the WCDMA communication systems, which compared to the second generation systems has a larger system capacity and greater coverage area to provide higher transmission rate and more services to consumers.

3.3 Six-port receiver in a WCDMA DL communication System

Fig.3.2 shows a MATLAB demo of the WCDMA end-to-end physical layer. It simulates the downlink (DL) path of the frequency division duplex (FDD) downlink physical layer of a WCDMA wireless communication system with the inclusion of the receiver FE. The model has 8 main subsystems listed in table 1 below with a brief description of their functions.

TABLE 3.1: WCDMA end-to-end physical layer Subsystems

	SUBSYSTEM	**FUNCTION**
1	WCDMA DL Tx Channel Coding Scheme	Transport channel encoding and multiplexing
2	WCDMA Tx Physical Mapping	Physical channel mapping
3	WCDMA BS Tx Antenna Spreading and Modulation	Modulation and spreading
4	WCDMA Channel Model	Channel model
5	Receiver Front End	RF signal reception and frequency demodulation
6	WCDMA UE Rx Antenna	Despreading ad demodulation
7	WCDMA RX Physical Channel Decoding Scheme	Physical channel demapping
8	WCDMA RX Channel Demapping	Transport channel demultiplexing and decoding

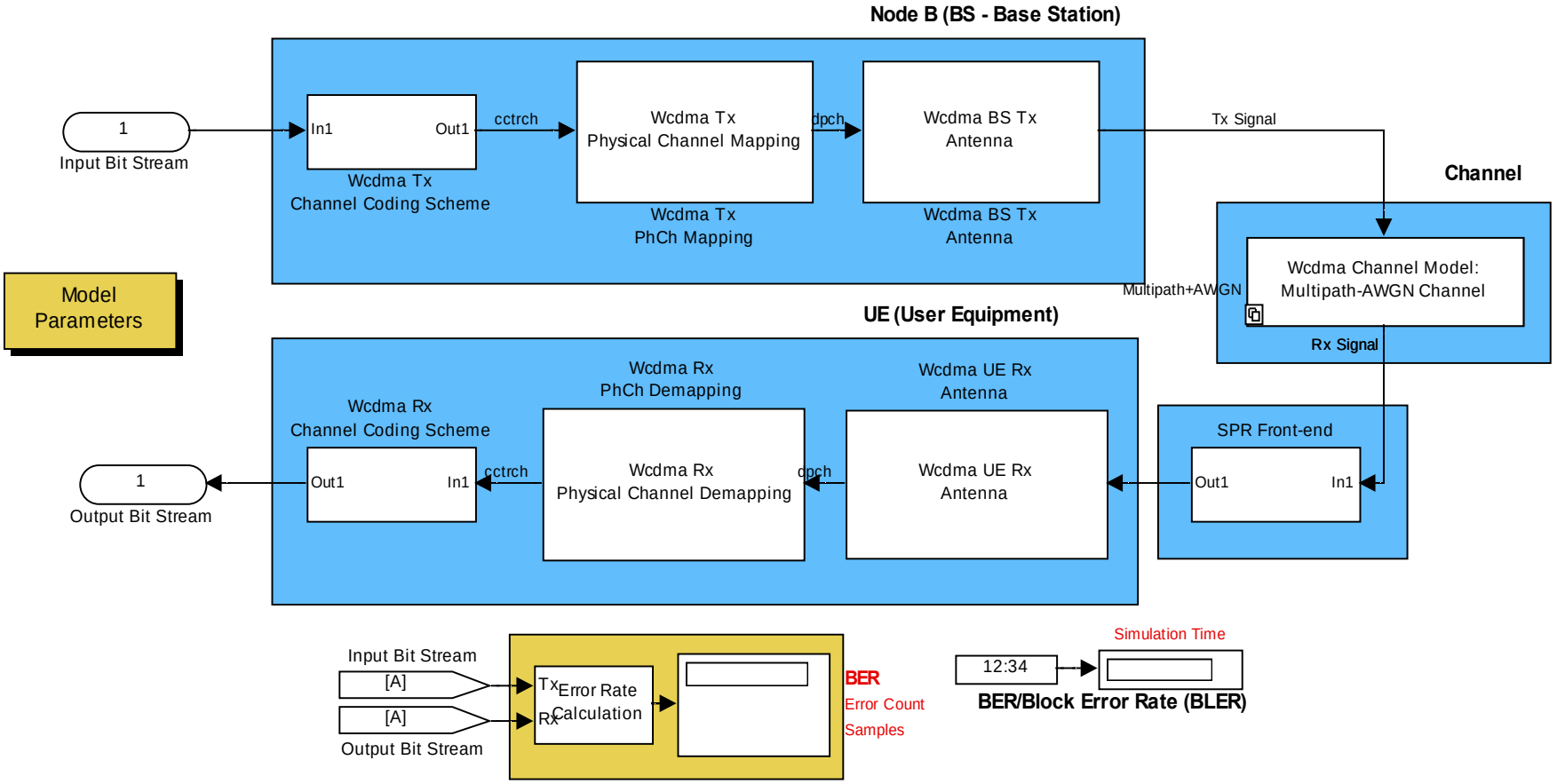


Figure 3.2 MATLAB Simulink WCDMA end-to-end physical layer demo

The DL channels of the demo were set to 384kbps with the default transport block size of [3840 100]. The number of filter taps for the root raised cosine filter was set to 96 and the number of coefficient for the channel estimation filters was 21. The oversampling factor was set to 8. The channel is a multipath channel block with four multipath channels and an additive white Gaussian noise (AWGN) source block. The Rayleigh multipath fading channel model described in was used, the multipath delay channels were set with relative delays of 0 secs, 260e-9 secs, 521e-9 secs, and 781e-9 secs. The corresponding vector of the average power for the delay paths is [0, -3, -6, -9] dB. The speed of the terminal to model the Doppler Effect was set to 120Kmph. The signal to noise ratio of the AWGN was varied between -15dB and 5dB in steps of 2.5dB to plot the BER profile of the receiver system. A fabricated SPR is used as the receiver FE as depicted in the model. A detailed description of the setup for the SPR is given in the following subsection.

3.3.1 SPR Front-End Implementation.

The SPR test bench is assembled as in fig. 3.3. The six port wave correlator is constructed using three quadrature hybrid couplers Q1 to Q3 and a Wilkinson combiner structure as depicted in fig 2.2. Four 8472B Schottky detectors from Agilent Technologies Inc. were used as the power detectors. The generated baseband I/Q data at the output of the channel subsystem of the MATLAB Simulink model is up-converted to 2.5GHz RF using a signal generator (E4438C ESG from Agilent Inc.). The LO signal, also at 2.5GHz is generated using a second signal generator (E8247C from Agilent Technologies). The RF and LO signals are passed into the SPR and the voltages generated by the diode detectors are captured and digitized with a four channel mixed

signal oscilloscope (infiniium MSO9404A from Agilent Technologies). The captured voltages are imported to MATLAB.

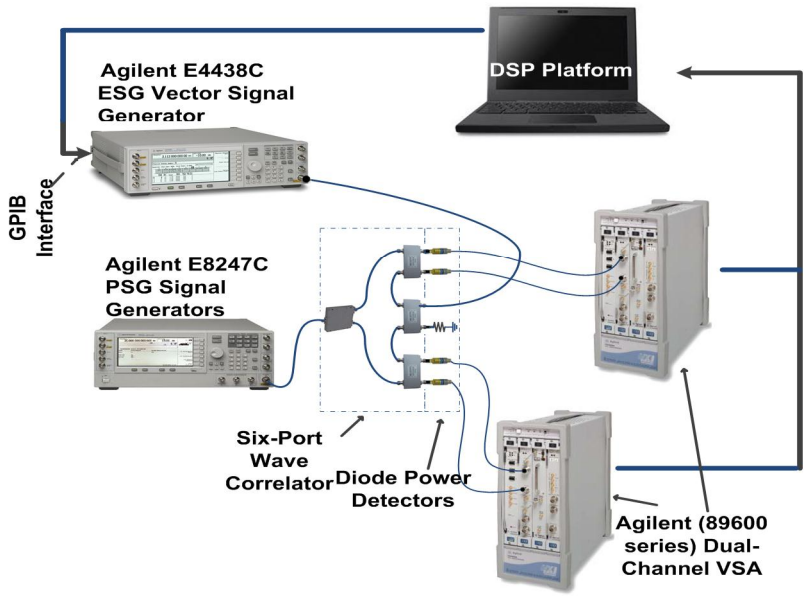


Figure 3.3 Test bench set-up for the SPR Front End.

3.3.2 Receiver Calibration

As discussed in section 2.4 of chapter 2, the receiver has to be calibrated to mitigate non-idealities in the receiver structure. The used calibration technique determines the performance of the receiver. Two calibration techniques were used to estimate the transmitted I/Q data.

- The direct linear calibration: this is the direct linear combination of the diode output voltages discussed in chapter two. For convenience, the expression (2.4a) and (2.4b) used to estimate the inphase (I) and quadrature (Q) component of the transmitted data is repeated here;

$$\hat{I}_{est} = \sum_{q=1}^{Q} \sum_{p=0}^{P} a_{pq} I_{p,q} \quad (3.3a)$$

$$\hat{Q}_{est} = \sum_{q=1}^{Q} \sum_{p=0}^{P} b_{pq} Q_{p,q} \quad (3.3b)$$

- The modified memory polynomial calibration technique discussed in chapter two was also used. The expression (2.6) used to estimate the inphase (I) and quadrature (Q) component of the transmitted data is repeated here for convenience.

$$\hat{I} + j\hat{Q}_{est}(n) = \sum_{k=0}^{K} \sum_{m=0}^{M} \sum_{q=0}^{Q} A_{kmq} v_q(n-k)\,|v(n-k)|^m \quad (3.4)$$

The transmitted I/Q data is estimated using expressions (3.3) and (3.4). The estimated I/Q data is hence transmitted to the UE section of the MATLAB Simulink model as depicted in fig. 3.2 for further demodulation process to recover the transmitted bit.

3.4 MEASUREMENT RESULTS

The performance of the communication system with a SPR front end is evaluated using the bit error rate (BER) of the communication system. The test bench was set up as described in previous section. The RF input power to the SPR FE was 7dBm while the LO power was set to 10dBm. 15,362,048 IQ data points were generated from the WCDMA end-to-end physical layer MATLAB model and sent at an RF frequency of 2.5GHz with the signal generator. A block of 2500 samples of the generated IQ data was used in calibrating the SPR and the estimated

calibration constants were used to recover the remaining IQ data points from the RF signal. To enable a plot of the BER characteristics of the receiver, the signal-to-noise ratio of the generated IQ data point was varied between -15dB and 5 dB in steps of 2.5dB. Measurements were taken for the following scenarios and the corresponding references in brackets are used in the BER plot legend;

- Complete MATLAB simulation without a receiver FE and without multipath channel fading (Matlab_wo_Multipath)
- Complete MATLAB simulation without a receiver FE, with a multipath fading channel (Matlab_w_multipath)
- SPR homodyne receiver FE simulation with a multipath fading channel with memory polynomial calibration technique (SPRmp_w_mutipath) using (3.4)
- SPR homodyne receiver FE simulation with a multipath fading channel with linear combination estimation technique (SPRc_w_mutipath) using (3.3a) and (3.3b)

The first two cases are complete MATLAB simulations, which skip the homodyne receiver block. It assumes a perfect receiver FE which does not introduce any distortion or noise to the received signal. In the third and fourth case, the implemented six-port receiver front-end of Fig. 3.3 is used and along with the signal generation and demodulation in MATLAB. Table 2 shows the measured BER the estimated EVM of the receiver at different SNRs after the multipath fading equalization which is carried out in the WCDMA UE Rx Antenna subsystem of the MATLAB model. Fig. 3.4 shows a plot of the BER characteristics of the communication system. The receiver calibration and IQ demodulation was done at a non-linearity order of 2 memory depth of 4.

From these results, it can be concluded that, in the case of a WCDMA communication system including a multi-path fading channel, both calibration techniques (in the third and fourth cases) are able to provide similar BER performance to an ideal receiver with a multi-path channel. Therefore, both these calibrations are able to compensate for the receiver imperfections to acceptable levels. It is worth mentioning that the calibration technique based on memory polynomials has more coefficients and therefore is more complex to implement.

TABLE 3.2: Estimated EVMs of receiver FE at all SNRs

SNR (DB)	MATLAB_WO_MULTIPATH BER (%)	MATLAB_W_MULTIPATH BER (%)	SPRMP_W_MUTIPATH (N=2, M=4) BER (%)	SPRC_W_MUTIPATH) (N=1, M=0) BER (%)
-15	0.47180	0.4697	0.4687	0.4707
-12.5	0.47000	0.4695	0.4686	0.4701
-10	0.46910	0.4633	0.4636	0.4625
-7.5	0.45900	0.4122	0.4135	0.4167
-5	0.30040	0.2301	0.2346	0.2357
-2.5	0.022310	0.04113	0.04258	0.04486
0	1.53e-05	0.00154	0.00165	0.001945
2.5	0	1.021e-5	3.064e-5	4.085e-5
5	0	5.106e-6	5.106e-6	5.106e-6

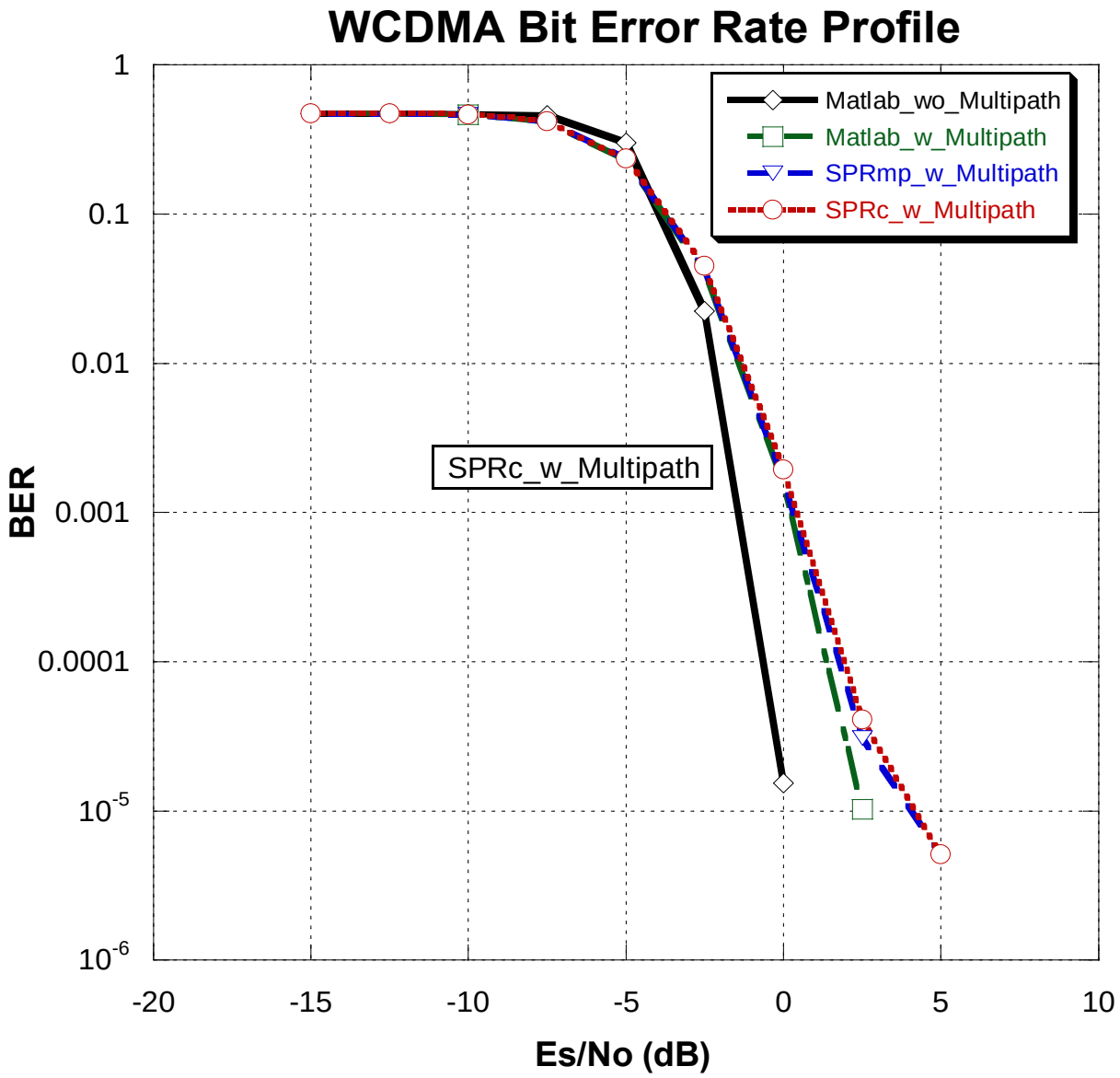


Figure 3.4 BER plot of the communication system.

3.5 4G LTE System

The bock diagram of fig. 3.5 describes a similar setup for an LTE based communication signal.

Here, transmit and receive antennas were used to set up a wireless communication link.

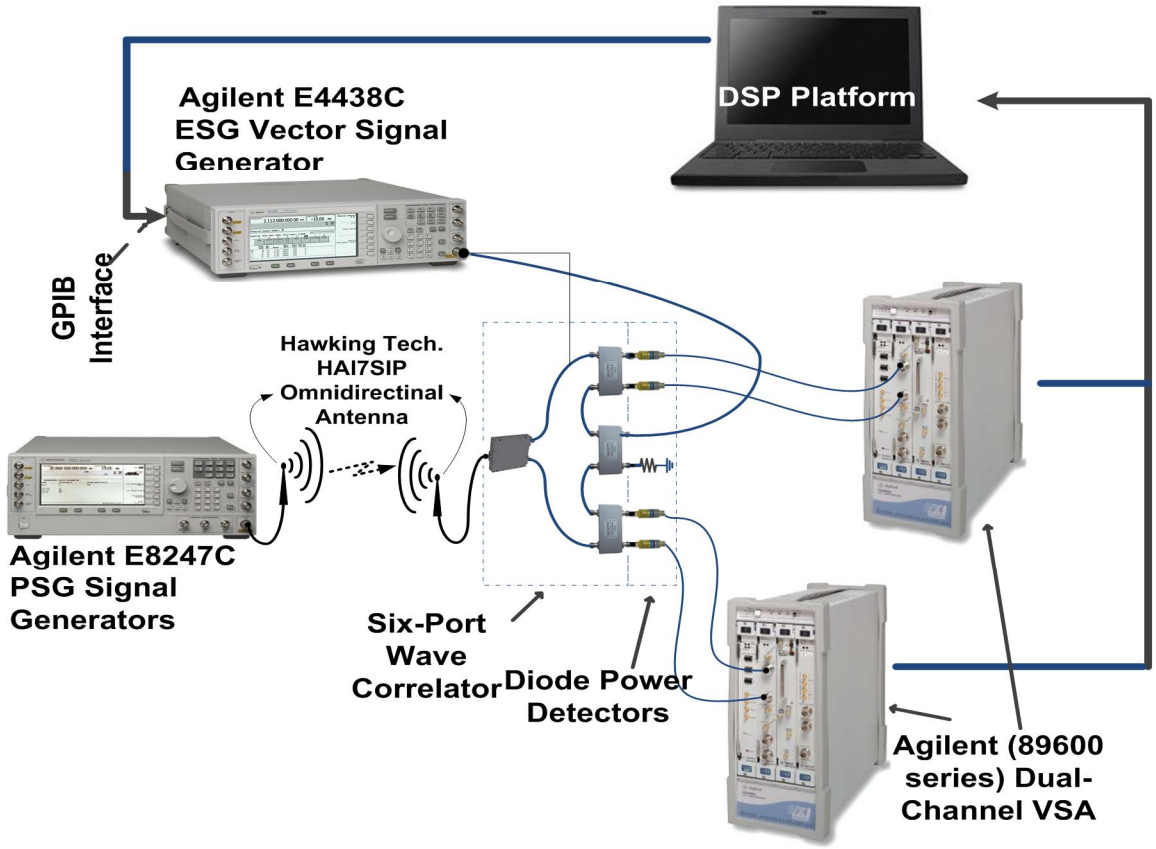


Figure 3.5 Test bench set-up for the SPR Front End using transmitting and receiving antennas

This is to verify the suitability of the SPR for real communication signals with high data throughput. A 3 MHz bandwidth LTE signal was sent and received at 2.4 GHz using two commercially available omnidirectional antennas (Hawking Tech. HAI7SIP). The resulting EVM of the received I/Q data as compared to the transmitted data was 2%. This further shows the suitability of the SPR for high data rate communication systems coupled with being multi-standard and highly reconfigurable. Table 3.3 below summarizes the result.

TABLE 3.3 Summary of performance LTE based communication system

SPECIFICATIONS	RESULT
Signal Bandwidth (MHz)	3
Peak-to-Average Power PAPR (dB)	8.7
RF Power (dBm)	15
LO Power (dBm)	8
EVM (%)	2.0
Non-linearity Order (N) Memory Depth (M)	N = 2; M = 4
Number of Calibration Coefficient	40

3.6 CONCLUSION

This chapter investigates the viability of a SPR front end in a WCDMA communication system with a multi-path fading channel. The BER profile for the communication system is plotted for four different cases. In the first case, the system is without a multipath channel effect and assumes a perfect receiver FE. In the second case, the system has a multipath channel effect and also assumes a perfect receiver FE. In the third and fourth cases, a multipath channel is considered along with an implemented SPR FE. In the third case, modified memory polynomial calibration technique is used, while in the fourth case, a less complex calibration technique using a direct linear estimation is adopted. A comparison between the four BER plots concludes that both calibration techniques are capable of providing very good BER performances, similar to the BER of an ideal receiver with multi-path channel fading. This proves the viability of the SPR front end in a WCDMA communication system. It is also safe to conclude that it is sufficient to use the least complex calibration technique in the case of a WCDMA communication system in a multi-path fading environment.

Chapter Four: **Concurrent Dual-band Six-Port Receiver for Multi-standard and Software Defined Radio Applications**

4.1 Introduction

The importance of multiband receiver architectures in communication systems has been discussed in chapter one of this thesis. The diverse range of modern wireless applications and services necessitates communication systems with more bandwidth and flexibility in order to maintain the plurality of the services. The concept of concurrent multiband operation in RF electronics has been introduced to improve the overall communication throughput in spectrum aggregation systems and in concurrent use of multiple communication services. The simplest of such multiband receiver front end is the concurrent dual-band receiver.

In this chapter we introduce a novel concurrent dual-band receiver architecture based on six-port concept. This receiver architecture uses only one six-port correlator circuit to downconvert two signals in two different bands concurrently. The receiver is reconfigurable over a broadband to simultaneously receive two different signals with same or different modulation techniques and bandwidths. The receiver is very flexible, hence availing itself for use in SDR applications. There are no limitations on the carrier frequencies of the two signals except that they have to be within the bandwidth of the six port receiver. The mathematical model for the receiver is derived and subsequently implemented to evaluate its performance. A suitable calibration technique was also developed to mitigate the receiver non-idealities.

4.2 Modern Dual-band Receivers Architectures

Modern dual-band receivers use the front-end stack-up technique. This architecture is achieved by building two individual receiving paths, one part for each signal to be received. This increases

cost, complexity, size and power consumption. Fig 4.1 below shows a schematic description of the front-end stack-up dual-band receiver.

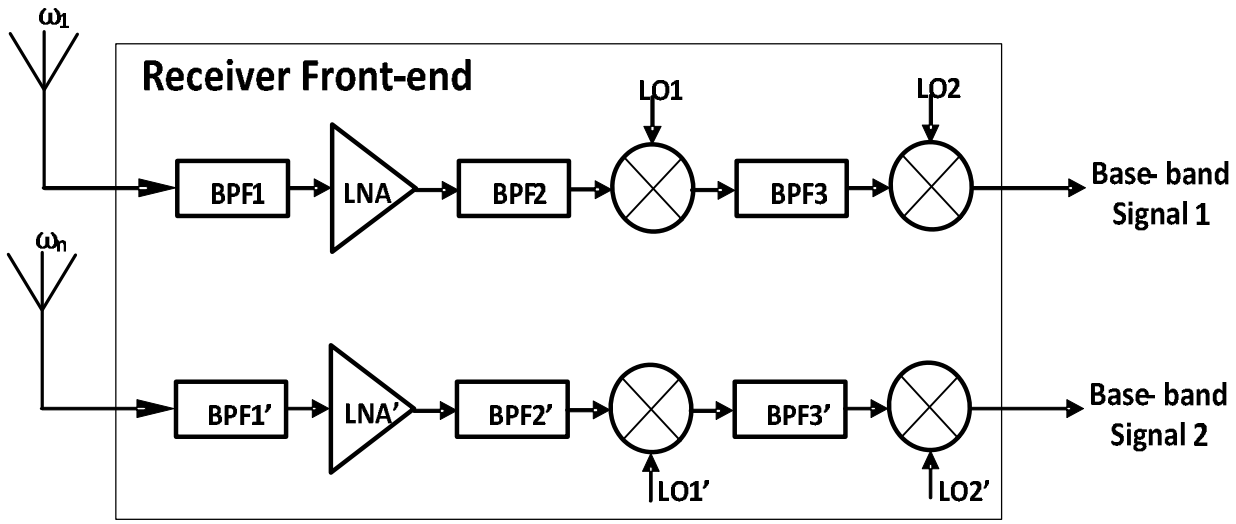


Figure 4.1: Front-end Stack-up concurrent dual-band receiver

The front-end stack-up architecture has very good performance because technically, it is two independent single-band receivers. It is however not the most efficient of techniques. Consequently, a lot of research has been done with the aim of reducing component duplications in the transition from single to concurrent dual-band operation. Fig. 4.2 shows the conceptual evolution of a dual-band receiver, starting with two totally independent heterodyne receiving paths, and leading to an efficient concurrent dual-band receiver.

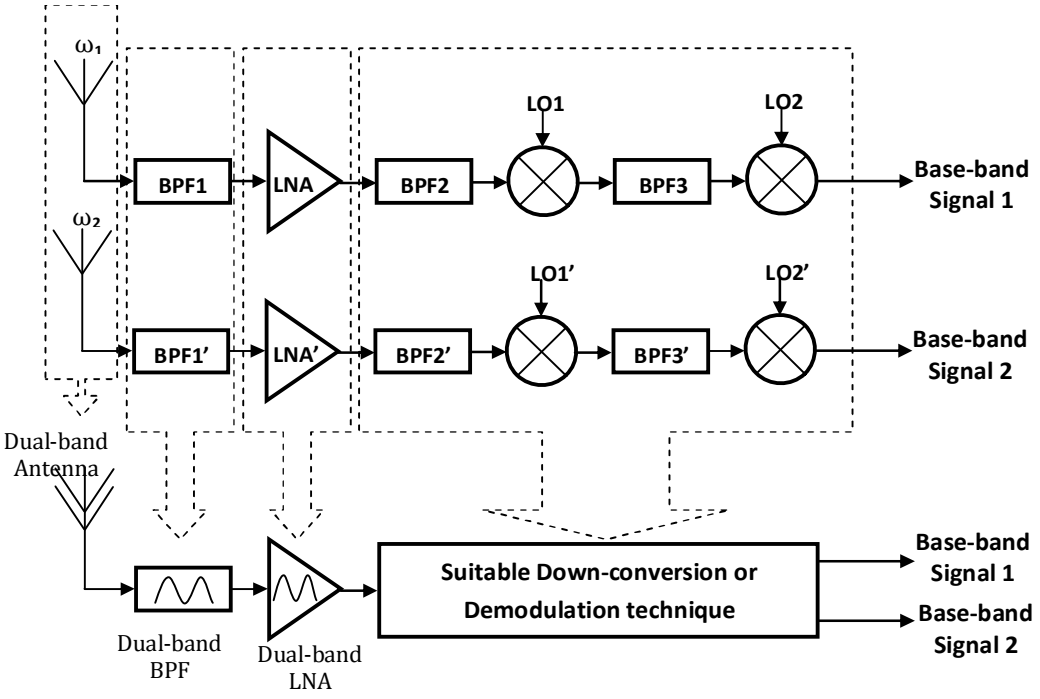


Figure 4.2 Evolution of dual-band receivers from single-band receivers.

There has been advancement in the design of dual-band antennas [30], dual-band filters [32] and low noise amplifiers (LNA) [29]. However, much of these solutions still have dual receiver paths at the final down-conversion/demodulation stage. [40], [41] present single path down-conversion stage for concurrent receivers, they however have fixed bands of operations, which limits their functionality for software defined radio (SDR) applications. RF Sub-sampling technique has been shown to avoid the duplication of the final down-conversion stage [42]-[45]. This technique however has some drawbacks. Typical design challenges associated with the RF sub-sampling receiver include the track and hold noise effects, aliasing and aperture jitter noise generated from the sampling clock phase noise [42]. These issues reduce the sensitivity and dynamic range of the receiver. Peculiar to the concurrent dual band mode, the analog-to-digital converters (ADCs) used in the RF subsampling architecture must cover the spectral range of the RF signals. This is

challenging because the maximum achievable analog frequency of the ADC is limited by its aperture jitter. The power dissipation of the architecture is also high due to the increased bandwidth when a dual-band signal is to be received [40].

In this chapter, a new receiver architecture based on the six-port demodulation technique is proposed and implemented in the context of concurrent dual-band and multi-standard applications. The receiver is reconfigurable over a broadband with no constraints on the carrier frequencies of the two signals. The only condition on the two signals is that they have to be within the bandwidth of the passive six-port circuit of the receiver architecture, which can be designed to be very broadband. Hence the receiver is highly reconfigurable, tunable and multi-standard.

4.3 Concurrent Dual-band and multi-standard SPR

Fig. 4.4 shows the architecture for the proposed concurrent dual-band and multi-standard SPR. Similar to the single-band SPR, at the heart of the receiver is a six-port wave-correlator circuit and four power detectors at ports 3 through 6. Port 2 is the input port for the dual-band RF signal (RF1 and RF2) and port 1 is the input port for two local oscillator (LO) signals (LO1 and LO2) used in the proposed receiver system. The two LO signals are combined using a microwave combiner (C) and fed to the LO port as shown in Fig. 4.4. Fig. 4.5 is a blown out schematic of the functional blocks of the DSP block depicted in Fig. 4.4. By carefully assigning the two local oscillator frequencies, RF1 and RF2 can be received and their respective baseband components (I_1,Q_1) and (I_2,Q_2) recovered.

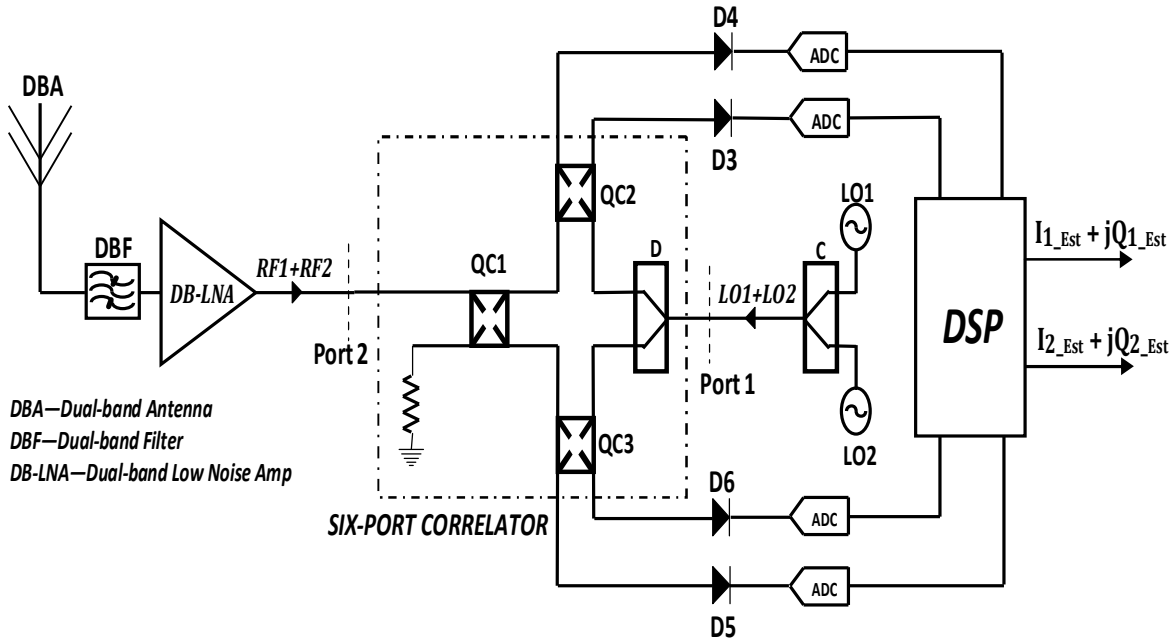


Figure 4.4 Concurrent dual-band six-port receiver architecture.

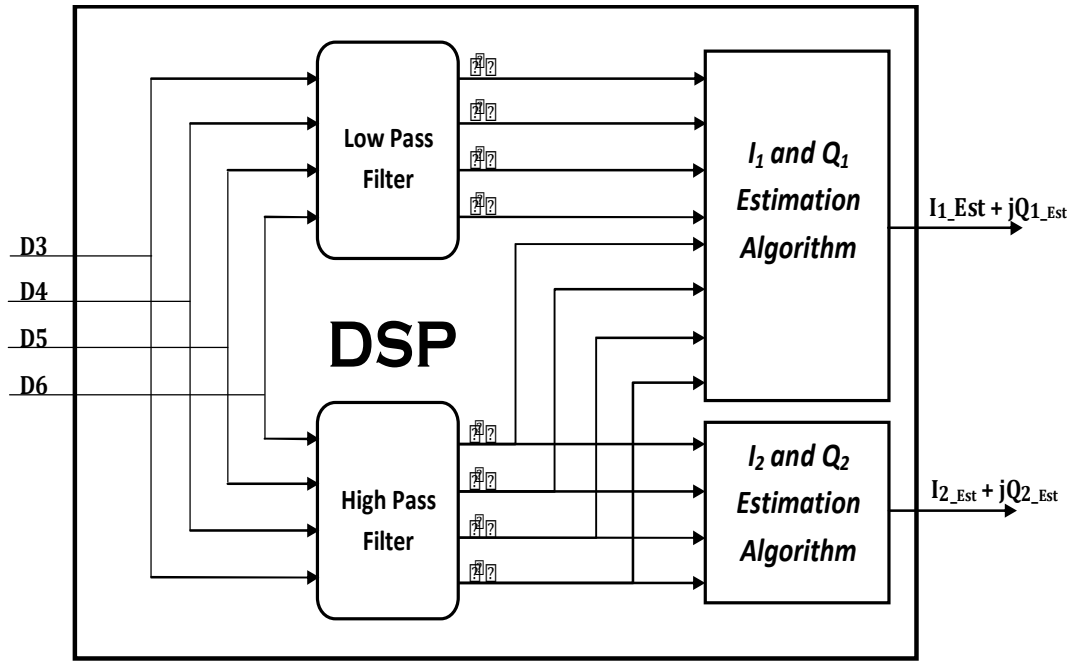


Figure 4.5. Schematic diagram of the DSP block of proposed dual-band architecture.

This can be achieved by imposing the following conditions on the LO signals:

$$f_{LO1} = f_{RF2}$$

$$f_{IF} = f_{LO2} - f_{RF1} > \frac{BW_{RF1} + BW_{RF2}}{2}$$

where f_{RF1} is the carrier frequency of RF1, f_{LO1} is the LO1 frequency, f_{RF2} is the carrier frequency of RF2, f_{LO2} is LO2 frequency and BW_{RF1}, BW_{RF2} are the signal bandwidths of RF1 and RF2 respectively. As an illustration, Fig. 4.6 shows two signals A and B at RF frequencies f_{RF1} and f_{RF2}. To enable the concurrent DB SPR operation, an overlap of the two frequency bands of the diode output at baseband must be prevented.

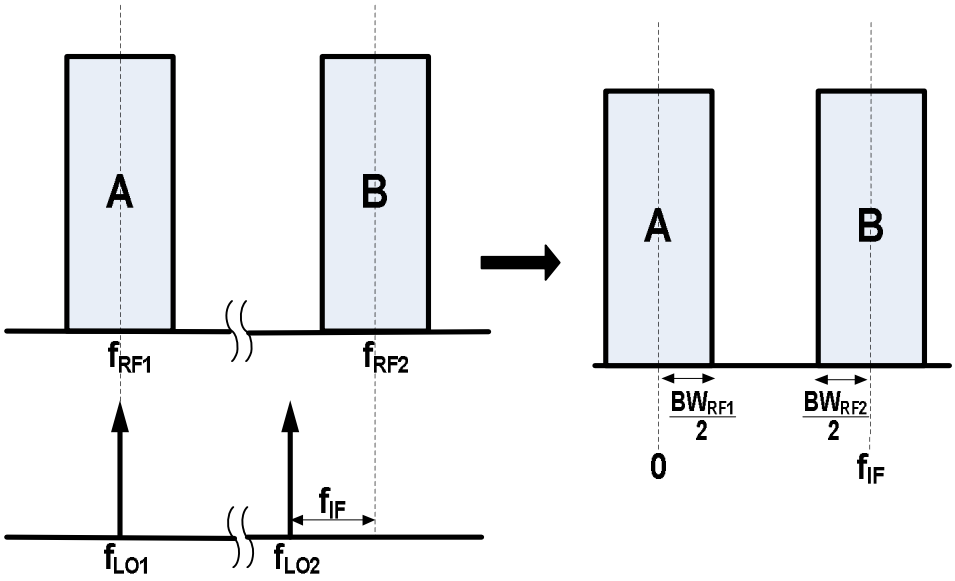


Figure 4.6 Illustration of the LO frequency selection of proposed dual-band SPR

It is worth noting that, in order to prevent ambiguity, the second LO signal (LO2) with frequency (f_{LO2}) is subsequently referenced as LO3 with frequency f_{LO3}, to highlight that it is not equal to the carrier frequency of RF2.

Defining the following as phasor representation of the microwave signals at the SPR RF and LO ports,

$$a_{RF} = \frac{1}{\sqrt{2}}|a_{RF}|e^{j\omega_{RF}t+\phi_{RF}}$$

$$a_{LO} = \frac{1}{\sqrt{2}}|a_{LO}|e^{j\omega_{LO}t+\phi_{LO}}$$

$$a_{3} = \frac{1}{\sqrt{2}}|a_{3}|e^{j\omega_{3}t+\phi_{3}}$$

$$a_{4} = \frac{1}{\sqrt{2}}|a_{4}|I_{4} + Q_{4}e^{j\omega_{4}t+\phi_{4}}$$

$$S_{21} = |S_{21}|e^{j\phi_{21}}; \qquad S_{31} = |S_{31}|e^{j\phi_{31}}$$

the power (Pi) detected by the power detectors is given by

$$P_i = |S_{2i}a_{RF} + a_{LO}| + S_{3i}a_{3} + a_{4}|^2 \text{ for } i = 3,4,\ldots 6 \qquad (4.1)$$

Power difference between two different output ports of the SPR can be written as in equations (4.2) and (4.4). The calculation details are provided in the appendix.

$$P_5 - P_6 = \alpha_{11}I_4 - [\alpha_{12} + \alpha_{13}Q_4 + \alpha_{14}(1 + \alpha_{15}\sin(\Delta\omega t_{43})I_4 - \alpha_{16}(1 + \alpha_{17}\cos(\Delta\omega t_{43})Q_4 \qquad (4.2)$$

$$P_7 - P_8 = [\alpha_{18} + \alpha_{19}I_4 + \alpha_{20}Q_4 + \alpha_{21}(1 + \alpha_{22}\sin(\Delta\omega t_{43})I_4 + \alpha_{23}(1 + \alpha_{24}\cos(\Delta\omega t_{43})Q_4 \qquad (4.3)$$

where α_{25} are constants and $\Delta\omega t_{43} = \omega_4 t - \omega_3 t$

Equations (4.2) and (4.3) show that the output of the diode will have two frequency bands, the first at baseband and the second centered at (f_{RF2} – f_{RF1}).

For convenience, subsequent reference to the high pass component of the diode output is represented with a bar over the signal name, for example $\overline{P_2 - P_1}$, while the low pass component is represented with a bar under the signal name, for example $\underline{P_2 - P_1}$. The high pass components of (4.2) and (4.3) are given by:

$$\overline{P_2 - P_1} = \alpha_{RF2}\alpha_{RF1}\sin(\Delta\omega t_{RF2})\, I_2 - \alpha_{RF2}\alpha_{RF1}\cos(\Delta\omega t_{RF2})\, Q_2 \qquad (4.4)$$

$$\overline{P_2 - P_1} = \alpha_{RF2}\alpha_{RF1}\sin(\Delta\omega t_{RF2})\, I_2 + \alpha_{RF2}\alpha_{RF1}\cos(\Delta\omega t_{RF2})\, Q_2 \qquad (4.5)$$

From (4.4) and (4.5), it can be deduced that the high pass components are the data of (I_2, Q_2) at a frequency $\Delta\omega t_{RF2}$. Hence, by down-converting to baseband, expressions (4.4) and (4.5) become;

$$\overline{P_2 - P_1} = \alpha_{RF2}\alpha_{RF1} I_2 - \alpha_{RF2}\alpha_{RF1} Q_2 \qquad (4.6)$$

$$\overline{P_2 - P_1} = \alpha_{RF2}\alpha_{RF1} I_2 + \alpha_{RF2}\alpha_{RF1} Q_2 \qquad (4.7)$$

(4.6) and (4.7) can be expressed in linear relationship of the high-pass components of the four diode power measurement as in equations (4.8) and (4.9) below.

$$I_2 = a_{11}\overline{P_1} + a_{12}\overline{P_2} + a_{13}\overline{P_3} + a_{14}\overline{P_4} \qquad (4.8)$$

$$Q_2 = a_{21}\overline{P_1} + a_{22}\overline{P_2} + a_{23}\overline{P_3} + a_{24}\overline{P_4} \qquad (4.9)$$

where a_{ij} are constants. Ideally, a_{ij} should be equal to ±1. However, due to the non-idealities in the SPR circuit, these constants may have different values and should be estimated in the calibration process.

The matrix representation of (4.8) and (4.9) is

$$\begin{bmatrix} I_2 \\ Q_2 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \end{bmatrix} \begin{bmatrix} \overline{P_1} \\ \overline{P_2} \\ \overline{P_3} \\ \overline{P_4} \end{bmatrix} \quad (4.10)$$

where a_{ij} is a matrix of the calibration constants for I_2 and Q_2 demodulation of the receiver. These constants can be determined using an appropriate calibration technique, which will be discussed in the next section.

The low pass components of (4.2) and (4.3) can be obtained as follows:

$$\underline{P_1 - P_2} = \alpha_{11} I_2 - \alpha_{12} + \alpha_{12} Q_2 + \alpha_{11} I_2 - \alpha_{12} Q_2 \quad (4.11)$$

$$\underline{(P_1 - P_2)} = \alpha_{12} + \alpha_{11} I_2 + \alpha_{12} Q_2 + \alpha_{11} I_2 + \alpha_{12} Q_2 \quad (4.12)$$

Substituting the expression for I2 and Q2 from (4.8) and (4.9) into the low pass equations, (4.11) and (4.12) resolves to;

$$\underline{P_1 - P_2} = \alpha_{11} I_2 - \alpha_{12} + \alpha_{12} Q_2 + \alpha_{11} a_{11} \overline{P_1} + a_{12} \overline{P_2} + a_{13} \overline{P_3} + a_{14} \overline{P_4} - \alpha_{12} a_{11} \overline{P_1} + a_{12} \overline{P_2} + a_{13} \overline{P_3} + a_{14} \overline{P_4} \quad (4.13)$$

$$\underline{P_1 - P_2} = \alpha_{12} + \alpha_{11} I_2 + \alpha_{12} Q_2 + \alpha_{11} a_{11} \overline{P_1} + a_{12} \overline{P_2} + a_{13} \overline{P_3} + a_{14} \overline{P_4} + \alpha_{12} a_{11} \overline{P_1} + a_{12} \overline{P_2} + a_{13} \overline{P_3} + a_{14} \overline{P_4} \quad (4.14)$$

This is also a two equation system with two unknowns. It can be expressed in linear relationship of the four diode outputs (low-pass and high-pass component) as;

$$I_2 = b_{11} \underline{P_1} + b_{12} \underline{P_2} + b_{13} \underline{P_3} + b_{14} \underline{P_4} + b_{11} \overline{P_1} + b_{12} \overline{P_2} + b_{13} \overline{P_3} + b_{14} \overline{P_4} \quad (4.15)$$

$$Q_2 = b_{21} \underline{P_1} + b_{22} \underline{P_2} + b_{23} \underline{P_3} + b_{24} \underline{P_4} + b_{21} \overline{P_1} + b_{22} \overline{P_2} + b_{23} \overline{P_3} + b_{24} \overline{P_4} \quad (4.16)$$

and subsequently in a matrix form as

$$\begin{bmatrix} I_1 \\ Q_1 \end{bmatrix} = \begin{bmatrix} b_{11} & b_{12} & b_{13} & b_{14} & b_{15} & b_{16} & b_{17} & b_{18} \\ b_{21} & b_{22} & b_{23} & b_{24} & b_{25} & b_{26} & b_{27} & b_{28} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_1^2 \\ P_2^2 \\ P_3^2 \\ P_4^2 \end{bmatrix} \tag{4.17}$$

where b_{ij} are the calibration constants for I_1 and Q_1 of the receiver. This is also determined using an appropriate calibration technique.

4.4 Receiver Calibration

The calibration procedure for the SPR involves the calculation of the constants that will be used to retrieve the I/Q information contained in the RF signal from the four diode detector output powers. An efficient calibration procedure must be able to compensate for any shift from the ideal SPR system. State of the art techniques use a training sequence to determine these calibration constants. It has been discusses that a diode power detector has a memory effect response when a complex modulated signal passes through it due to its frequency response. Of all the calibration techniques reported in literature, a black box model calibration proposed by Hasan et al [19] has the best performance. As discussed in chapter two of this thesis, the technique models the imperfections of the six-port correlator and nonlinearity of the diode in one step using a modified memory polynomial. An inverse model of the memory polynomial is used to linearize the system (correlator and diode). Using this reverse model, the I/Q information

contained in the RF signal is estimated directly from the output voltage measurement of the diodes.

The diode output voltages and the estimated (I/Q) information are related by;

$$I + jQ_{pqd}(n) = \sum_{p=1}^{M}\sum_{q=0}^{N}\sum_{d=0}^{1} A_{pqd}\, v_d^{p}(n-q) \qquad (4.18)$$

where A_{pqd} is the complex predetermined calibration constants from a training signal. M is the memory depth and N is the nonlinearity order of the modified memory polynomial for the nth symbol. The error vector magnitude (EVM) of the received signal as compared to the transmitted signal is used as the metric to measure the performance of the calibration technique. Given (R) number of transmitted symbols (S_{TMT}) and estimated symbols (S_{EST}), the EVM is given by;

$$EVM(\%) = \sqrt{\frac{\frac{1}{R}\sum_{n=1}^{R}|S_{EST} - S_{TMT}|^2}{\frac{1}{R}\sum_{n=1}^{R}|S_{TMT}|^2}} * 100 \qquad (4.19)$$

The above described calibration technique is employed in this work. A modified memory polynomial is used to estimate the I/Q information from the dual-band signal. The high-pass and low-pass component of the diode output are used in the modified memory polynomial expression for the (I_1, Q_1) estimation while (I_2,Q_2) uses only the high-pass component of the diode output. Equations (4.20) and (4.21) are the models defined for the estimation of the I-Q information contained in RF1 and RF2 respectively.

$$I_1 + jQ_1{}_{pqd}(n) = \sum_{p=1}^{M}\sum_{q=0}^{N}\sum_{d=0}^{1} A_{pqd}\underline{V}_d^{p}(n-q) + B_{pqd}\underline{V}_d^{p}(n-q) \qquad (4.20)$$

$$I_d + jQ_d = \sum_{p=0}^{P}\sum_{q=0}^{Q}\sum_{d=0}^{D} C_{pqd}\, V_2^p(n-q)\, V_3^d(n-q) \qquad (4.21)$$

where A_{pqd}, B_{pqd} and C_{pqd} are the calibration constants, which are obtained by using known training signals.

4.5 Concurrent Dual-Band and Multi-Standard SPR Implementation

Concurrent dual band and multi-standard SPR test-bench is implemented as depicted in Fig. 4.7. The six-port wave correlator is configured using three quadrature couplers (Q1-Q3) and a Wilkinson combiner (C). The two baseband I/Q data are generated and raised cosine filtered using MATLAB. The filtered baseband data are up-converted separately using two synchronized signal generators (E4438C ESG from Agilent Inc.) and combined using a combiner (2090-6304-00 from M/A-COM Inc.). The two LOs are generated using two signal Generators (E8247C from Agilent Technologies) and also combined using a power combiner (M/A-COM 2090-6304-00). The LO and RF generators are trigged synchronously. The output voltages generated by the Schottky diodes are captured and digitized using two synchronized dual-channeled VSAs (89600 series VSA from Agilent Technologies). The concurrent dual-band and multi-standard SPR demodulation model defined by expressions (4.20) and (4.21) are carried out using MATLAB to retrieve the I-Q information in both RF signals.

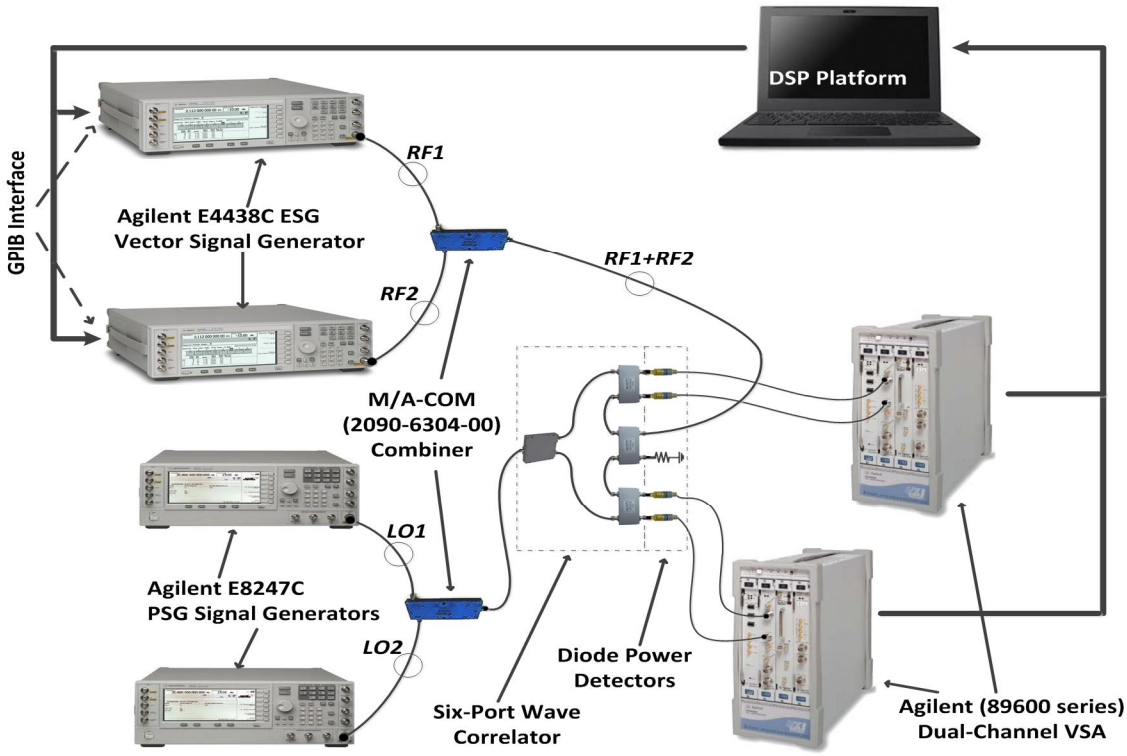


Figure 4.7 Test bench set-up for the concurrent dual-band SPR.

4.6 Measurement Results

To validate and evaluate the performance of the proposed model, two signals were generated and sent into the setup as described in Section IV. A 16-QAM signal at 3.0 GHz (RF1) and a 64-QAM signal at 2.5 GHz (RF2) combined to simulate a dual-band real RF signal. Signals with different modulation are used to test the robustness of the receiver. Both RF signals have 20,000 I/Q data points each at a data rate of 2 MSamples/s. The symbols are filtered with a raised cosine filter having 0.3 roll-off factor and up-sampled by a factor of 8. The frequency of the first local oscillator (LO1) is 3 GHz, which is same as the carrier frequency of RF1. The second local oscillator (LO2) is 2,492 MHz, which is an offset of 8 MHz from RF2 carrier frequency. The

power of the signals of the two LOs is set to 3 dBm while that of RF1 and RF2 is 0 dBm. 0 dBm RF power was used for experimental purpose because of the loss in the assembled passive wave correlator and the sensitivity of the diode detectors used. In real application, a low loss wave correlator will be designed and envelope detectors with good sensitivity will relax the requirement on the LNA.

Fig. 4.8 shows the spectrum of the signal at the output of the diodes. There are two bands, one at baseband and the other centered at 8 MHz which is the frequency offset of LO2 from RF2. This spectrum plot validates the equations (4.2) and (4.3).

The first 2500 corresponding symbols from RF1 and RF2 are used as the training packet to calibrate the receiver and estimate calibration constants. These constants are used to estimate the received signal as defined in (4.20) an (4.21). Fig. 4.9 shows the plots for the 16-QAM (RF1) transmitted and received signals. It can be concluded that the received and transmitted data are quasi identical. Fig. 4.10 shows the constellation plot and frequency spectrum of the transmitted and received data for the 64-QAM (RF2) signal and the corresponding frequency spectrum.

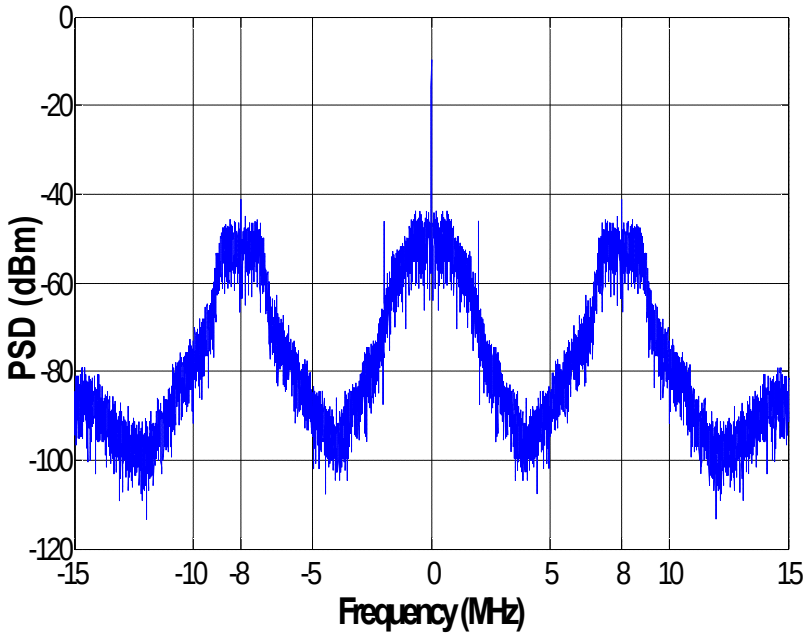
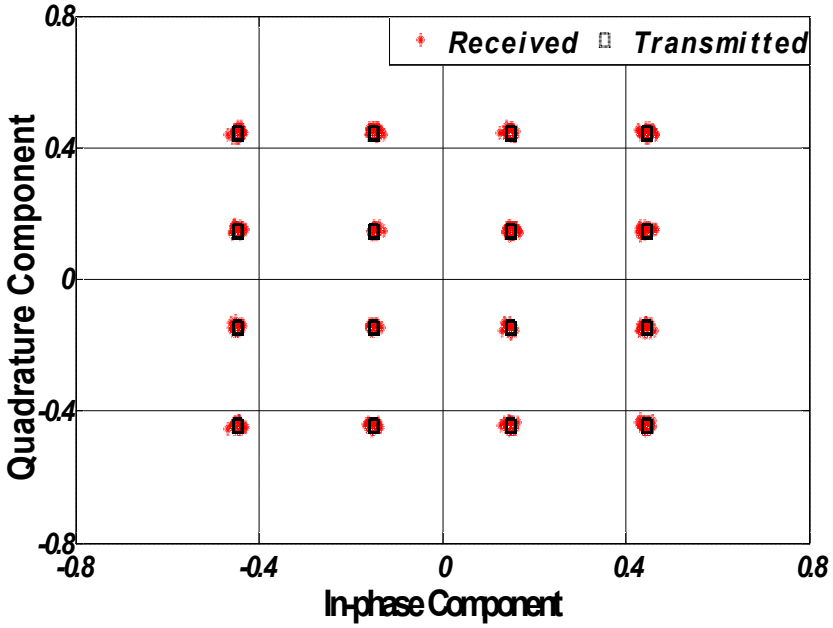
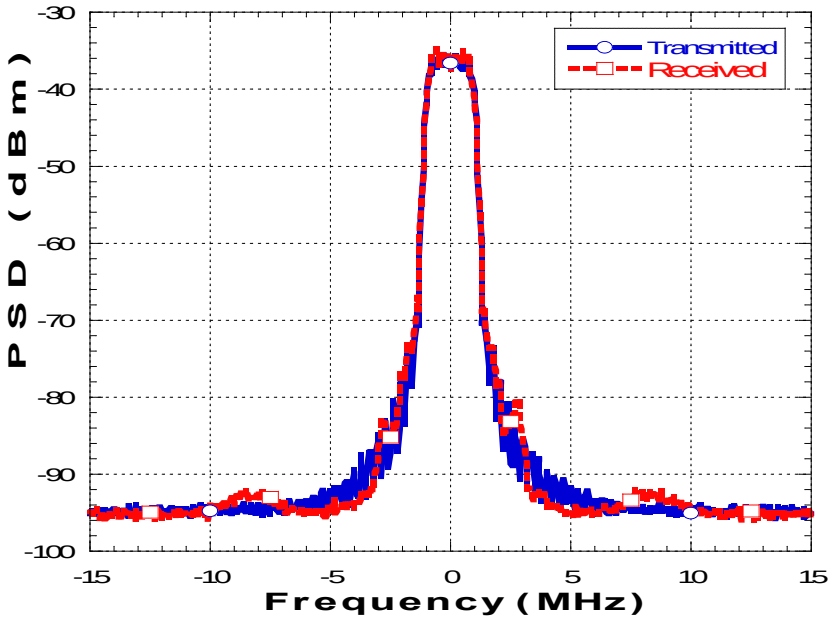


Figure 4.8 Diode Output Frequency Spectrum.



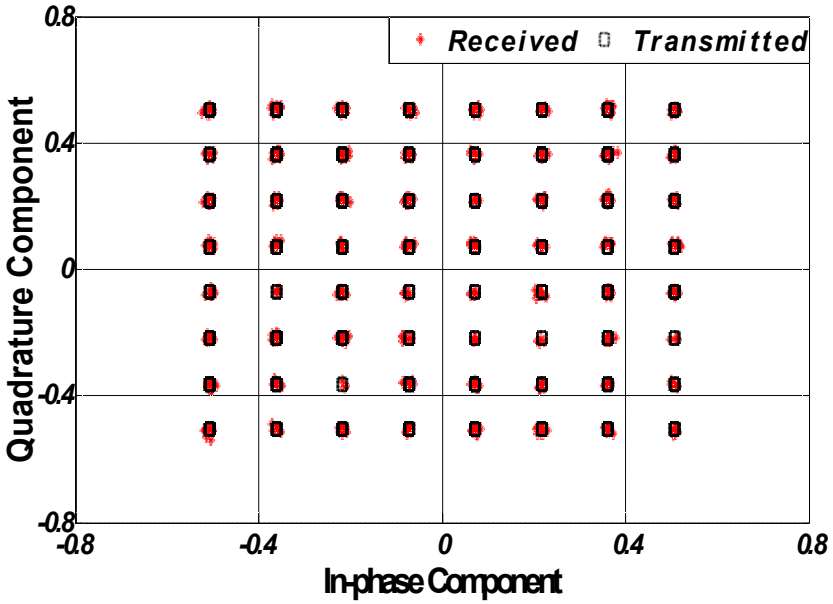
(a)



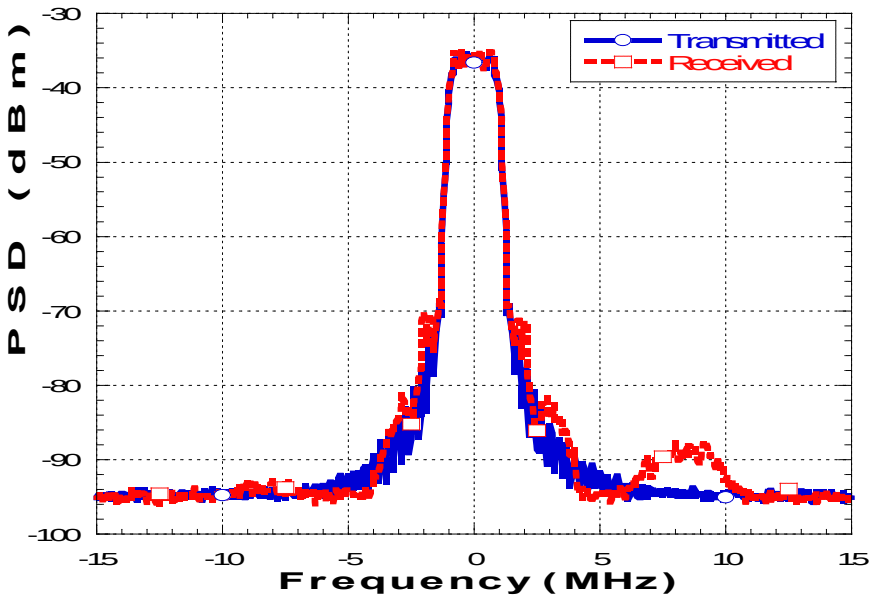
(b)

Figure 4.9 Window of 16QAM Transmit and Received Signal (a) Constellation Plot;

(b) Frequency Spectrum.



(a)



(b)

Figure 4.10 64QAM Transmitted and Received Signals (a) Constellation Plot; (b) Frequency Spectrum

It is seen from fig. 4.8 that the diode output has LO leakage. This is due to the lack of good isolation between the RF and LO ports in the six port circuit. This leakage affects the dynamic range of the system. Its effect is reduced by pushing the power detectors to their nonlinear region and by compensating for the leakage in the calibration algorithm. By pushing the power detector to the nonlinear region, nonlinear distortion appears in the signal generating spectral regrowth and signal quality degradation, hence the need for a suitable calibration technique that is able to compensate for these imperfections. To quantitatively evaluate the performance of the model of the receiver, the EVM is calculated from the measured data using (4.19).

Using a direct linear combination of the diode outputs, the resulting EVMs of the received signals are 19.6% for the 64QAM signal and 19.4% for the 16QAM signal. Using the modified memory polynomial calibration technique, the resulting EVMs are 1.9% for the 64QAM signal and 1.8% for the 16QAM signals. This shows the importance and performance of the developed calibration method. The results are summarized in Table 4.1.

TABLE 4.1: Summary of performance for the demodulation process of 64 QAM and 16 QAM signal

Specifications	RF1 (64-QAM)	RF2 (16-QAM)
Signal Bandwidth (MHz)	2	2
Peak-to-Average Power PAPR (dB)	9.5	9.5
RF Frequency (GHz)	2.5	3.0
LO Frequency (MHz)	2 492	3000
EVM (%)	1.9	1.8
Non-linearity Order (N) Memory Depth (M)	N = 2; M = 3	N = 2; M = 3
Number of Calibration Coefficient	32	64

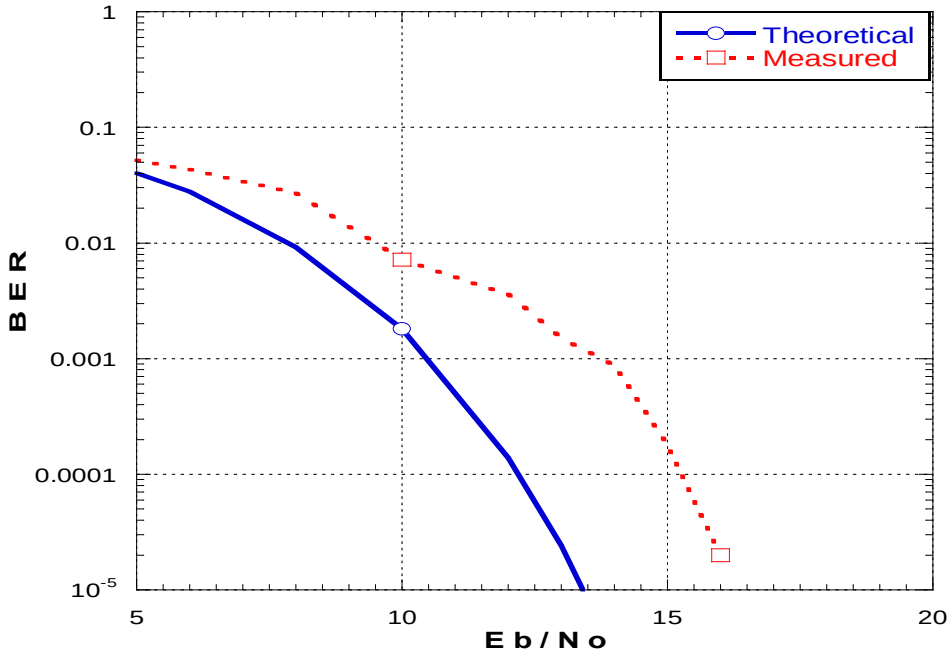


Figure 4.11 BER plot for 16 QAM at 2Mbps.

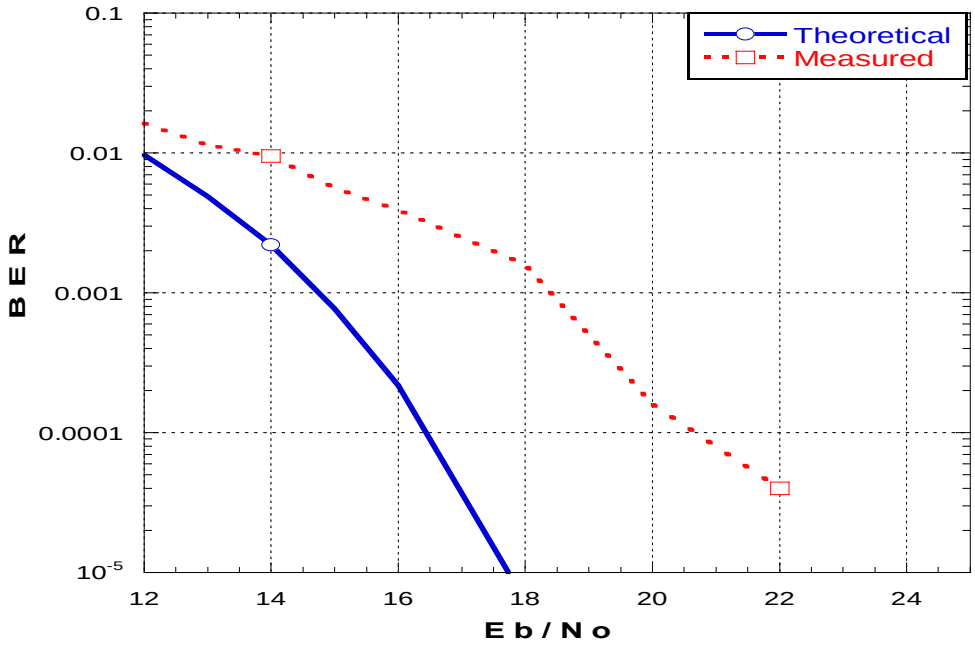


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Figure 4.12 BER plot for 64 QAM at 2Mbps.

Fig. 4.11 shows the BER plot of the 16-QAM signal while fig. 4.12 shows the BER plot for the 64-QAM signal, when both signals are received concurrently at 2Mbps data rate.

A co-existence signal interference test was also carried out. Two signals with 20dBc power difference between both bands are received. In the first case, a 64QAM signal at 0dBm and a 16QAM at -20dBm are received. The resulting EVMs are 1.4% for the 64QAM signal and 5.6% for the weaker 16QAM signal. The second case has the 64QAM at -20dBm and the 16QAM at 0dBm. The resulting EVMs are 4.4% for the 64QAM signal and 1.2% for the 16QAM signal. The EVMs for the signals at lower power level (-20dBm) is a bit degraded when compared with when the signals are of equal power levels. It will be ideal to have the weaker signal amplified to the same power level as the stronger signal prior to down-conversion to optimize the performance of the receiver.

TABLE 4.2: Summary of performance for the demodulation process of a WCDMA and LTE signal

Specifications	RF1 (WCDMA)	RF2 (LTE)
Signal Bandwidth (MHz)	3.84	3
Peak-to-Average Power PAPR (dB)	8.6	8.7
RF Frequency (GHz)	2.5	3.0
LO Frequency (MHz)	2 492	3 000
EVM (%)	1.9	2.0
Non-linearity Order (N) Memory Depth (M)	N = 2; M =3	N = 2; M = 3
Number of Calibration Coefficient	32	64

Table 4.2 shows the result of concurrent multi-standard SPR receiving a WCDMA and a LTE signals. Excellent linearity is observed in the concurrent multi-standard mode of operation. Indeed, the measured EVM is equal to 1.9% and 2.0% for the WCDMA and LTE signals, respectively. Fig. 4.13 shows the transmitted and received signal spectrums of the WCDMA signal while Fig. 4.14 shows the spectrums for the LTE signal. The modified memory polynomial is very effective at modeling the diode detector nonlinearity to give a very good receiver performance but from both figures, it can be seen that there is residual nonlinearity in the received signal which is due to the diode detector nonlinearity.

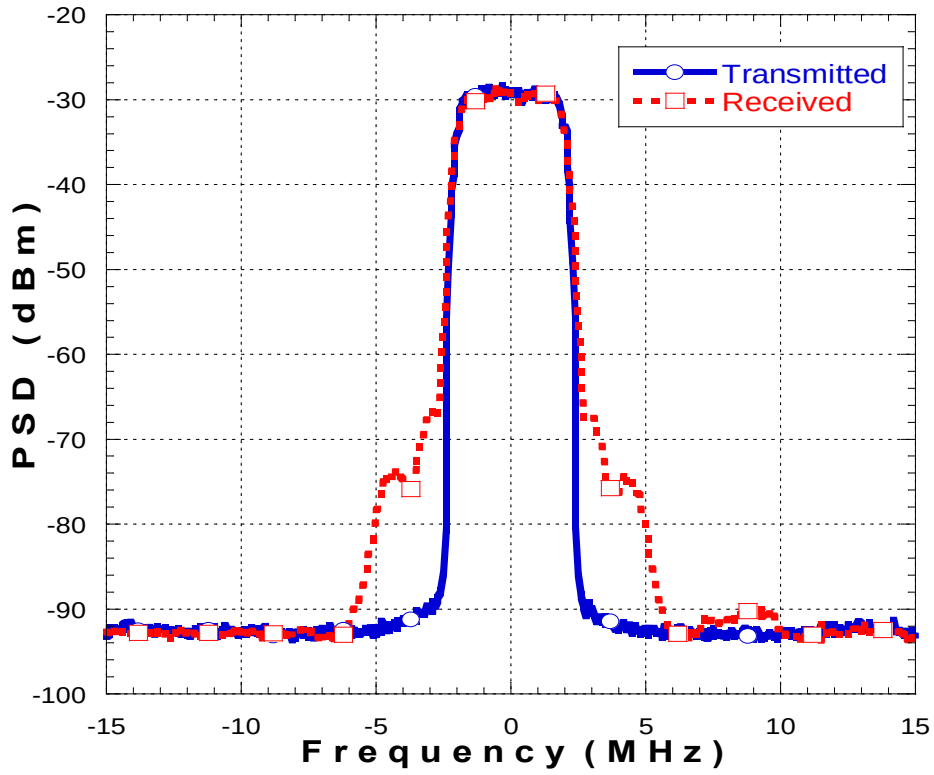

Figure 4.13 WCDMA Transmit and Received Signal Frequency Spectrum

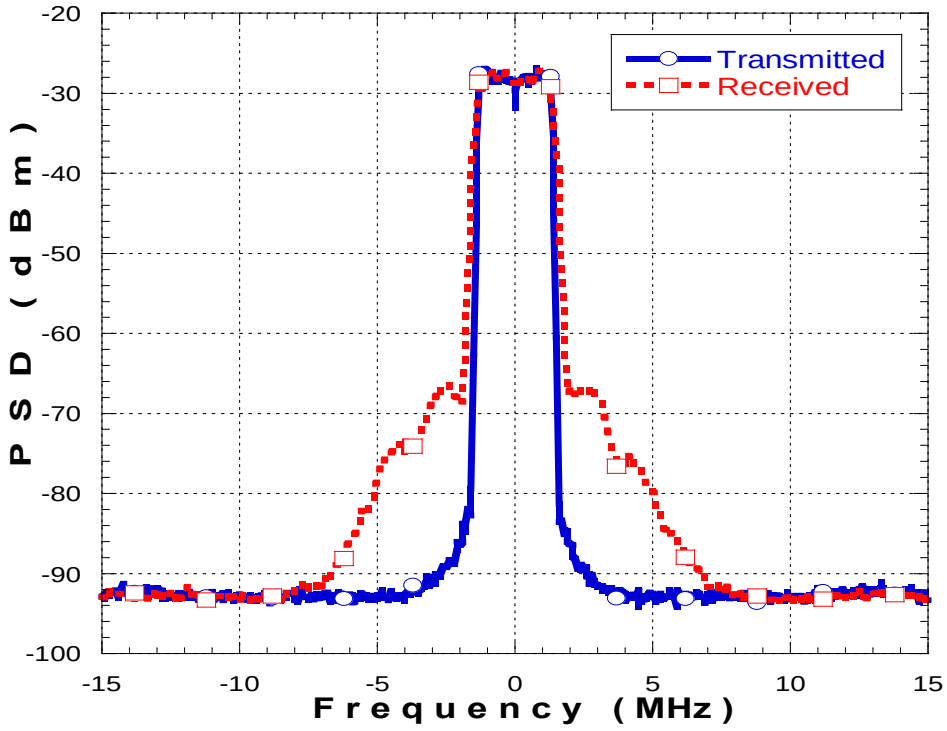

Figure 4.14 LTE Transmit and Received Frequency Signal Spectrum

4.7 Conclusion

In this chapter, a novel concurrent dual-band and multi-standard receiver using the six-port technique was introduced. The receiver was modeled mathematically and then validated with measurement. The receiver has the same hardware requirement as the single band SPR thereby avoiding hardware duplication which is peculiar to the state of the art concurrent dual-band receivers. An appropriate calibration technique was also developed to mitigate the receiver non-idealities and improve performance. It was used to concurrently receive a dual-band signal at different carrier frequencies (2.5 GHz and 3 GHz) using two different modulation techniques; 64QAM and 16QAM. Validation using two different real communication signals (WCDMA and LTE) was also carried out. Performance was evaluated using the EVM of the received data as

compared with the transmitted data. The estimated EVMs for the 64QAM/16QAM signal pair were 1.9% for the 64QAM signal and 1.8% for the 16QAM while those for the WCDMA/LTE pair were 1.9% for WCDMA and 2.0% for LTE. The proposed concurrent dual-band and multi-standard SPR showed excellent linearity performance while requiring few calibration parameters. Overall, 96 complex parameters to compensate for all types of distortion in the multi-standard RF front-end.

Chapter Five: **Conclusion**

5.1 Research Summary

This thesis establishes the importance of a typical software defined radio (SDR) as a solution to the continuous proliferation of wireless communication standards and protocols. The challenges to the design of such ideal SDR was discussed thus leading to modern architectures used in proxy of the ideal SDR. These modern architectures in light of their advantages and drawbacks were discussed as regards SDR applications and the homodyne receiver was identified to be most flexible and viable substitute for an ideal SDR. Furthermore, the idea of concurrent dual band receivers have been introduced to increase data rate and avail users of real time simultaneous use of more than one wireless application.

The six-port receiver (SPR) which is an alternative to the conventional homodyne receiver is explored in this work as a SDR enabling receiver architecture. The structure of the SPR comprises a core passive six-port wave correlator circuit and four envelope power detectors (typically diode power detectors). The transmitted I/Q data is recovered from a linear combination of the diode detector output voltages. The SPR structure is inherently broadband. This makes it flexible and multiband. The SPR receiver is also multi-standard because much of the signal processing is done at baseband (bb). The drawback in the SPR is due to the non-linearity, frequency response and the limited dynamic range of the diode detectors coupled with the non-idealities in the ideal power and phase relationships of the wave correlator circuit. These drawbacks degrade the performance of the receiver. Consequently, suitable calibration techniques to mitigate this structural weakness have been described. Part of the work done in this thesis is to investigate the performance of a SPR front-end (FE) in a WCDMA downlink communication system. Two calibration techniques were used. The first one involves the direct

combination of the diode detector output. In the second case, a block box model which uses a modified memory polynomial is used. In both cases, known training signals are sent and received and using a least square method, the calibration constants are estimated. These calibration constants are hence used to receive the remaining transmitted data. A BER profile of the communication system was plotted and the result shows a quasi-identical performance with a perfect receiver in both cases.

Typical architectures for concurrent dual-band receiver use the front-end stack-up technique, whereby two individual receiver paths are designed with each receiver path dedicated to a different communication standard and protocol. This is not very efficient as it increases the size, complexity, power requirement and cost of the receiver. The increased size also affects integration of the receivers in IC units. In this thesis we have developed a novel SPR model which uses the same FE architecture as in the single band case, thus avoiding any component duplication in the frequency downconversion path. The difference between the single band SPR and the concurrent dual-band SPR is in the final signal processing stage to estimate the transmitted I/Q data. By analytically selecting the frequency of the two LO signals sent into the SPR, the diode power output has two bands, a baseband and an IF component. A linear combination of the filtered IF band of the diode output is used to estimate the transmitted data I_1/Q_1 in the first signal (RF_1) while a linear combination of both filtered baseband and IF component of the diode output is used to estimate the transmitted data I_2/Q_2 in the second signal (RF_2). A new black box calibration technique using a modified memory polynomial model was developed for the receiver to mitigate non-idealities and improve receiver performance.

The concurrent dual-band SPR was implemented and used to concurrently receive two RF signals, a 64QAM and 16QAM signal, both at 2Mbps data rate. Using the direct linear

combination of the diode outputs, the resulting EVMs of the received signals are 19.6% for the 64QAM signal and 19.4% for the 16QAM signal. Using the modified memory polynomial calibration technique, the resulting EVMs are 1.9% for the 64QAM signal and 1.9% for the 16QAM signals. This shows the importance and performance of the developed calibration method.

To show the viability of the receiver for real communication signals, a WCDMA and LTE were also received concurrently. A BER profile was plotted for both the 64QAM/16QAM pair. The resulting BER plot shows a good result. Table 5.1 and 5.2 below gives a summary of the receiver performance for the 64QAM/16QAM and WCDMA/LTE pair respectively.

TABLE 5.1: Summary of performance for the demodulation process of 64 QAM and 16 QAM signal

Specifications	RF1 (64-QAM)	RF2 (16-QAM)
Signal Bandwidth (MHz)	2	2
Peak-to-Average Power PAPR (dB)	9.5	9.5
RF Frequency (GHz)	2.5	3.0
LO Frequency (MHz)	2 492	3000
EVM (%)	1.9	1.8
Non-linearity Order (N) Memory Depth (M)	N = 2; M = 3	N = 2; M = 3
Number of Calibration Coefficient	32	64

TABLE 5.2: Summary of performance for the demodulation process of a WCDMA and LTE signal

Specifications	RF1 (WCDMA)	RF2 (LTE)
Signal Bandwidth (MHz)	3.84	3
Peak-to-Average Power PAPR (dB)	8.6	8.7
RF Frequency (GHz)	2.5	3.0
LO Frequency (MHz)	2 492	3 000
EVM (%)	1.9	2.0
Non-linearity Order (N) Memory Depth (M)	N = 2; M =3	N = 2; M = 3
Number of Calibration Coefficient	32	64

5.2 Comparison between the Concurrent Dual-band SPR and State-of -the-art receivers

The state-of-the-art concurrent dual band receiver uses the front-end stack-up technique which increases complexity, size, power requirement and cost. The new concurrent dual-band SPR uses a single receiver path to receive two signals concurrently. The SPR typically has low power requirement, this results in a more power efficient receiver architecture. State-of-the-art receivers have excellent performance particularly when they are designed with the SHR architecture. They are however less reconfigurable and not flexible because of the accompanying web of filters which help reduce interference, leakages and other sources of distortion. The attempt at using a single mixer based architecture reported in [35] for a concurrent reception of signals in three bands for spectrum aggregation resulted in performance which was degraded by intermodulation and spurious output from the mixer. The concurrent dual-band SPR on the other hand is very flexible and reconfigurable with a very good performance as has been shown in the results

presented. This lends them very suitable for SDR applications. The main contributions of this thesis work can be summarized in the following bullets.

- The suitability of the SPR technique for high data rate communication systems like the 3G and 4G systems was shown even in a multipath fading channel.
- A new concurrent dual-band SPR was developed suitable for software defined radio (SDR) applications.
- A suitable calibration technique was developed for the dual-band SPR to mitigate the nonlinearity, low dynamic rate, LO leakage, DC offset and all other imperfections which will otherwise adversely affect the performance of the receiver.

5.3 Future Works

Research activities that can be undertaken as an extension to the work done in this thesis can be summarized in the following paragraphs.

Efforts can be made at developing an effective calibration technique that optimizes either the linearity or the complexity of the calibration technique in terms of reducing the number of calibration constants and providing a simpler parameter estimation algorithm. This will ease the requirement on the DSP section of the SPR receiver thus saving power and processing time.

The SPR test setup used in this work comprises of off-the-shelf components. This assembly covers a frequency range of 2 GHz to 12 GHz. The wave correlator circuit which is an assembly of three quadrature hybrid couplers and a divider is bulky. The diode power detectors used are finger sized. This makes the SPR assembly quite large. It would be an area of interest to design a miniaturized integration of the wave correlator circuit, envelope power detector in suitable

technologies such as LTCC, or MMIC for example or any other suitable technology to minimize the footprint and size. Further to this, designing a complete receiver architecture which includes the antenna, LNA, filters, frequency synthesizers and a back end DSP section should be explored to proffer a unit IC receiver solution. By completing the design of the full receiver, evaluating the receiver sensitivity, dynamic range and linearity will be possible. Moreover, studying the effect of strong interferers on the receiver performance will be an interesting area to investigate once a complete concurrent dual-band receiver is built.

One of the advantages of the six-port technique is that it can be designed to be very broadband. The set up used in this thesis covered a frequency range of 2 GHz to 12 GHz. Hence, exploring a similar model for a concurrent multiband receiver with three bands or more without duplicating any component in receiver path will be interesting.

Appendix

In what follows from (4.3) in chapter four, simplification and derivation of the diode output difference equation is as follows:

$$P_i = |S_{i1}a_{LO} + a_{RF1}| + S_{i2}a_{LO} + a_{RF2}| \quad \text{for } i = 3,4,\ldots 6 \tag{A.1}$$

Equation (A.1) can be expanded as in (A.2).

$$\begin{aligned} P_i = {} & |S_{i1}|^2|a_{LO}|^2 + |a_{LO}|^2\cos\Delta\omega t_{13} \\ & + |S_{i1}|^2\left[\tfrac{1}{2}|a_{RF1}|^2 B_1{}^2 + |a_{RF1}||a_{RF2}|B_1B_2\cos(\omega_1 t - \omega_2 t + \phi_{RF1} - \phi_{RF2})\right. \\ & \left. + \tfrac{1}{2}|a_{RF2}|^2 B_2{}^2\right] + K_1\left[\cos(\phi_{si2} - \phi_{si1} + \Delta\omega t_{13} - \phi_{LO}) + \cos(\phi_{si2} - \phi_{si1} - \phi_{LO})\right]I_1 \\ & + K_1\left[\sin(\phi_{si2} - \phi_{si1} + \Delta\omega t_{13} - \phi_{LO}) + \sin(\phi_{si2} - \phi_{si1} - \phi_{LO})\right]Q_1 \\ & + K_2\left[\cos(\phi_{si2} - \phi_{si1} + \Delta\omega t_{21} - \phi_{LO}) + \cos(\phi_{si2} - \phi_{si1} + \Delta\omega t_{23} - \phi_{LO})\right]I_2 \\ & + K_2\left[\sin(\phi_{si2} - \phi_{si1} + \Delta\omega t_{21} - \phi_{LO})\right. \\ & \left. + \sin(\phi_{si2} - \phi_{si1} + \Delta\omega t_{23} - \phi_{LO})\right]Q_2 \end{aligned} \tag{A.2}$$

Where

$$B_1 = \sqrt{I_1^2 + Q_1^2}; \quad B_2 = \sqrt{I_2^2 + Q_2^2},$$

$\Delta\omega t_{13} = \omega_1 t - \omega_3 t$; $\Delta\omega t_{21} = \omega_2 t - \omega_1 t$;

$\Delta\omega t_{23} = \omega_2 t - \omega_3 t$

$|a_{RF1}| = |a_{RF2}| = |a_{LO}|$, $\phi_{RF1} = \phi_{RF2} = \phi_{LO}$

$K_1 = |S_{i1}||S_{i2}||a_{LO}||a_{RF1}|$; $K_2 = |S_{i1}||S_{i2}||a_{LO}||a_{RF2}|$

$\Delta\omega t_{RF1}$ and $\Delta\omega t_{RF2}$ components in the diode output expression are high frequency components

at RF which appear as constant envelope signals at the diode output.

Similar to the single-band SPR, the following conditions are required to enable the down-conversion of the baseband I/Q data in the proposed receiver.

While the conditions on the wave correlator are:

1) $|S_{\square\square}| = |S_{\square\square}|$ and $|S_{\square\square}| = |S_{\square\square}|$
2) $|S_{\square\square}| = |S_{\square\square}|$ and $|S_{\square\square}| = |S_{\square\square}|$
3) $\angle S_{\square\square} = \angle S_{\square\square} + 90°$ and $\angle S_{\square\square} = \angle S_{\square\square} + 90°$
4) $\angle S_{\square\square} = \angle S_{\square\square} + 90°$ and $\angle S_{\square\square} = \angle S_{\square\square} + 90°$
5) $\angle S_{\square\square} - \angle S_{\square\square} - \emptyset_{\square\square} = 2n\pi,\ n = 0,1,2 \ldots,$
6) $\angle S_{\square\square} - \angle S_{\square\square} - \emptyset_{\square\square} = (2n + \frac{\square}{\square})\pi,\ n = 0,1,2 \ldots,$

The condition on the diode detectors is such that they operate within their square law region ($P_{\square} = K_{\square}V_{\square}, k = 3,4..6$) at all times and have identical response, i.e. $K_{\square}$ is the same for k = 3,4, ... 6.

Hence, considering an ideal six port junction where $|S_{\square\square}| = \square S_{\square\square}\square$ and $|S_{\square\square}| = \square S_{\square\square}\square$ as proposed in the six port design, the difference in power between any two diode outputs is given by

$$
\begin{aligned}
\square P_{\square} - P_{\square}\square = & -2K_{\square}\sin\left(\frac{\square_{\square}}{\square}\right)\square\sin\left(\frac{\theta_{\square} + 2\Delta\omega t_{\square\square}}{2}\right) + \sin\left(\frac{\theta_{\square}}{2}\right)\square\square I_{\square} \\
& + 2K_{\square}\sin\left(\frac{\square_{\square}}{\square}\right)\square\cos\left(\frac{\theta_{\square} + 2\Delta\omega t_{\square\square}}{2}\right) + \cos\left(\frac{\theta_{\square}}{2}\right)\square\square Q_{\square} \\
& - 2K_{\square}\sin\left(\frac{\square_{\square}}{\square}\right)\square\sin\left(\frac{\theta_{\square} + 2\Delta\omega t_{\square\square}}{2}\right) + \sin\left(\frac{\theta_{\square} + 2\Delta\omega t_{\square\square}}{2}\right)\square\square I_{\square} \\
& + 2K_{\square}\sin\left(\frac{\square_{\square}}{\square}\right)\square\cos\left(\frac{\theta_{\square} + 2\Delta\omega t_{\square\square}}{2}\right) + \cos\left(\frac{\theta_{\square} + 2\Delta\omega t_{\square\square}}{2}\right)\square\square Q_{\square} \qquad (A.3)
\end{aligned}
$$

where

$\theta_{\square} = \square\emptyset_{\square\square} - \emptyset_{\square\square} - \emptyset_{\square\square} + \emptyset_{\square\square}\square$

$\theta_{\square} = \square\emptyset_{\square\square} - \emptyset_{\square\square} + \emptyset_{\square\square} - \emptyset_{\square\square} - 2\emptyset_{\square\square}\square.$

Fulfilling the above specified conditions for an ideal six port junction, the power difference equations for the different diodes can be reduced to the following;

$$[P_2 - P_1] = 2K_2 \sin(\Delta\omega t_{12})\, I_2 - 2K_2[\cos(\Delta\omega t_{12}) + 1]Q_2 + 2K_2[\sin(\Delta\omega t_{12}) + \sin(\Delta\omega t_{12})]I_2 - 2K_2[\cos(\Delta\omega t_{12}) + \cos(\Delta\omega t_{12})]Q_2 \quad (A.4)$$

$$[P_2 - P_1] = 2K_2[\sin(\Delta\omega t_{12}) + 1]I_2 + 2K_2 \cos(\Delta\omega t_{12})\, Q_2 + 2K_2[\sin(\Delta\omega t_{12}) + \sin(\Delta\omega t_{12})]I_2 + 2K_2[\cos(\Delta\omega t_{12}) + \cos(\Delta\omega t_{12})]Q_2 \quad (A.5)$$

As discussed, $\Delta\omega t_{12}$ and $\Delta\omega t_{12}$ are at RF and appear at the diode output as constant envelope signals. Hence, the respective equivalent expressions for (A.4) and (A.5) are

$$[P_2 - P_1] = \alpha_{12} I_2 - [\alpha_{12} + \alpha_{12}]Q_2 + \alpha_{12}[1 + \alpha_{12} \sin(\Delta\omega t_{12})]I_2 - \alpha_{12}[1 + \alpha_{12} \cos(\Delta\omega t_{12})]Q_2 \quad (A.6)$$

$$[P_2 - P_1] = [\alpha_{12} + \alpha_{12}]I_2 + \alpha_{12}Q_2 + \alpha_{12}[1 + \alpha_{12} \sin(\Delta\omega t_{12})]I_2 + \alpha_{12}[1 + \alpha_{12} \cos(\Delta\omega t_{12})]Q_2 \quad (A.7)$$

Expressions (A.6) and (A.7) are referenced as (4.4) and (4.5) in chapter 5.

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