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Design of a CMOS Standard Cell Library

by

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ABSTRACT

To facilitate rapid design of digital integrated systems a double-level-metal, CMOS standard cell library has been developed. Some of the more important library features include longevity and vendor and process independence. Fifty-four general purpose cells have been generated, software verified, and characterized through simulation. The physical and electrical characteristics of this library have been found to be comparable or superior to those of libraries currently offered by vendors.

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FOREWORD

This thesis presumes that the reader is familiar with CMOS processing technology and hopes that the reader has also had some exposure to the concept of standard cells. In the event that some background reading is required for CMOS processing, any good text such as [44] or [17] is recommended.

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Chapter 1

Introduction

1.1 Motivation

In the generation of application specific integrated circuits, standard cell libraries are emerging as the premier design form as they serve as a good compromise in the silicon efficiency - design time efficiency dichotomy. Design forms employing a higher degree of regularity such as the gate array or PLA may be composed and fabricated faster but are wasteful in area. At the other end of the spectrum, higher levels of integration such as macrosystems and full custom design, though highly silicon efficient, are prone to layout errors, are difficult to revise, and require much more time to complete.

In addition, standard cell libraries are becoming easier to develop and use because of the support they are receiving from computer-aided engineering (CAE) environments. Verification aids, schematic capture, place and route tools, and precise simulations all promote rapid and accurate system integration.

An examination of process and fabrication technology suggests CMOS for many reasons. Unlike other technologies it is conceptually clean; in digital circuits, output values actually attain rail voltages and there is little static power dissipation. Other digital features include good output swing and noise margins and high speed.

For analog circuits, CMOS exhibits high input impedance, no inherent offset voltages for switches, high-quality capacitors, and good gain and linearity. Generally, it offers good density and drive capability, and supports a wide range of supply voltages. Overall, CMOS boasts excellent digital and good analog behaviour.

In spite of all the advantages a CMOS standard cell library would seem to possess, many are still designed with extrinsic deficiencies like process dependence, vendor dependence, and lack of longevity. Each of these problems is addressed in turn.

Process dependence is encountered when a library is composed with only one CMOS process variant in mind. Of the bulk CMOS processes (P-, N-, and twin-well) none appears to dominate characteristically. This comment has been raised by several authors such as Gulett [1], Young [2], Batra et al. [3], and Wollensen et al. [4]. It is commonly agreed that P-well technology has a proven reliability record, reduced alpha-particle sensitivity, closer matched p- and n-channel devices, and high gain NPN structures. N-well proponents acknowledge better compatibility and performance with NMOS processing and designs, good substrate quality, availability, and cost, lower junction capacitance, and reduced body effects. Issues such as which variant is the least susceptible to latch-up are still heavily debated. CMOS processes that avoid the problem of latch-up altogether include those employing dielectric isolation (SOI, SOS, trenched CMOS) and three-dimensional versions described by Kawamura et al. [5] and Hoefflinger et al. [6]. Clearly, with the attributes that each

process has to offer designs should attempt to accommodate as many processes as possible.

Vendor dependence is suffered when designs are tailored to the design rules of one vendor; designs are rendered incompatible with all vendors' processes except one. In the event that a vendor is unable to meet commitments or perhaps for economic reasons, vendor independence or generic design appears as an obvious asset. Still there are documented cases in which this feature has been overlooked [7, 8, 9, 10, 11, 12, 13].

With the rapid and frequent advances in fabrication technology, it is often the case that by the time a library is designed, characterized, and used in the development of a product, the process is antiquated. This is especially true when referring to minimum feature size. Sources pertaining to scalable or lambda-based design rules [14, 15, 16, 17] propose a solution to this problem.

The aim of this thesis is to demonstrate that it is possible to develop a CMOS standard cell library free of such deficiencies. This is not truly unique as similar works have been noted. Lincoln [18] developed a library that is both vendor and process independent and Schediwy [19] has recently produced a scalable, vendor and process independent library. Our efforts follow the format of Lincoln more closely as Schediwy has introduced additional problems by subscribing to the *grounded-substrate* convention (see Chapter 2). A good substrate convention in

concert with sound design techniques and an integrated CAE environment has helped produce a powerful standard cell library.

1.2 Objectives

Specifically, the task at hand is the development of a CMOS standard cell library with the following features.

- process independence : supports N-, P-, and twin-well CMOS
- vendor independence or generic design
- scalability

For simulation purposes and to provide a starting point, several vendors' processes utilizing a second level of metal and two micron gates were initially investigated. Although this technology is not leading-edge, it is supported by most fabrication houses [20] and is mature enough to be used with confidence [21, 22]. Also, use of two micron technology conveniently facilitates transcription or comparison with lambda-based design rules.

Other salient library features proposed include the following operational specifications.

- digital in nature
- *15 MHz* operation given *4* asynchronous devices between synchronous ones and with each device supporting a full load (defined to be a fanout of *4*)

Although the library is designed for the implementation of digital systems, possible expansion and inclusion of analog cells has not been excluded.

The thesis follows a logical progression. Chapter 2 concentrates on the selection of a suitable standard cell methodology and design strategy. Chapter 3 then describes the design environment as it pertains to library development and reviews the latch-up phenomenon. Chapter 4 contains the entire development procedure from generation of the design rules through layout, verification, and design considerations. Chapter 5 provides a comparison of the library to other libraries currently offered by vendors. Finally, Chapter 6 establishes conclusions.

Chapter 2

Standard Cell Methodology and Design Strategy

2.1 Introduction

Libraries of standard cells are used to assemble integrated systems by means of a *design strategy*. Since standard cells may be treated as functional blocks, design strategies are usually straight forward and entail the tiling and interconnection of individual cells. Cells are tiled into rows to ease the task of power distribution, and cell interconnections, or *routing*, tend to occur in *channels* between cell rows. To aid comprehension, the entire procedure may be likened to the breadboarding of TTL components. In addition, assuming that individual cells are correctly designed, the final product can virtually be assured of being *correct by construction*. A typical *floorplan* will prove to be some variant of Figure 2.1.

To readily facilitate tessellation a certain degree of regularity must be ingrained in every cell. It is this regularity that promotes rapid design. And if followed to its logical conclusion, design regularity enables systems to be designed via automated means such as schematic capture, place and route programs, or silicon compilation.

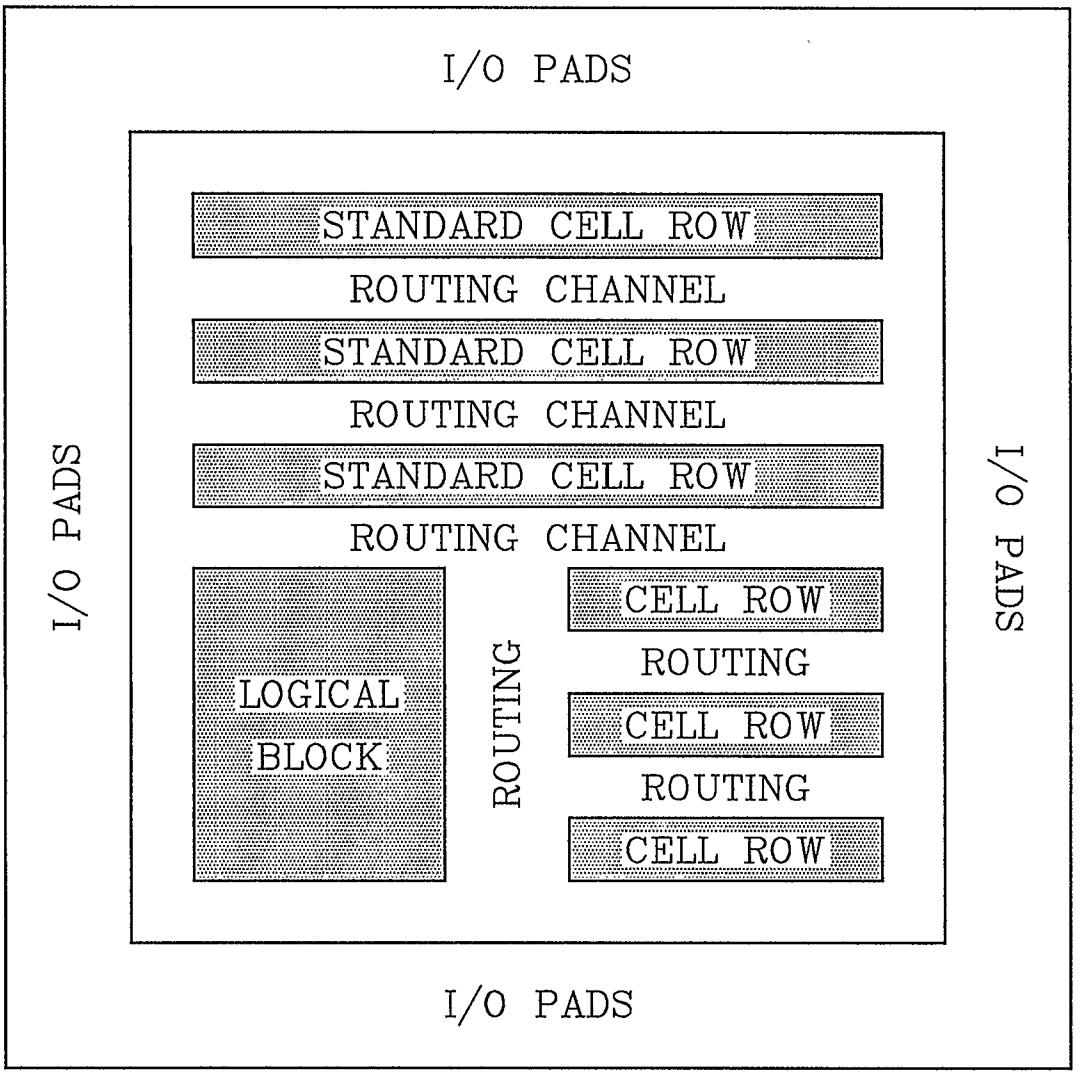


Figure 2.1: Typical floorplan

A *standard cell methodology* is a set of design constraints imposed on every cell in a library to support the design strategy. This term is somewhat ambiguous though as the methodology can also be considered to encompass behavioural issues such as design for testability [23] and structural issues such as process independence [18, 19]. In any event the methodology will always include a regular set of rules defining how and where all cell I/O (including supply rails) are to be placed. As standard cells come in different flavours, this chapter presents from literature three sample standard cell methodologies and their respective design strategies and then describes and justifies the methodology and strategy selected for our library.

2.2 Published methodologies and design strategies

Setting aside behavioural issues for the moment, there are several generalizations that can be drawn regarding most standard cell methodologies.

Standard cell dimensions

Standard cells are rectangular and have either variable width, variable height, or both for all cells in a library.

Supply rails

Supply rails are established using metal to minimize resistive effects. First-level metal is normally used because, unlike second-level metal, it is free to connect

directly to all other layers and, given process topology, can be more reliable than second-level metal. To facilitate rail extension, as cells are placed adjacent to one another, rails must be oriented parallel to one another and, for any given row, be separated by a fixed distance. Consequently, some methodologies group the supply rails while others choose to part them.

I/O lines

I/O lines cross cell boundaries orthogonally and may be restricted to one, two, three, or all cell faces depending on the design strategy. In addition, I/O lines are usually run in polysilicon or second-level metal so they may be easily routed over the power supply rails.

Routing

Routing is performed using the supply rail layer and an I/O layer. Typically, a routing line is viewed in a *manhattan* sense or as being comprised of several sections orthogonal to the design axes. To avoid operational design violations, portions of the routing line parallel to the supply rails are run in the supply rail layer and remaining portions are run in the I/O layer.

Substrate convention

For CMOS circuits there is a need to select the substrate convention. This may involve the use of N-, P-, twin-, or in the case of the grounded-substrate convention, D-wells.

2.2.1 Sample methodology 1

The first methodology and strategy to be discussed were described by Hortensius et al. [24] (refer to Figure 2.2). As shown in the design strategy, cells have both variable width and height. The supply rails are grouped and this feature has been taken advantage of as adjacent rows are mirrored and overlapped to maintain a common ground line thereby reducing area requirements. I/O lines are available in polysilicon at the top of the cell for routing but additional lines may be run between adjacent cells when constructing large functional blocks. P-well CMOS has been selected as the substrate convention.

As an aside, it should be mentioned that Figure 2.2 is not drawn to scale but is only intended to show the relative locations of cell features and the basics of the design strategy. The same holds true for all other sample methodologies and design strategies in this chapter.

2.2.2 Sample methodology 2

The second methodology and strategy to be discussed were recently described by Schediwy [19] (refer to Figure 2.3). Here, cells are assigned fixed height and variable width. Supply rails are grouped as in the previous methodology but adjacent rows do not share a common rail. I/O are available in first-level metal and polysilicon over the cell perimeter and, process permitting, provision can be made for routing with second-level metal. As with the previous methodology, preferred

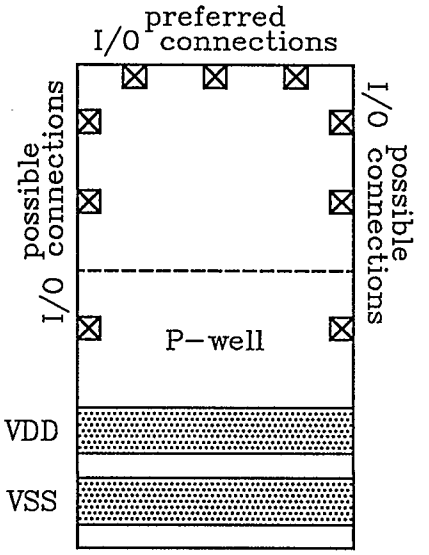


Figure 2.2a: Sample standard cell methodology 1

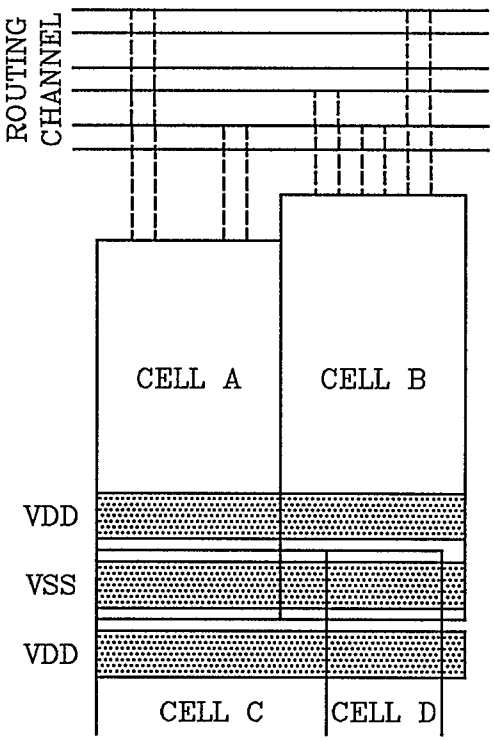


Figure 2.2b: Sample design strategy 1

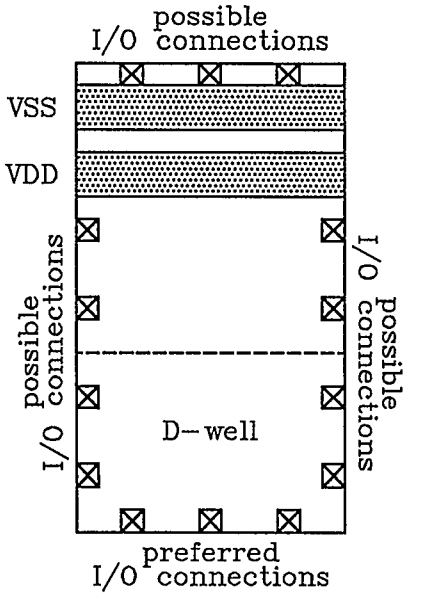


Figure 2.3a: Sample standard cell methodology 2

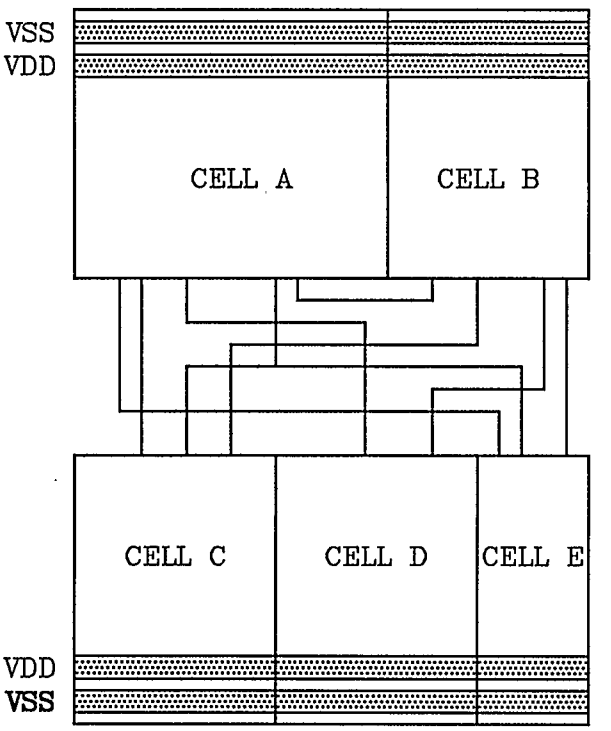


Figure 2.3b: Sample design strategy 2

routing connections are made on the cell face furthest from the supply rails to limit switching noise. To facilitate process independence, the grounded-substrate convention has been employed. In the grounded-substrate convention a single layer (D-well) is designated as a well. This layer then becomes either an N-well or P-well depending on the target process. Consequently, transistors may become either n-channel or p-channel. Also, to reflect a change in process, supply rails and all I/O must change polarity to maintain consistent logical operation.

2.2.3 Sample methodology 3

The third and final sample strategy and methodology are in fact conglomerates compiled from several sources such as Feller et al. [12], Kang [25], Lincoln [18], and Martinez et al. [13] (refer to Figure 2.4). With this methodology supply rails are separated and placed at or near opposing cell boundaries. All sources propose cells with variable width and all show fixed height except [12]. Instead, to ensure that supply rails align properly, [12] suggests enforcing a fixed height for each cell row. All sources have I/O available at both the cell top and bottom and all support I/O in either polysilicon or second-level metal. Substrate convention varies dramatically as [25] uses P-well CMOS, [13] uses N-well CMOS, [12] uses SOS CMOS, and [18] includes both N- and P-wells to enable process independence.

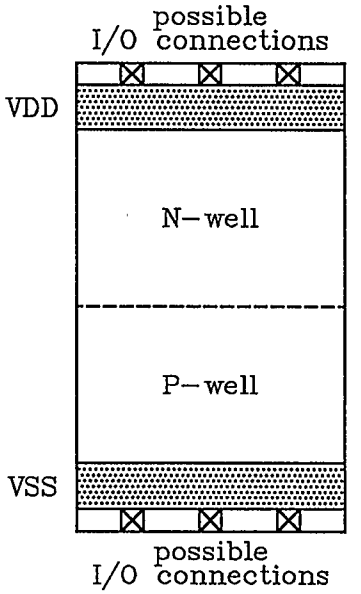


Figure 2.4a: Sample standard cell methodology 3

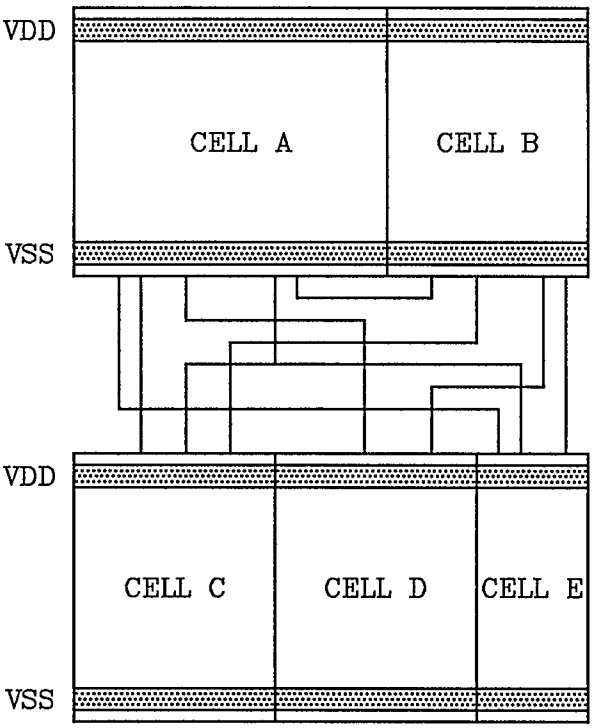


Figure 2.4b: Sample design strategy 3

2.3 Selected standard cell methodology and design strategy

The standard cell methodology and design strategy adopted for our library is similar to that depicted in Figure 2.4. To promote cell abutment, cells are assigned a fixed height and variable width. Supply rails have a fixed width and are placed along opposing cell boundaries. This technique, of course, implies that all cell I/O must cross the supply rails. And although routing over the rails inherently contributes to switching noise, it also alleviates internal routing complexity for large cells. In addition, separating the rails circumvents problems such as having to wire one rail over the other (as in the case of grouped rails at one end of the cell) or having to run internal lines over both rails (as in the case of grouped rails at the centre of the cell).

I/O are available in second-level metal at both the cell top and bottom. Second-level metal is utilized to enhance library speed while I/O availability at both ends of the cell can ease routing congestion. Many methodologies do not condone the use of second-level metal within a cell. Rather, they prefer to have the capability to rout second-level metal over any cell or connect to cells of interest at will. Such an approach though fails to recognize the undesirable topologies that can result from this. Also, if analog cells are involved, the uncontrolled routing of second-level metal can have an adverse effect. For instance, running a clock line in second-level metal directly over analog devices may introduce a substantial amount of noise and may potentially corrupt cell functionality. Our approach merely ensures

step coverage rules, via design rules, and operational integrity are maintained. As a compromise, to reduce routing complexity second-level metal feedthroughs are included in designs wherever possible. Finally as with most libraries, possible I/O locations are constrained to a rectangular grid the spacing along which is known as the *pitch*.

As with [18], to realize process independence, both an N- and P-well are included in layout. Then prior to fabrication, software can remove any undesired mask. To avoid design rule violations between adjacent cells, both wells have a fixed height. This approach has three distinct advantages over the grounded-substrate convention:

- In the grounded-substrate convention, transistors may be either n- or p-channel depending on the process. Thus, cells optimized for one process may perform poorly in another.
- Supply rails and all I/O change polarity in the grounded-substrate convention in response to a changing process. Therefore, integrated circuits fabricated in different processes defy *plug-compatibility*.
- Finally, the grounded-substrate convention is incapable of supporting a twin-well process as only one well is defined.

By no means should the reader infer that the grounded-substrate convention is without merit. To the contrary, it is a powerful conceptual tool. And in his work

Schediwy unconditionally demonstrates that the convention is both feasible and practical. However, some issues - particularly plug-compatibility - have swayed us from subscription.

The actual methodology is shown in Figure 2.5. Note that all dimensions are in lambda and are qualified through calculation in chapter 4. As the target environment of any given cell is unknown, every cell should be able to *stand alone.* Since we are using bulk CMOS processes, this implies that to prevent latch-up every cell must contain substrate contacts; split contacts are not used. Regarding the design strategy and tessellation guidelines, a regular I/O grid may be easily realized if each cell is designed as in Figures 2.6a and 2.6b. However, to get maximum use of cell area while still adhering to stand alone design, our cells are designed as in Figures 2.6c and 2.6d. Greater elaboration is afforded in chapter 4.

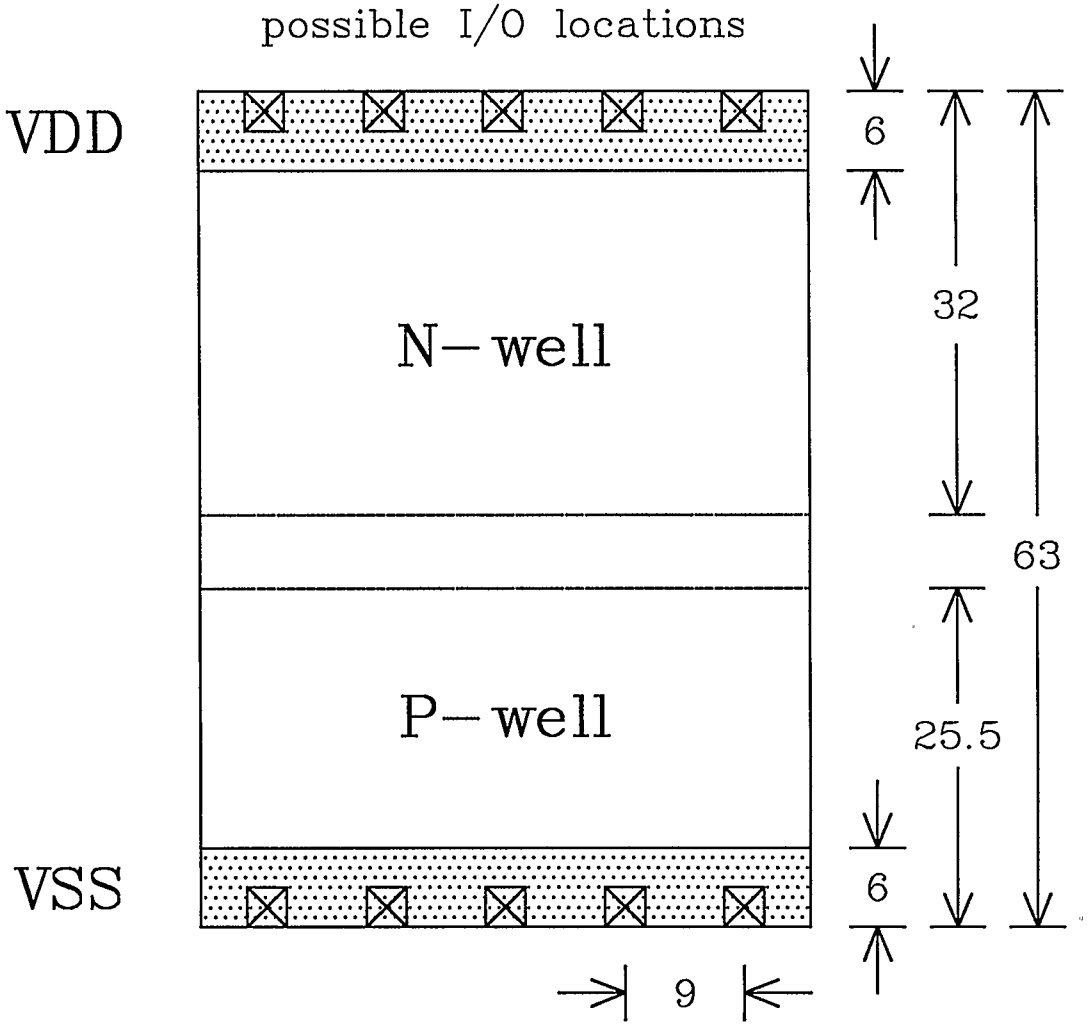


Figure 2.5: Adopted standard cell methodology

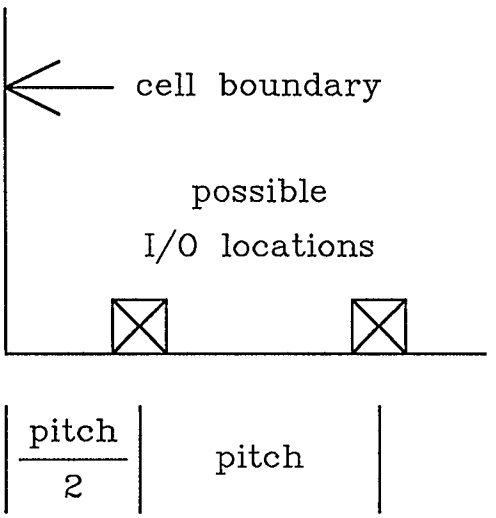


Figure 2.6a: Ideal cell design

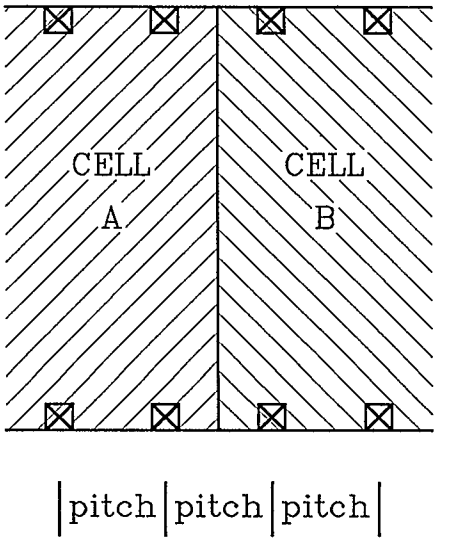


Figure 2.6b: Ideal cell interface

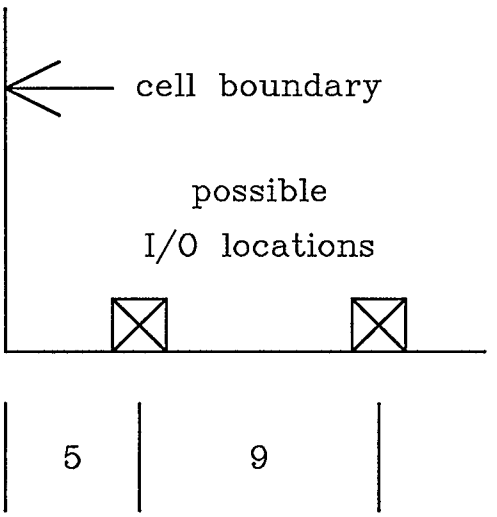


Figure 2.6c: Actual cell design

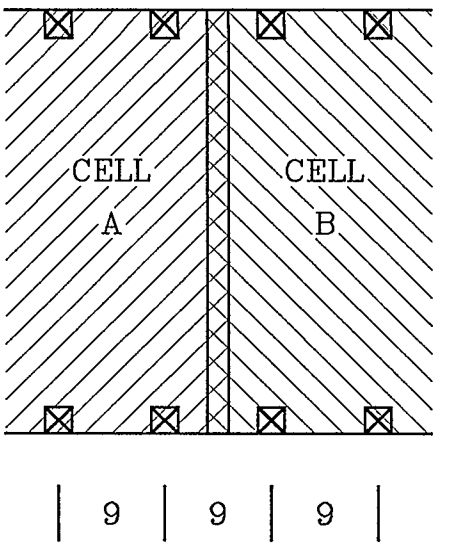


Figure 2.6d: Actual cell interface

Chapter 3

Design Environment and Procedure

3.1 Introduction

Recently, designers have found that the sheer size of their designs has warranted the use of extremely sophisticated CAE environments. These environments tend to manifest themselves in dedicated design workstations. An accurate portrayal of the industry standard entails, besides aesthetically pleasing design facilities, several verification aids, schematic capture, and place and route software.

According to Collett [26], most standard cell vendors support either Mentor Graphics, Daisy, or Valid Logic workstations. This claim is validated by [27]; of the standard cell vendors listed, overwhelming favourites were Mentor Graphics, Daisy, Valid Logic, and Calma workstations. Also, as a related aside, of the gate-array vendors listed in [28], most used either Daisy, Mentor Graphics, Silvar-Lisco, or Valid Logic workstations.

Standard cell design and development was effected on the Mentor Graphics DN550 and DN660 workstations and a VAX 8550 made available to us at NovAtel.

The remainder of this chapter describes briefly both the design environment and the design procedure.

3.2 Standard cell design procedure

Standard cell development may be fractured into design and verification phases. Cell design was performed exclusively on the Mentor Graphics workstations and may be further subdivided into three distinct levels of abstraction: a physical *layout*, a *transistor-level schematic*, and a *symbolic schematic*. Figure 3.1 illustrates these three design levels using the common inverter.

Layout has been accomplished using the program *chipgraph* [29]. This editor is similar to *CAESAR* [30] in that it operates on individual design masks as opposed to symbolic representations [31, 32, 33] or design primitives [34]. In each layout, all I/O points must be labelled for identification. To accelerate the design process, designs may be initialized either through the use of a general template or by copying a previous layout. The general template has the form shown in Figure 2.5 and is comprised of both supply rails and both wells. Initialization through layout duplication was avoided unless justified by logical similarities between designs.

Transistor-level schematics were composed using the network editor, *neted* [35]. Within the network editor, transistors and other primitives are native. Hence, the schematic may be quickly assembled through simple interconnection of

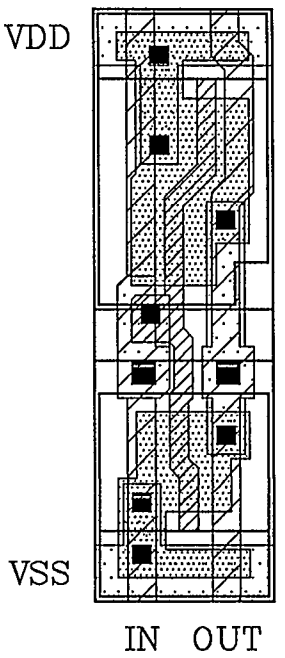


Figure 3.1a: Inverter layout

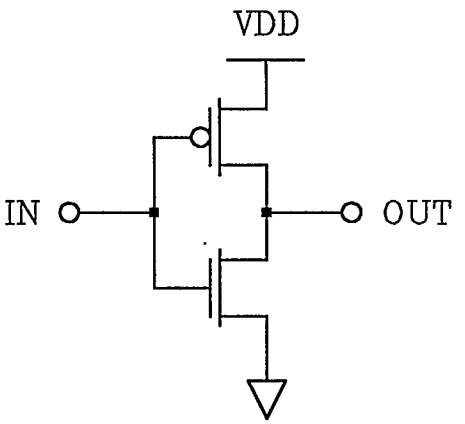


Figure 3.1b: Inverter transistor-level schematic

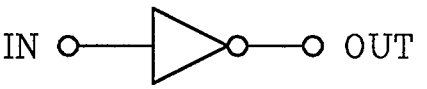


Figure 3.1c: Inverter symbolic schematic

primitives. For verification purposes, all I/O points must be labelled as in the layout.

Symbolic schematics have been created via the symbol editor, *symed* [35]. Though symbols may be manufactured expressly using graphical primitives (lines, arcs, circles, et cetera), this is unnecessarily tedious. A better method entails the duplication and modification of existing symbols from other libraries as most schematic symbols are standard. And again for verification purposes, all I/O points must be labelled as in the layout.

Verification assumes several forms: a design rule checker (DRC), layout versus schematic (LVS), layout parameter extraction (LPE) and simulation via *SPICE2G.6* [36]. The first three verification aids are in fact facets of the IC verification tool, *DRACULA* [37]. All verification was performed on the Mentor Graphics workstations except for simulation which was done on the VAX.

Besides the layout itself, the DRC requires a user-defined set of rules. These rules describe geometrically, those intermask relationships which constitute design rule violations. All such violations are logged in a file by the program.

LVS extracts a schematic from the layout and compares this to the user-defined circuit schematic. Again, errors are recorded in a file. When used in

tandem, DRC and LVS can virtually ensure design integrity; the DRC assumes a geometric perspective while LVS polices functionality.

LPE is used as a precursor to simulation and is responsible for performing two tasks: assembly of a SPICE simulation model (deck) and the extraction of all parasitic capacitances from the layout. Extraction of parasitic capacitance, of course, helps provide a more accurate simulation model. Unfortunately, LPE is not completely thorough as source and drain areas and perimeters must be measured by hand and included in the SPICE deck if desired. The author found the absence of this feature both inconvenient and time consuming.

The actual design sequence is shown in Figure 3.2. Here, design flow is clearly marked in flow-chart fashion using *pass-fail* conditions after each verification stage. While the pass and fail conditions for DRC and LVS are understood, not much has been said regarding simulation. SPICE may be considered to have failed if the simulated cell functionality does not comply with the operational criteria outlined in the introduction. Note that if a verification stage fails it is usually indicative of a layout oriented problem.

3.3 Determining susceptibility to latch-up

Since designs will be fabricated using a bulk CMOS process, latch-up becomes a major concern. So in addition to the verification aids used, an attempt was made

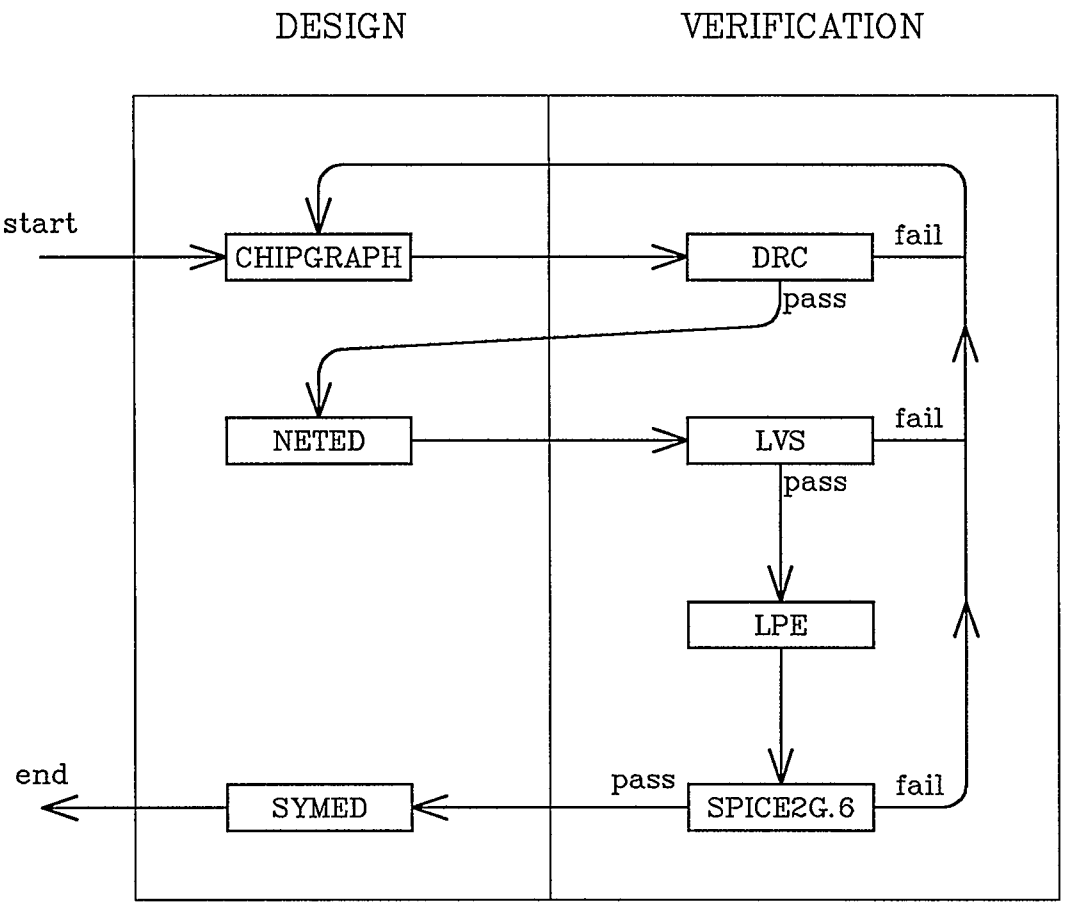


Figure 3.2: Standard cell design procedure

to incorporate Waterloo's *LAF* [38] package. LAF's sole purpose is to identify those designs which are susceptible to latch-up. It was hoped that perhaps designs could have been declared insensitive to latch-up with a minimum of theory.

All cell designs in the library include structures with non-orthogonal (forty-five degree) edges. And unfortunately, LAF only understands orthogonal geometries. Massaging designs into an orthogonal form by *edge jagging* resulted in polygons too large to be handled by the package. Further attempts to accommodate LAF by *polygon fracturing*, or the splitting of polygons with an excessive number of vertices into smaller portions also failed. The program authors were unable to correct the situation within the time frame of this thesis.

As we cannot ignore latch-up, circumstances necessitate both a review of the latch-up phenomenon and a conscious effort to minimize latch-up susceptibility through design techniques.

3.4 Latch-up in CMOS

Latch-up is a condition which may be attributed to the crux of CMOS processing; different substrates must be used to fabricate n- and p-channel devices. Consider the simplified bulk CMOS inverters in Figure 3.3. In addition to the devices intentionally created, parasitic bipolar transistors have resulted because the two substrates actually interface.

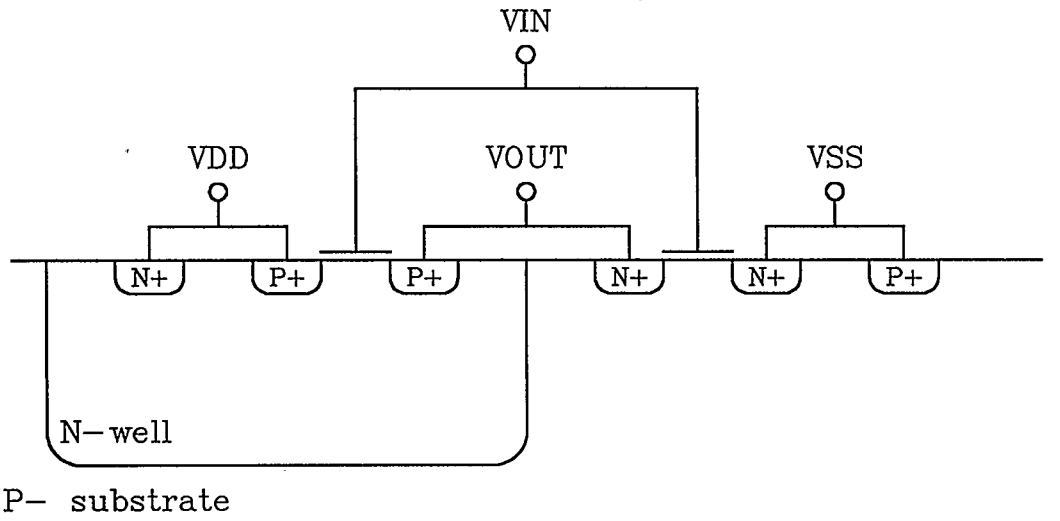


Figure 3.3a: Simplified inverter using an N-well technology

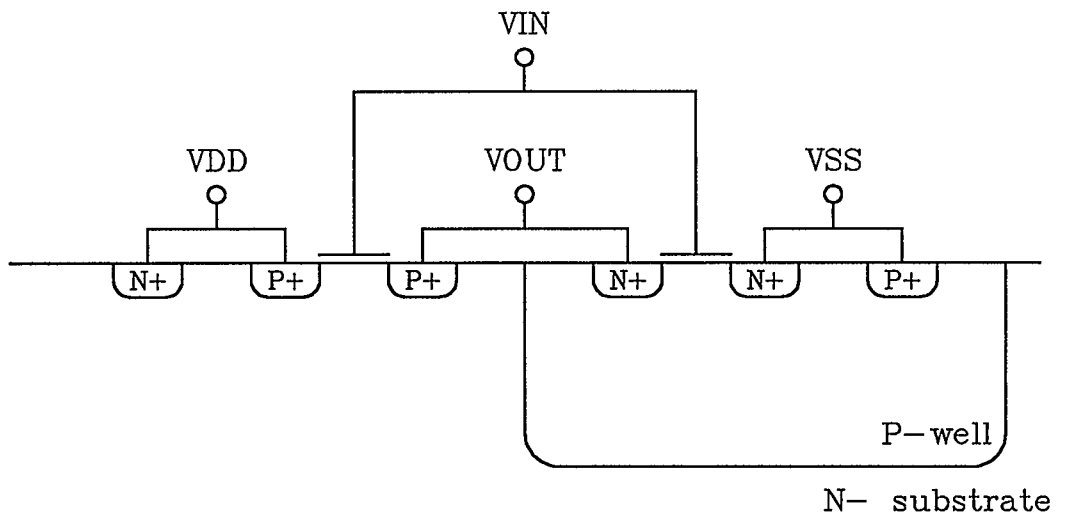


Figure 3.3b: Simplified inverter using a P-well technology

Vertical transistors turn up in the wells. Here, bases are formed by the wells themselves while collectors and emitters are formed by, respectively, the native substrate and source/drain (*S/D*) areas in the wells. Horizontal transistors arise with the native substrate as a base. Collectors and emitters become, respectively, the wells and the S/D areas in the native substrate. Effective transistors and resistive paths complementing Figure 3.3 are shown in Figure 3.4.

Circuit schematics extracted from either Figure 3.4a or 3.4b are similar (see Figure 3.5). Normally, all base-emitter junctions are biased such that the parasitic bipolar transistors are *blocked*. However, if substrate conditions forward bias these junctions hard enough to drive the transistors, a direct path from the power supply to ground ensues for current in the substrate. This is the *latched* state. The currents involved are unusually destructive and are easily capable of corrupting normal functionality.

To describe the latched condition in more detail, consider the inverter in Figure 3.4b. If the base-emitter junction of either of the lateral PNP transistors becomes forward biased, the P+ diffusion will inject holes into the substrate. Holes that do not recombine may be collected by the reverse biased well-substrate junction. Once in the P-well, the holes become majority carriers and may be swept toward the P+ substrate contact. If an increase in the well potential induced by this current is sufficient to forward bias a base-emitter junction in the well, then an N+ emitter will inject electrons into the well. Electrons collected by the N- substrate

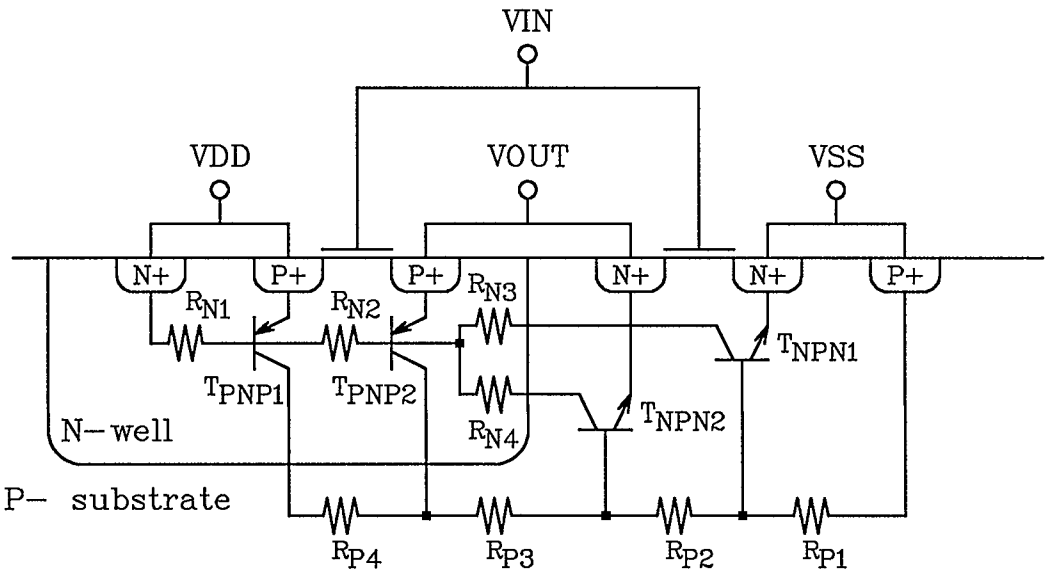


Figure 3.4a: Parasitic devices within an N-well inverter

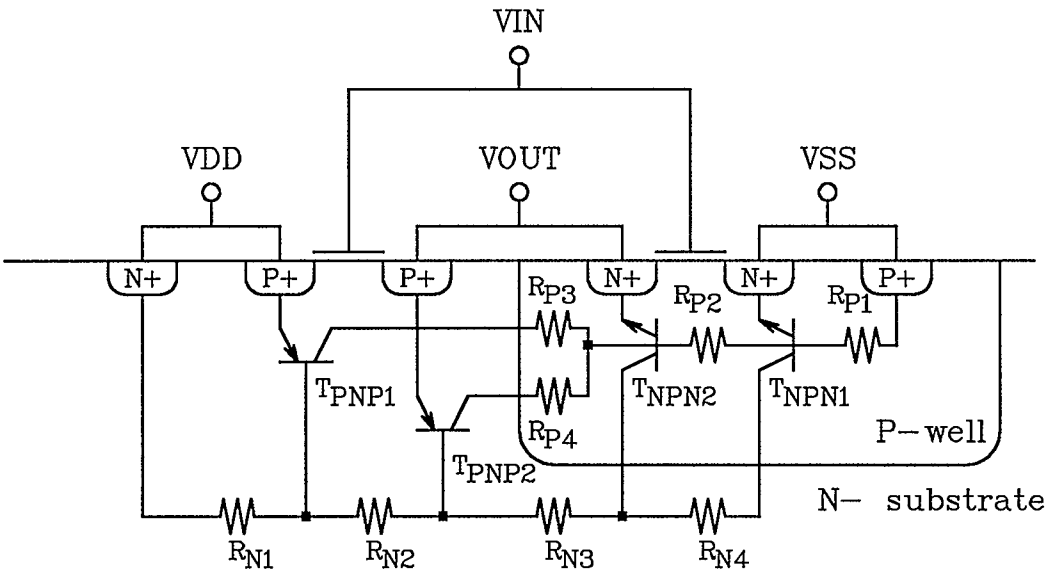


Figure 3.4b: Parasitic devices within a P-well inverter

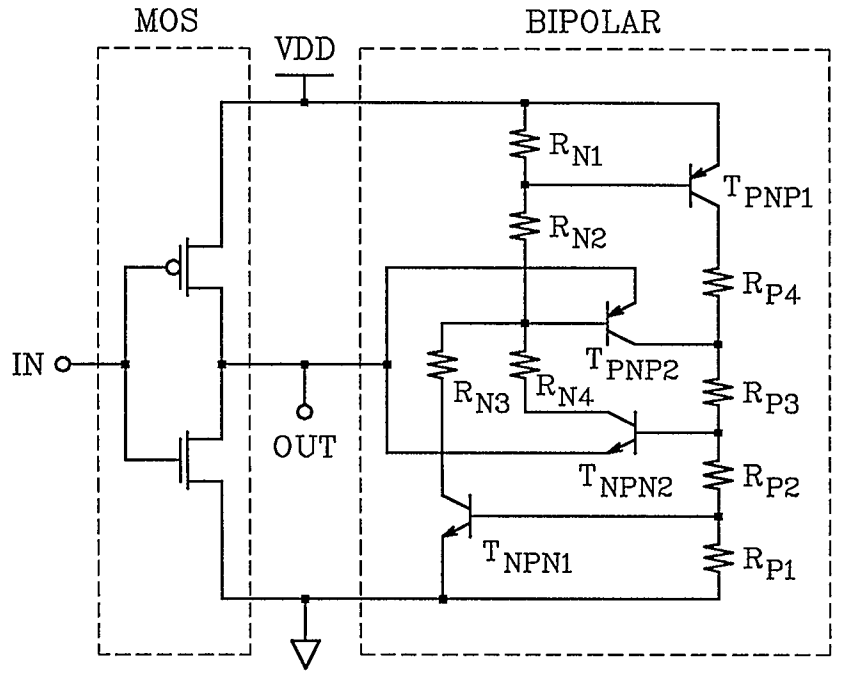


Figure 3.5a: MOS and bipolar schematics of an N-well inverter

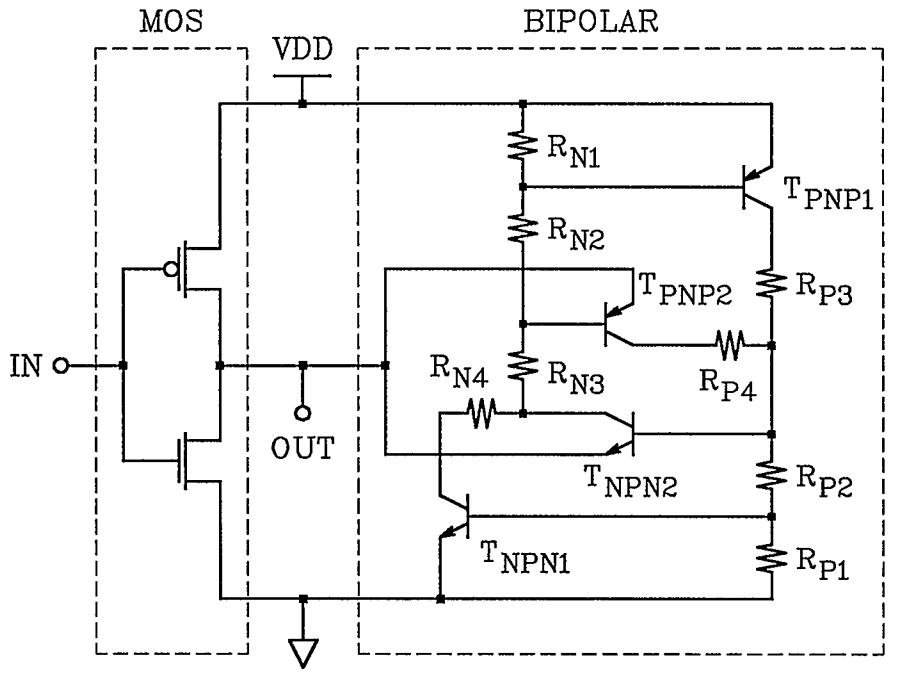


Figure 3.5b: MOS and bipolar schematics of a P-well inverter

and swept toward the N+ substrate contact may cause a voltage drop in the substrate large enough to forward bias a base-emitter junction in the substrate thereby sustaining the latched state.

Troutman [39] lists several possibilities (*mechanisms*) of which any one may cause (*trigger*) latch-up. These include:

- output node overshoot/undershoot
- input node overshoot/undershoot
- avalanching well-substrate junction
- avalanching S/D junctions
- punchthrough from the well to an external diffusion
- punchthrough from the native substrate to an external diffusion
- parasitic field devices
- floating well

As Troutman has elected to portray each of these mechanisms in the context of an N-well process, we shall use a P-well process for backwards compatibility.

Output/input node overshoot occurs when the voltage on a P+ diffusion output/input node exceeds that of the substrate. Holes are injected into the substrate and initiate the sequence of events. For output/input node undershoot, the voltage on an N+ diffusion output/input node must fall below that of the P-well. Here, latch-up is initiated by the injection of electrons into the well.

An avalanching well-substrate junction is caused by excessively large power supply voltages. As the junction between the well and substrate breaks down,

electrons are injected into the substrate and holes into the well. NPN and PNP transistors turn on at approximately the same time with this mechanism.

An avalanching S/D junction is also caused by a high voltage differential but initiates latch-up in a much different fashion. An avalanching N+ drain will produce a hole current in the P-well which in turn may forward bias a nearby source-well junction. Similarly, an avalanching P+ drain produces a substrate electron current which may drive a lateral PNP transistor.

Punchthrough is a phenomenon attributed to high voltages and/or the proximity of S/D regions to the well-substrate interface. Punchthrough occurs whenever the depletion region surrounding the well-substrate junction extends far enough to reach any S/D region. For N+ diffusions in the well, this entails an electron current in the substrate that may turn on a lateral PNP device. For P+ diffusions in the substrate, a hole current in the well may drive a vertical NPN transistor.

Parasitic field devices are similar in nature to punchthrough except that depletion region growth under the field oxide is assisted, either by charges trapped in the oxide or by an unintentional gate.

Finally, a floating well is disastrous as the well-substrate junction cannot be guaranteed to be reverse biased.

The effect that each of these mechanisms may have on the library is discussed in the design considerations section of the next chapter.

Chapter 4

Library Development

4.1 Introduction

Having explained the design procedure and environment, we can proceed to development of the library. We begin by addressing those factors common to all cells such as the design rules and standard cell dimensions. Then the cells that were designed are described and some layout particulars are covered. Finally, a section is presented on characterization through simulation.

4.2 Design rule development

In practice we find that with respect to design rules there are two distinct sets which must be observed. These are the *intracell* rules which describe layer relationships within a cell and *intercell* rules which describe layer relationships between cells. Intercell rules are actually extensions of the intracell rules but must still be expressed to ensure no design violations occur when cells are placed adjacent to one another.

4.2.1 Intracell rules

As mentioned earlier, generic designs may not be realized by adopting the design rules of a single vendor. Instead, prospective companies were first solicited for their two micron design rules. In all, five process lines were of particular interest. Three of these use an N-well technology and two have P-wells. From the design rules for these processes, the most aggressive yet encompassing set was derived. As this generic set of rules is rather lengthy, it has been placed in Appendix A.

Our process contains the following layers: N-well, P-well, active, polysilicon, N+ (inclusion), P+ (inclusion), contact, first-level metal, via, second-level metal, and overglass. Guard layers remain the province of the vendors as they are usually derived from well dimensions. Both N+ and P+ masks have been made inclusive to realize the largest number of process variants. For example, if a process requires designs to be submitted with P+ inclusion and N+ exclusion (as all our target processes do) then software can reassign the N+ mask to be identical to the P+ mask before fabrication. The converse is true if a process demands N+ inclusion and P+ exclusion. And of course, there actually are some processes which will require both masks to be inclusive.

In compliance with thesis objectives, the generic design rules have been compared to published sets of scalable or lambda based rules [16, 17]. As an aside

the design rules found in [17] are in fact the set endorsed by MOSIS [40, 41]. Our design rules, with few exceptions, are either identical or more conservative than the published rules. In cases where our rules do not conform to MOSIS specifications, the difference is so minimal that problems may only begin to appear when using extreme scaling factors. Consequently, the library may be considered scalable and may take advantage of finer fabrication lines as processing technology improves.

4.2.2 Intercell rules

To compose intercell rules from intracell rules, one must note how far each layer should be separated from all other layers. Without exception, the limiting or largest spacing value turns out to be the relationship of a layer with itself. For example, the furthest that first-level metal need be separated from any other layer is three lambda - and that is from itself.

To elaborate on the first-level metal spacing example, let us consider two cells containing first-level metal which follow the ideal tessellation guidelines illustrated in Figures 2.6a and 2.6b (see Figure 4.1). If we define *x1* as the distance from first-level metal to the interface for the first cell and *x2* as the complementary distance in the second cell, then for a design rule violation to appear the following condition must be true.

$$x1 + x2 < \textit{first-level metal intracell spacing rule}$$

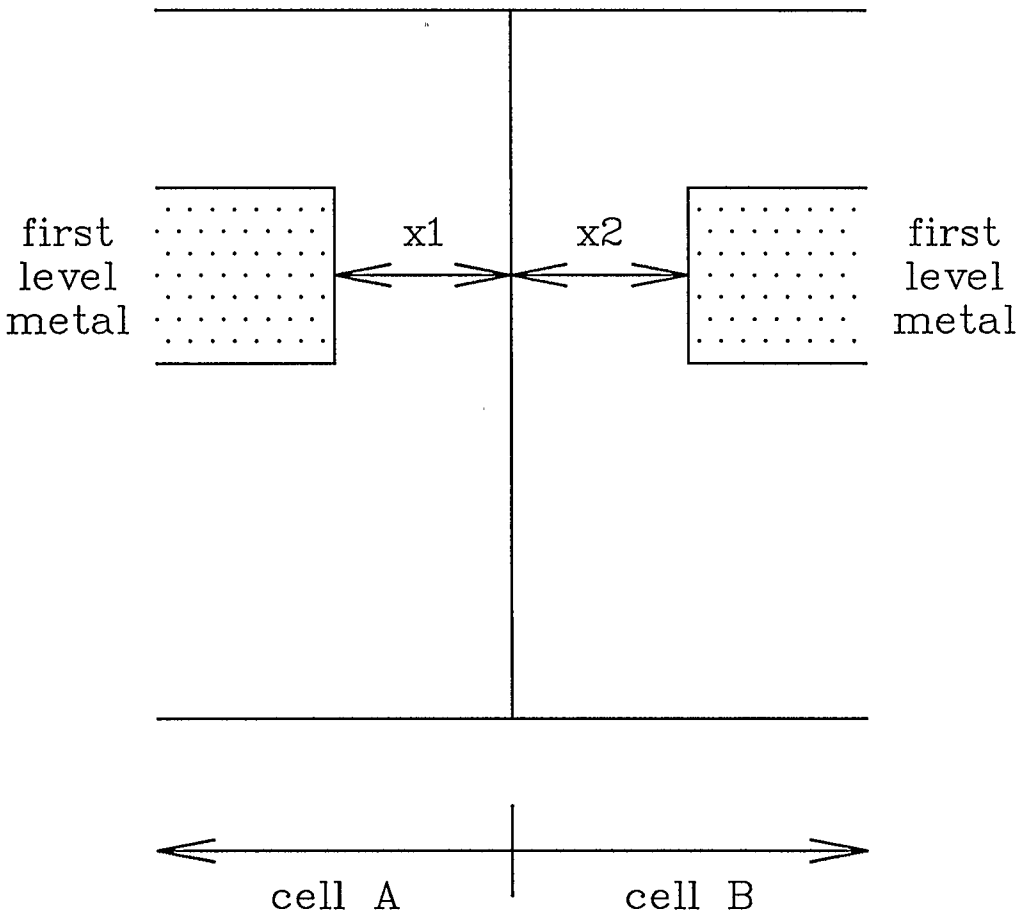


Figure 4.1: Adjacent cells with first-level metal

Clearly, the easiest way to ensure that a violation does not occur is if

$$x1 \geq \textit{(first-level metal intracell spacing rule)/2}$$

$$x2 \geq \textit{(first-level metal intracell spacing rule)/2}$$

For any intracell spacing rule in general, the intercell rule should be half this distance. Because of the design strategy employed, intercell rules only apply to the left and right faces of any cell. Analysis yields the intercell rules in Table 4.1.

As this table is incomplete, the absence of some layers will have to be justified. N-well and P-well layers are not included in the table since these are embedded in the standard cell methodology and will, in a row, butt from cell to cell to form a single well. Interconnection layers such as contact and via have been ignored as these will always be enveloped by one or more of the table layers. The N+ and P+ masks are used to define doping for the active regions. The design rules specify that they must cover the active layer by two lambda. Since active may come to within two lambda of the interface, that implies that it is possible for N+ and P+ to lie coincident with the interface. The design rules also state that N+ and P+ should be spaced by three lambda. Accordingly, the intercell rule for N+ and P+ should be zero lambda or three lambda. Designs may use either of these values but nothing in between.

Table 4.1: Some initial intercell rules

Layer	Minimum distance to interface
Active	2 lambda
Polysilicon	1.25 lambda
First-level metal	1.5 lambda
Second-level metal	1.5 lambda

Unfortunately, examination of the design rules reveals that if the active layer is allowed to come within two lambda of the interface, or subsequently the well edge, a cell will be unable to *stand alone*. This is because the well is supposed to overlap active by two and a half lambda. Three solutions exist. The first is to adjust the active intercell rule to two and a half lambda. This makes inefficient use of silicon. The second is to place half lambda *caps* on the ends of the cell rows as in Figure 4.2a. A third and better method is to simply expand all cells by an extra half lambda on both left and right faces (see Figure 4.2b). Then within each row, wells and supply rails will overlap instead of merely butting; this scenario was depicted in Figures 2.6c and 2.6d. Adjusting intercell rules to account for cell expansion produces Table 4.2.

4.3 Standard cell dimensions

There are only two standard cell dimensions that need be calculated - horizontal pitch and cell height. While horizontal pitch falls directly from the design rules, cell height is more complicated and is deserving of the calculations performed in subsequent sections.

4.3.1 Horizontal pitch

Recall that as part of our standard cell methodology, all interconnections extend out of the top and bottom faces of a cell. To guarantee design regularity,

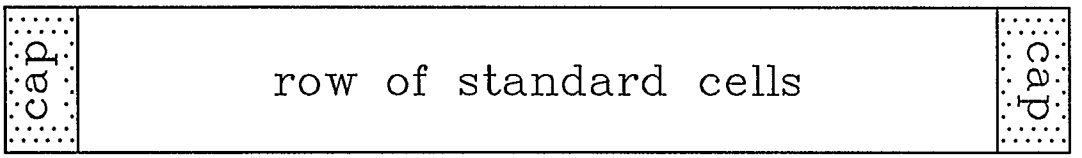


Figure 4.2a: Cell row with caps

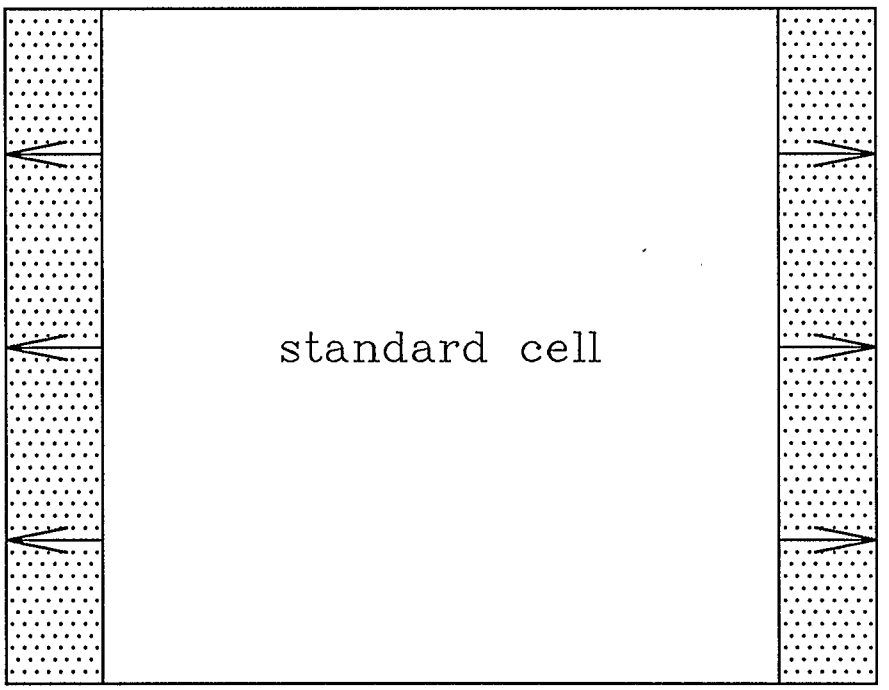


Figure 4.2b: Cell expansion

Table 4.2: Final intercell rules

Layer	Minimum distance to interface
Active	2.5 lambda
Polysilicon	1.75 lambda
First-level metal	2 lambda
Second-level metal	2 lambda
N+	0.5 or 3.5 lambda
P+	0.5 or 3.5 lambda

possible I/O locations are constrained to exist at a predefined interval. This interval is known as the horizontal pitch. A complementary distance, the vertical pitch, can be used in concert with the horizontal pitch to establish an I/O grid for use in routing channels.

In practice it is best if the horizontal pitch is kept as small as possible for two reasons - firstly to avoid I/O bound cells and secondly to enhance the possibility of including feedthroughs in layout.

For us, horizontal and vertical pitch are identical and may be defined as the minimum separation between two adjacent first-level metal to second-level metal connections. Generic design rules yield a value of nine lambda (see Figure 4.3).

4.3.2 Cell height

To calculate cell height we will use an approach similar to the one proposed in Kang [25] except that we will limit ourselves to the examination of a two input NAND gate. One reason for this is that most libraries are characterized with respect to the two input NAND gate as in [20], vendor documentation, and private communication. Another reason is to simplify the approach, especially with respect to computation. Like Kang, we shall attempt to establish a cell height via design rules and transistor heights and ratios to obtain short propagation delays and small

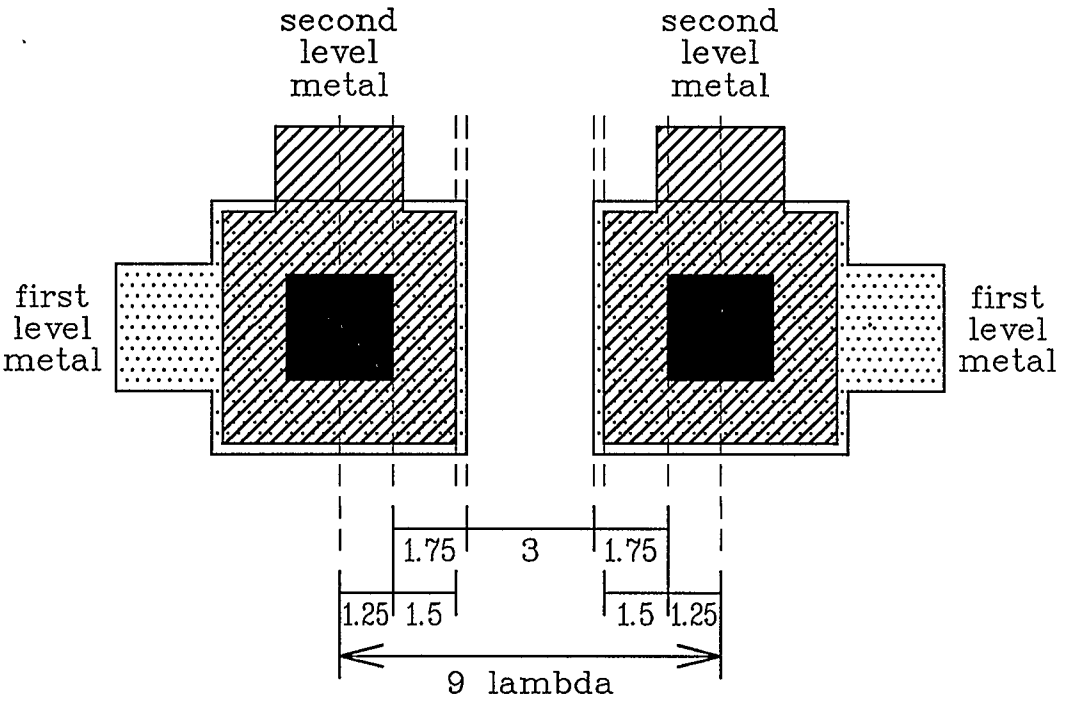


Figure 4.3: Horizontal pitch

chip area while maintaining good noise margins. In our analysis though, the product of propagation delay and chip area will not be minimized.

To begin we recall from the standard cell methodology that cell height may be decomposed into three portions, the two well areas and the separation between them. Further, each well may be subdivided into spaces for a supply rail and transistors (see Figure 4.4). Transistors are isolated from the rails to minimize switching noise on the rails. Separations between transistors and the well edges exist because of the design rules. To calculate cell height then, we must individually calculate the transistor widths, rail widths, and the various separations.

It is proposed that the cell height be determined in the following fashion. First, a simplified two input NAND gate be layed out for simulation by SPICE. Then a noise margin analysis can be used to select an appropriate transistor ratio. Simulations may be performed with this fixed ratio in a propagation delay analysis to determine an optimum drive size. Finally, with the transistor dimensions and ratio selected, simulations yielding switching currents may be coupled with metal migration considerations to suggest adequate rail widths. All separations fall directly from the design rules.

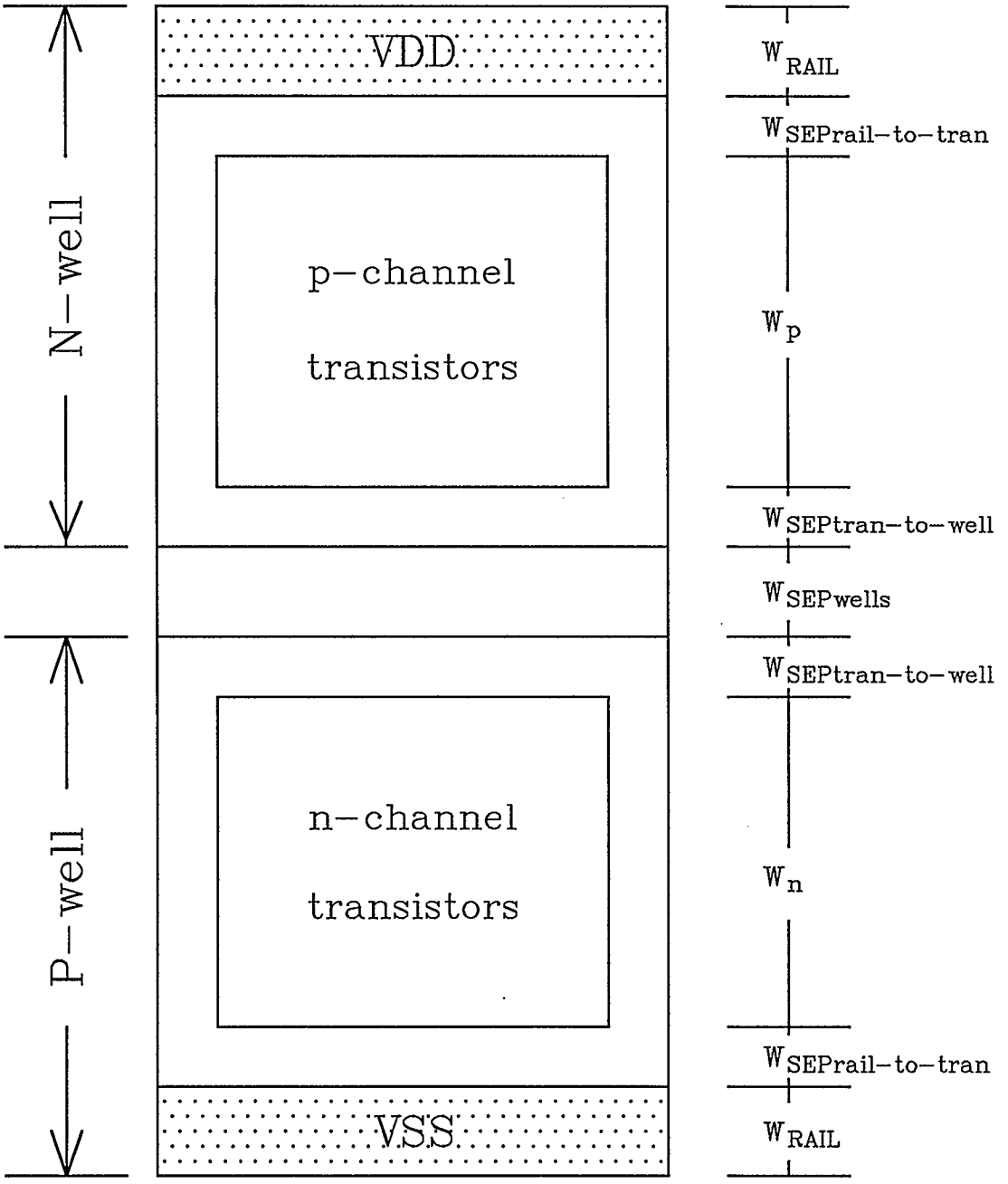


Figure 4.4: Cell decomposition

4.3.2.1 Simplified two input NAND gate

The circuit to be examined with output loading is shown in Figure 4.5. The diagram depicts the load as being comprised of two parts - a routing capacitance and a formal load. The formal load is in fact the input capacitance of one input of a second two input NAND gate and the routing capacitance is the load associated with the metal interconnect between cells. We are justified in modelling the routing in this fashion since metal is used and resistance is negligible. Also, it is important to note that all models in this section are deliberately kept simple as there is more than one target process and we are only attempting to calculate an approximate cell height.

To calculate the routing capacitance we shall assume as in Kang that the intercell routing length is seventy horizontal pitches.

$$C_R = A_R \, C_{Rav}$$

A_R is the routing area and C_{Rav} is the average metal to substrate capacitance per unit area. An average is used as it is assumed that half of the routing is in first-level metal and the other half in second-level metal. From vendor documentation for the processes being used,

$$C_{Rav} = 2.45 * 10^{-5} \, pF \, lambda^{-2}$$

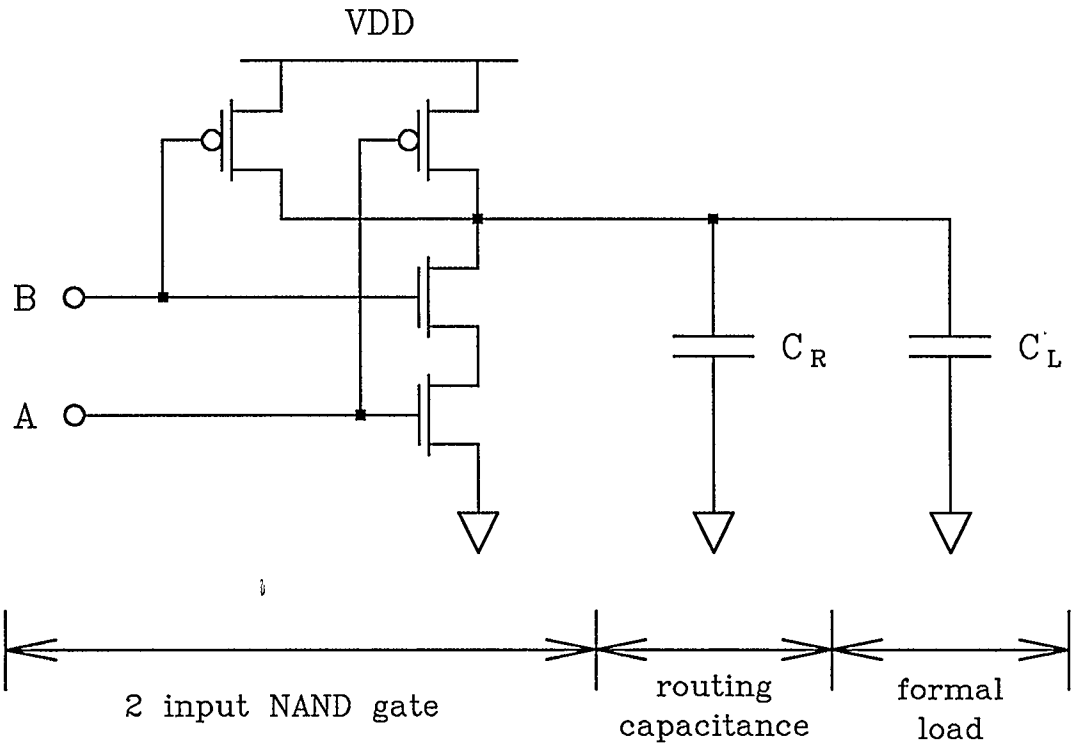


Figure 4.5: Simple two input NAND gate with load

And knowing the horizontal pitch is nine lambda, we rely on design rules to obtain

$$A_R = (\ 70\ )\ (\ 9\ lambda\ )\ (\ 3\ lambda\ ) = 1890\ lambda^2$$

$$C_R = (\ 1890\ lambda^2\ )\ (\ 2.45 * 10^{-5}\ pF\ lambda^{-2}\ ) = 0.046305\ pF$$

Note that we have taken the liberty of using lambda as the unit of area. This does not imply that the routing capacitance is fixed for all scaling factors but that we have assumed lambda to be one micron. This assumption is valid only because we will be simulating with device parameters for two micron processes. It is purely a mathematical convenience and is used throughout the remainder of this chapter.

For the gate capacitance of a two input NAND gate, we assume that both inputs have identical capacitive values.

$$C_L = A_G C_G$$

Here, A_G is the gate area and C_G is the gate capacitance per unit area. From vendor documentation

$$C_G = 1.38 * 10^{-3}\ pF\ lambda^{-2}$$

And since we are using two lambda gate lengths

$$C_L = (2\ lambda)\ (W_p + W_n)\ (1.38 * 10^{-3}\ pF\ lambda^{-2})$$
$$= 2.76 * 10^{-3}\ (W_p + W_n)\ pF$$

where W_p and W_n are respectively the widths of the p-channel and n-channel transistors.

Collectively, the routing and gate capacitance are called a *unit load.*

$$C_U = C_R + C_L$$
$$= 2.76 * 10^{-3}\ (W_p + W_n) + 0.046035\ pF$$

Once library development commences the unit load is used as a base on which to characterize the entire library. The value does not become finalized until the layout for the two input NAND is complete. If the layout changes, the entire library must be recharacterized.

Since all loads are capacitive and cells will be centre-fed as in [12], if we wish to simulate the circuit for any fanout other than one, a new load can be calculated by multiplying the unit load by the desired fanout. At some time simulations should be performed with a full load. We define a full load as a fanout of four.

For simulation purposes, Figure 4.6 shows a simplified layout of a two input NAND gate. This is not a complete layout. The only layers that have been utilized are polysilicon, active, first-level metal, and contact.

If we constrain this cell to stretching in a vertical sense, then from the design rules we can express all transistor dimensions as functions of their widths, W_p and W_n. First, the source and drain areas and perimeters for the p-channel transistors.

$$AS_p = 3.5\ W_p + 15\ lambda^2 \qquad PS_p = 2\ W_p + 13\ lambda$$
$$AD_p = 4\ W_p\ lambda^2 \qquad PD_p = W_p + 8\ lambda$$

Then the source and drain areas for the n-channel transistor driven by the input A.

$$AS_{nA} = 3.5\ W_n + 15\ lambda^2 \qquad PS_{nA} = 2\ W_n + 13\ lambda$$
$$AD_{nA} = 1.25\ W_n\ lambda^2 \qquad PD_{nA} = W_n + 2.5\ lambda$$

Finally, the dimensions for the n-channel transistor driven by the input B.

$$AS_{nB} = 1.25\ W_n\ lambda^2 \qquad PS_{nB} = W_n + 2.5\ lambda$$
$$AD_{nB} = 3.5\ W_n + 15\ lambda^2 \qquad PD_{nB} = 2\ W_n + 13\ lambda$$

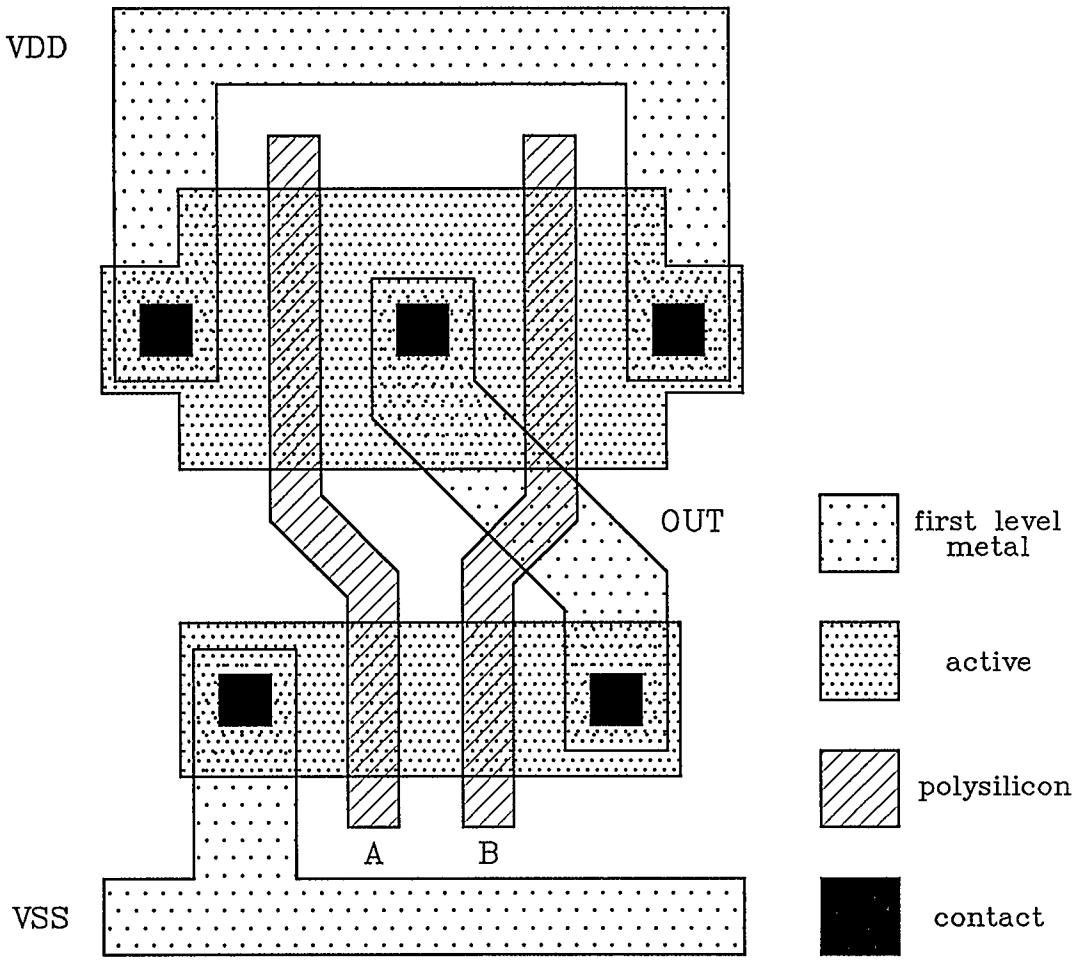


Figure 4.6: Simplified layout of a two input NAND gate

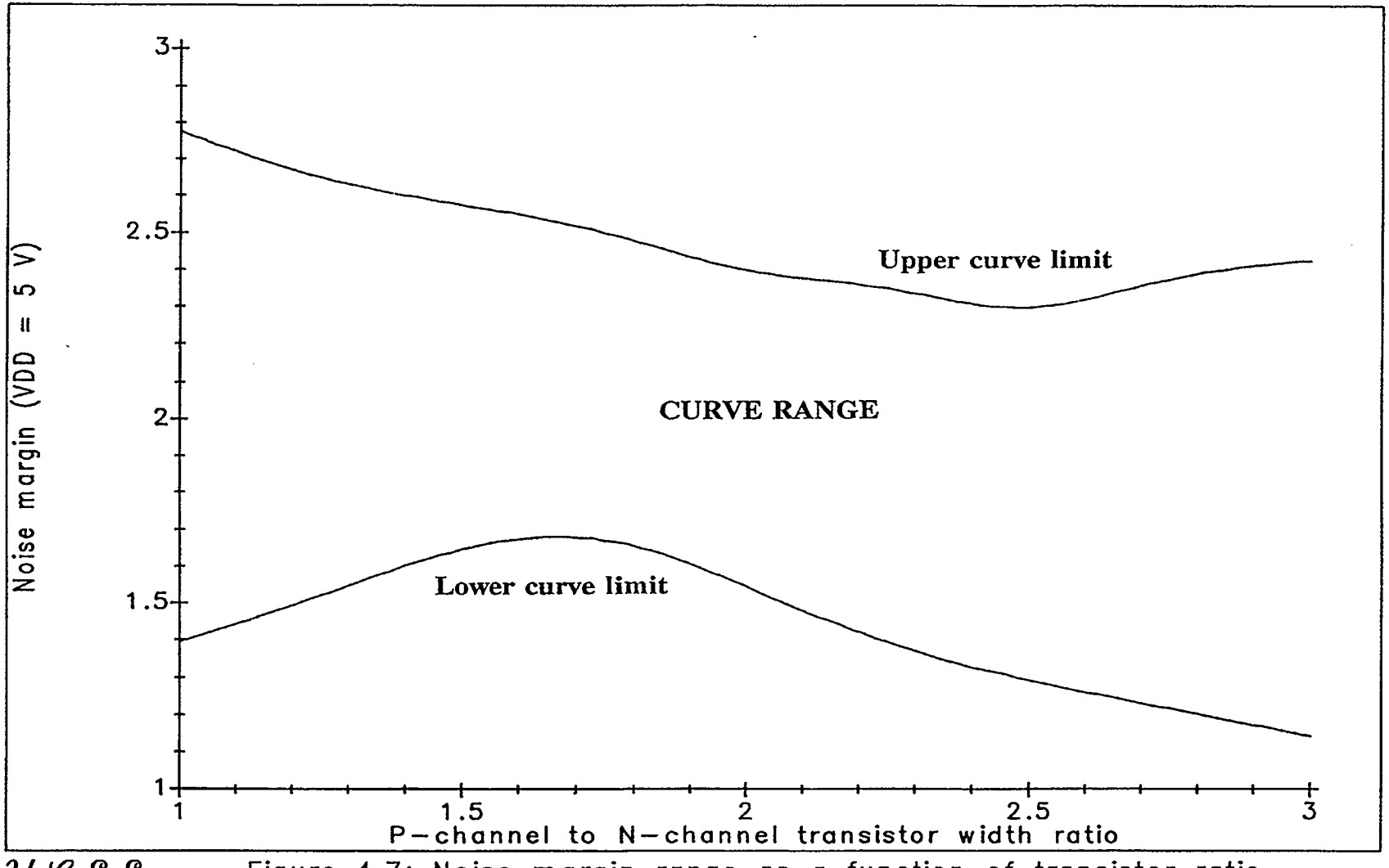
4.3.2.2 Noise margin analysis

By changing the ratio of W_p to W_n in the previous equations, one can observe how both the upper and lower noise margins vary as a function of the ratio. Simulations using SPICE give static transfer functions and from these the noise margins are extracted. In our analysis, the ratio was varied between one and three for all processes. For each process, two curves result. Rather than place all curves on a common plot or produce separate plots for each process, curve limits have been compiled to create the range shown in Figure 4.7.

From the lower limit on the plot it can be seen that best noise immunity is attained if a ratio of 1.75 is supported. With this small a ratio though, rise times and rising propagation delay times may suffer. But if we compensate by increasing the ratio, we decrease noise immunity. A ratio of two should prove an excellent compromise. Of course, this value is subject to individual layouts and will vary from device to device.

4.3.2.3 Propagation delay analysis

In the propagation delay analysis, the main objective is to note how propagation delay changes with device size. Obviously, since the gate capacitance is a function of device size, changing the device size will change the load. As device size is increased one would expect that as the gate capacitance exceeds the routing



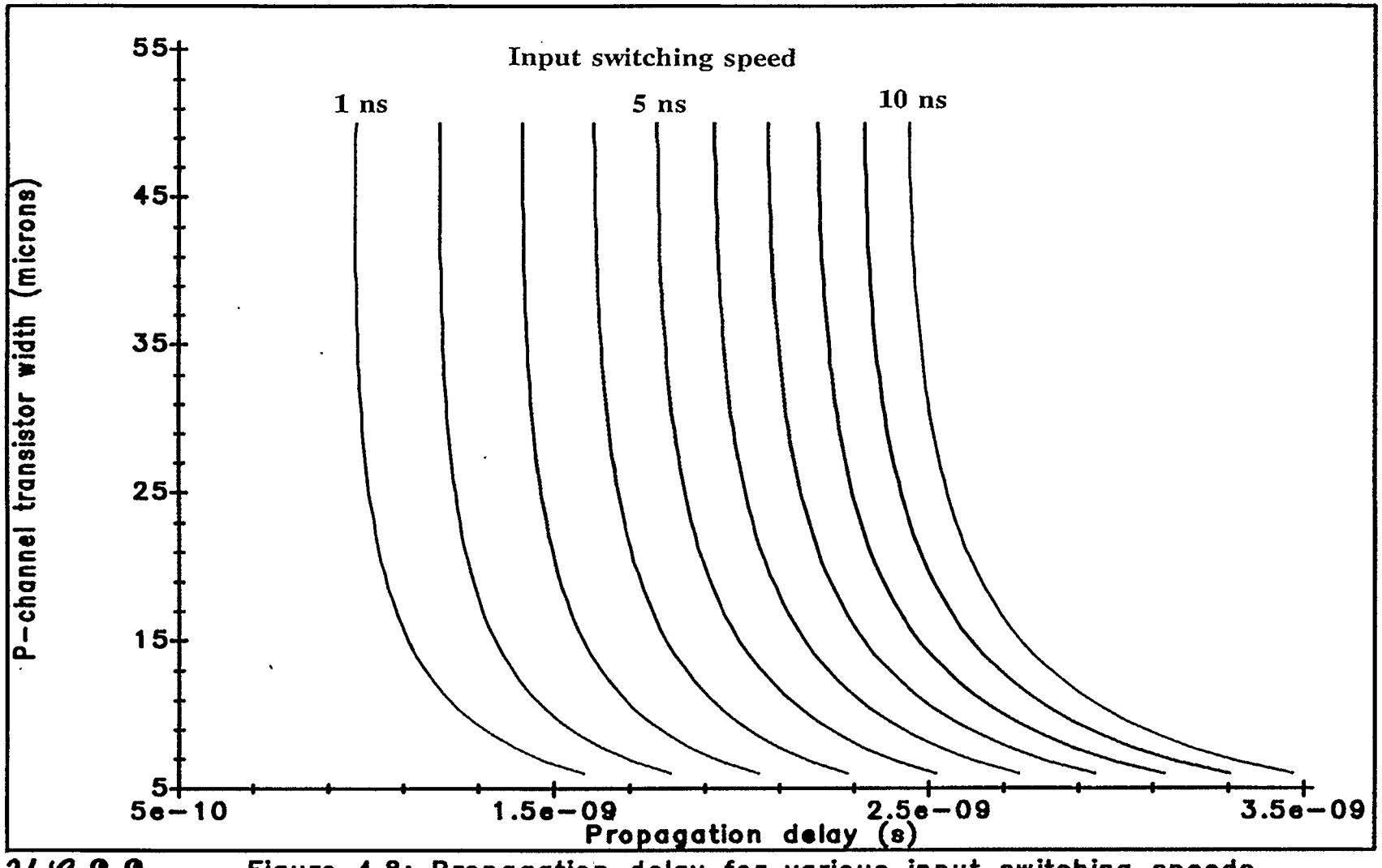
UCEE Figure 4.7: Noise margin range as a function of transistor ratio

capacitance, the added drive capability of a larger device will be offset by the increase in load. In other words, there will come a point when no further improvements in propagation delay may be gained by increasing the device size.

To define a device range for analysis we begin by examining the design rules. For an n-channel transistor, minimum device width is three lambda. Arbitrarily, an upper limit can be set to twenty-five lambda. If we are using a W_p to W_n ratio of two, this can alternately be expressed as a p-channel device width range of six to fifty lambda.

For each process, simulations have been performed over the device range. Also, since propagation delay is a function of the input waveform, simulations have been performed using various input ramp speeds. A family of curves similar to those in Figure 4.8 were obtained for each process. As expected, for large devices, propagation delay remained pretty much constant.

To select an optimum device size, one technique involves normalization of each curve to determine when marginal increases in device size fail to yield substantial decreases in propagation delay (ie. where the slope is -1). Of course, if normalization is performed, the result suggests an optimum drive size over the range simulated. For each process, recall we have a family of curves. An optimum device size was ascertained for each curve in the family. An optimal process device size was then calculated by averaging all curve-specific values. Averaging optimal



UCEE Figure 4.8: Propagation delay for various input switching speeds

process device sizes yields

Average optimum p-channel device size = 17.6 lambda

Average optimum n-channel device size = 8.8 lambda

For convenience, these numbers can be rounded up to twenty lambda for the p-channel transistor and ten lambda for the n-channel.

4.3.2.4 Rail width calculation

Using calculated transistor dimensions in our two input NAND gate, SPICE was used to determine current requirements for each process. Different scenarios were applied to simulate both the largest average and peak currents. These currents, in light of metal migration and our design strategy, serve to determine rail widths.

First, we consider average current. For the NAND gate, the largest amount of power is drawn when the switching speed of the input waveform is slow relative to the period and there is a full load being driven. For each process, simulations were performed assuming a minimal period (operating at rated speed) and that the cell switched once each period. The most current drawn by any process was

$$I_{CELLav} = 0.09927\ mA$$

Now assuming that an average library cell may draw twice this current and that a row may be comprised of twenty cells, row requirements become

$$I_{ROWav} = (2) (20) (0.09927\ mA) = 3.97\ mA$$

Consulting vendor documentation, we find that for the processes under consideration, maximum current densities in metal span from $0.65\ mA\ \mu m^{-1}$ to $1.0\ mA\ \mu m^{-1}$. Then to prevent metal migration, rail widths should be

$$W_{RAIL} = (3.97\ mA) / (0.65\ mA\ lambda^{-1}) = 6.1\ lambda$$

As the process consuming the most power and the process tolerating the smallest current density in metal are not one and the same, rail width may be relaxed to six lambda.

If we now consider peak current, the largest peak currents are drawn when the input waveform switches quickly and a full load is being driven. The highest peak current drawn by any process was

$$I_{CELLpk} = 3.807\ mA$$

If we make the same assumptions as we did for average current - an average library cell may draw twice the current and a row is comprised of twenty cells - this implies that to prevent metal migration, rail widths should be

$$I_{ROWpk} = (2) (20) (3.807\ mA) = 152.28\ mA$$
$$W_{RAIL} = (152.28\ mA) / (0.65\ mA\ lambda^{-1}) = 234.3\ lambda$$

Clearly, this is impractical. Mead and Conway [14] state that for pulses in the nanosecond range (simulated pulses for the NAND gate were in the sub-nanosecond range) lines can endure twice the maximum current density without sustaining damage. Also, it is improbable that two cells will ever switch simultaneously. Given this, rail widths of six lambda should suffice. However, before fabrication the designer should perform a system level simulation with the parameters for the target process. If the rail widths seem insufficient for a row, they may be easily widened since they reside on the periphery of the cell.

4.3.2.5 Cell height calculation

An initial value for cell height can now easily be computed by summing calculated values and values specified by design rules. Referring back to Figure 4.4

$$W_{SEPrail\text{-}to\text{-}tran} = 2\ lambda$$
$$W_{SEPtran\text{-}to\text{-}well} = 2.5\ lambda$$

$$W_{SEPwells} = 5.5\ lambda$$

$$\begin{aligned} W_{NWELL} &= W_{RAIL} + W_{SEPrail\text{-}to\text{-}tran} + W_p + W_{SEPtran\text{-}to\text{-}well} \\ &= 6 + 2 + 20 + 2.5\ lambda \\ &= 30.5\ lambda \end{aligned}$$

$$\begin{aligned} W_{PWELL} &= W_{RAIL} + W_{SEPrail\text{-}to\text{-}tran} + W_n + W_{SEPtran\text{-}to\text{-}well} \\ &= 6 + 2 + 10 + 2.5\ lambda \\ &= 20.5\ lambda \end{aligned}$$

$$\begin{aligned} W_{CELL} &= W_{NWELL} + W_{PWELL} + W_{SEPwells} \\ &= 30.5 + 20.5 + 5.5\ lambda \\ &= 56.5\ lambda \end{aligned}$$

It was proposed that cell height be made an integral number of vertical pitches. Then, cell height would have to be at least *63* lambda. After layout experimentation, *63* lambda was accepted for cell height, *25.5* lambda for P-well height, and *32* lambda for N-well height.

4.4 Design Considerations

Besides system I/O cells, or *pads*, standard cell libraries may include common SSI or MSI functions, cells for DSP, memory cells, and so on; library

contents are dictated by or tailored towards the types of systems being developed. With no particular application in mind, a good cross-section of common digital cells was selected for design. All are documented in Appendix B and are listed below.

2	inverters
5	NAND gates
3	AND gates
5	NOR gates
3	OR gates
1	XOR gate
1	XNOR gate
3	transmissions gates
12	D-type latches
8	D-type flip-flops
1	RS-type flip-flop
4	Two-stage clock buffers
4	tri-state buffers
1	multiplexer

In addition, a feedthrough cell was suggested to assist in routing. I/O cells have been neglected as these can be added from vendors' libraries prior to fabrication. Such action is justified by virtue of the fact that vendors invest considerable time and effort to develop I/O pads and protection circuitry compatible with their processes. This is not meant to imply that development of I/O cells would be worthless but that they are not a priority.

With respect to latch-up susceptibility, there was one outstanding safeguard which was taken to reduce the threat of some latch-up mechanisms. To avoid a floating well, butting contacts were included in all designs wherever possible. This not only allows cells to stand alone but also greatly reduces R_{N1} and R_{P1} in Figure

3.5. As a result, we combat all mechanisms because substrate currents must be fairly high to both initiate and sustain latch-up. Output and input node overshoot/undershoot are not much of a concern as these pertain mainly to the protection circuitry of pads. As the power supply is expected to be five volts, avalanching and voltage induced punchthrough should not pose a problem. Parasitic field devices and alternate forms of punchthrough should never result as this would render the design rules supplied by the vendors as unacceptable. It is foreseeable though that punchthrough may become an issue for large scaling factors.

Though many design issues have already been resolved by the standard cell design methodology, there are still enough cell-specific ones to warrant a separate section. Here, each design, or design class, is presented with schematics (where helpful) and a quick design discussion. Readers may find it beneficial to compare the schematics with their respective layouts in Appendix B.

4.4.1 Inverters

Two inverters were designed; one suitable for driving up to one full load (*medium-drive*) and one capable of driving up to two full loads (*large-drive*). For the medium-drive inverter, a standard layout was adopted using a transistor ratio of two as suggested in section 4.3.2.2. In generating the large-drive inverter, there was the option of either increasing the drive capability (channel width) of the

transistors or connecting several devices in parallel. The latter of these techniques was selected as very little well space remained for channel expansion.

Given two transistors in parallel, the layout area may be minimized if either a common source or a common drain is utilized. At the time the cell was designed, a common source seemed convenient. In practice though, a common drain should have been used as this would have greatly reduced output capacitance and enhanced cell performance.

4.4.2 NAND gates

Five different NAND gates have been designed; from two inputs to six inputs inclusive. All these cells were initially perceived in a traditional fashion; with parallel p-channel transistors and a series n-channel chain. But because the n-channel transistors are connected in series, body effect impairs cell operation. The problem becomes more pronounced as the number of inputs, and consequently the chain length, increases. In anticipation of slow switching times, some stratagems were investigated.

The first and perhaps the most obvious was to limit internal capacitance in the chain through common source/drain (*S/D*) area reductions. Efforts were taken to ensure that S/D areas were as feasibly small as the design rules would permit.

Secondly, for sufficiently large numbers of inputs, architectural modifications could have been made via cascaded logic. For example, the chain length of the conventional 4-input NAND gate in Figure 4.9 can be reduced if designed as in Figure 4.10. It is presumed that the time penalties incurred through cascading will be more than offset by device efficiency. This technique was rejected because of the added area requirements and because of uncertainty over the method's effectiveness.

Thirdly, to ascertain whether or not it was better to associate the same channel width with all transistors in the chain, several simulations were run using a simplified 5-input NAND gate. As in Figure 4.9, the n-channel transistor with the grounded source will for illustration be referred to as transistor A, the next transistor in the chain shall be transistor B, and so on. In these simulations, all n-channel transistors were allotted the same channel width except one. Then, as the channel width of this transistor was varied, cell behaviour was noted. Figure 4.11 shows simulated cell fall times. Note that only transistors B through E were varied.

From the graph it can be readily seen that varying the drive of a single device strongly influences cell operation. As the drive capability is reduced, fall times degrade. Conversely, increasing the channel width improves fall time. From the relative curve positions we can also see that it is preferable to have small-drive devices near transistor E than transistor A. Large-drive devices are better located near transistor A. Given this, we can infer that the drive capabilities of individual

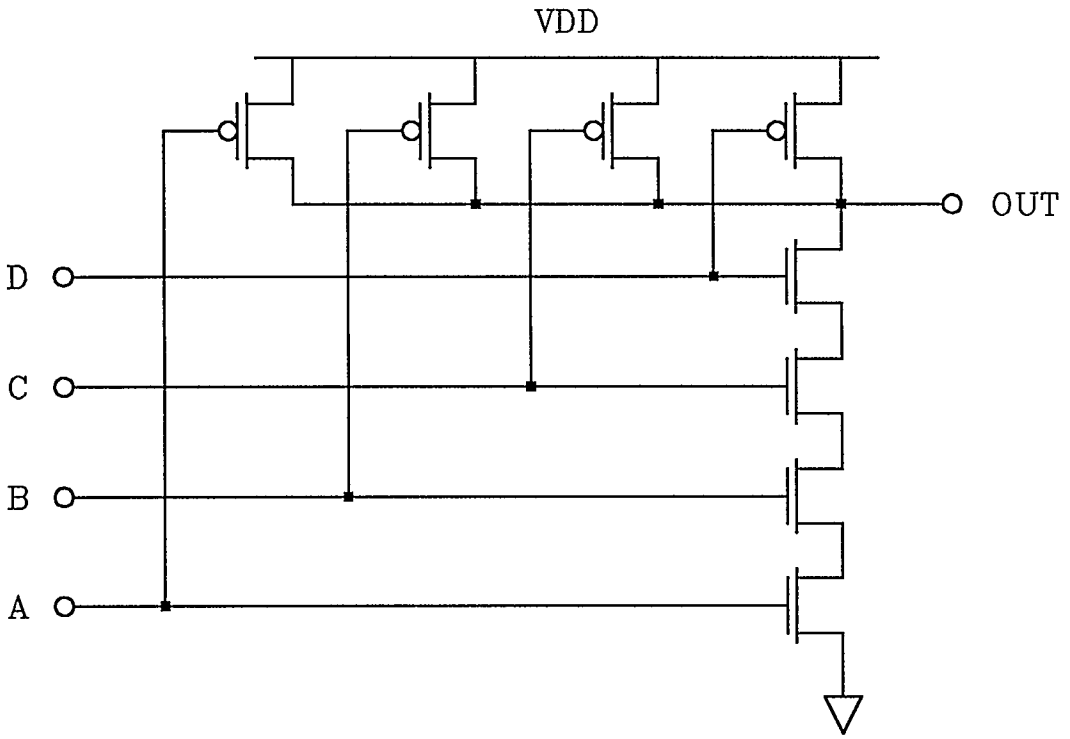


Figure 4.9: Conventional four input NAND gate

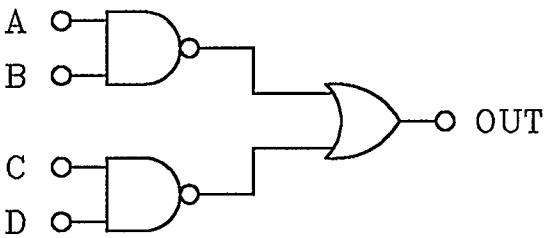


Figure 4.10: Four input NAND gate using cascaded logic

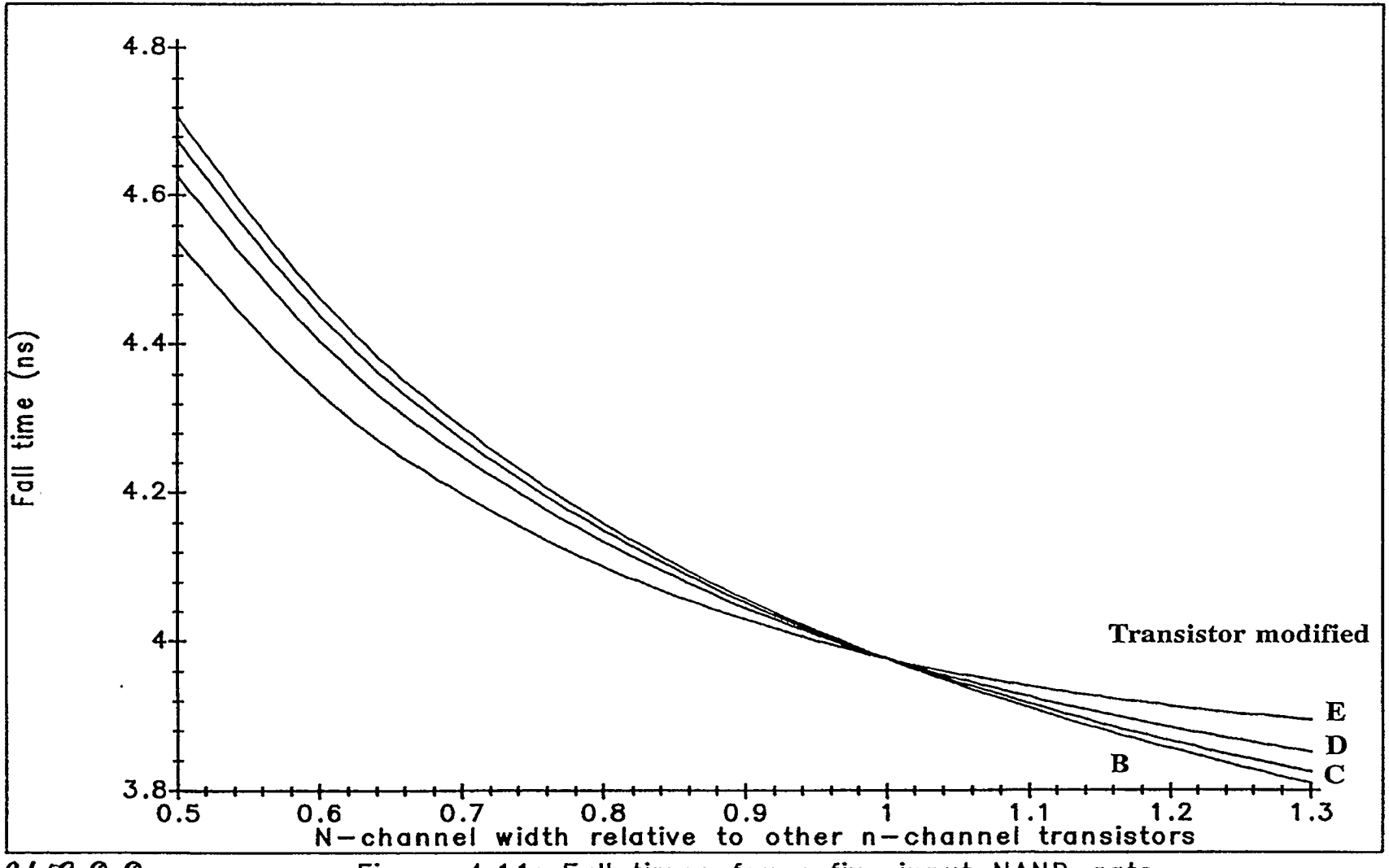


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Figure 4.11: Fall times for a five input NAND gate

transistors should not increase as one moves from the source transistor along the chain. This is the same conclusion drawn by Shoji [42]. As the plot shows only marginal improvement for an increase in device size and little difference between curves, for any given NAND gate all series transistors were assigned approximately the same channel width.

The fourth and final stratagem entails the use of a progressively smaller transistor ratio as the chain length increases. Although all transistors in a chain will have the same channel width, larger channel widths are afforded cells with longer chains. The range of transistor ratios used spans from 1.8 for a 2-input NAND to 1.2 for a 6-input NAND.

4.4.3 AND gates

Three AND gates have been designed; from two to four inputs inclusive. All cells evolved from their NAND counterparts and are succeeded logically by an inverting stage. The inverting stage was modelled after a medium-drive inverter. Common NAND/inverter sources were applied to conserve area.

4.4.4 NOR gates

Five different NOR gates have been designed; from two inputs to six inputs inclusive. Common practice dictates that cells have parallel n-channel transistors

and a series p-channel chain. As with the NAND gates, the presence of the series chain necessitates scrutiny of the design process. The remainder of this section is an abbreviated and complementary form of section 4.4.2.

Attempts have been made to minimize internal capacitance via S/D area reductions in the chain. Cascaded versions (for example Figure 4.13) of conventional designs (Figure 4.12) were forgone. Simulations resembling those used in generating Figure 4.11, were performed to obtain the rise time curves in Figure 4.14. Here we find that the differences in curve location to be much more dramatic. Also, we can see that for transistor *E*, increasing the channel width actually has an adverse effect on rise time. Channel widths were enhanced for transistors near the source. Unfortunately, though we would have preferred to have used a progressively larger transistor ratio for longer transistor chains, this was precluded by well height. The average transistor ratio used for all cells was approximately 1.9.

4.4.5 OR gates

Three OR gates have been designed; from two to four inputs inclusive. Like the AND gates, all cells evolved from their NOR counterparts and are succeeded logically by an inverting stage. The inverting stage is modelled after a medium-drive inverter. Common NOR/inverter sources have been applied to conserve area.

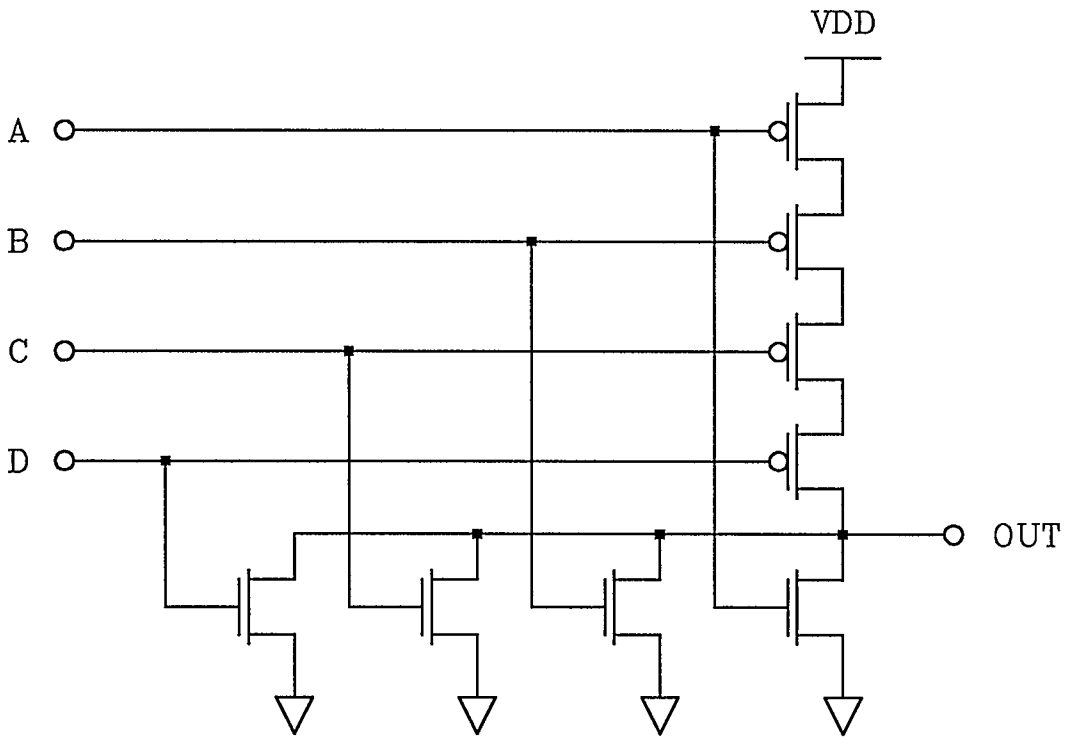

Figure 4.12: Conventional four input NOR gate

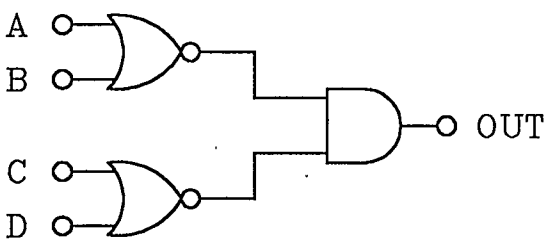

Figure 4.13: Four input NOR gate using cascaded logic

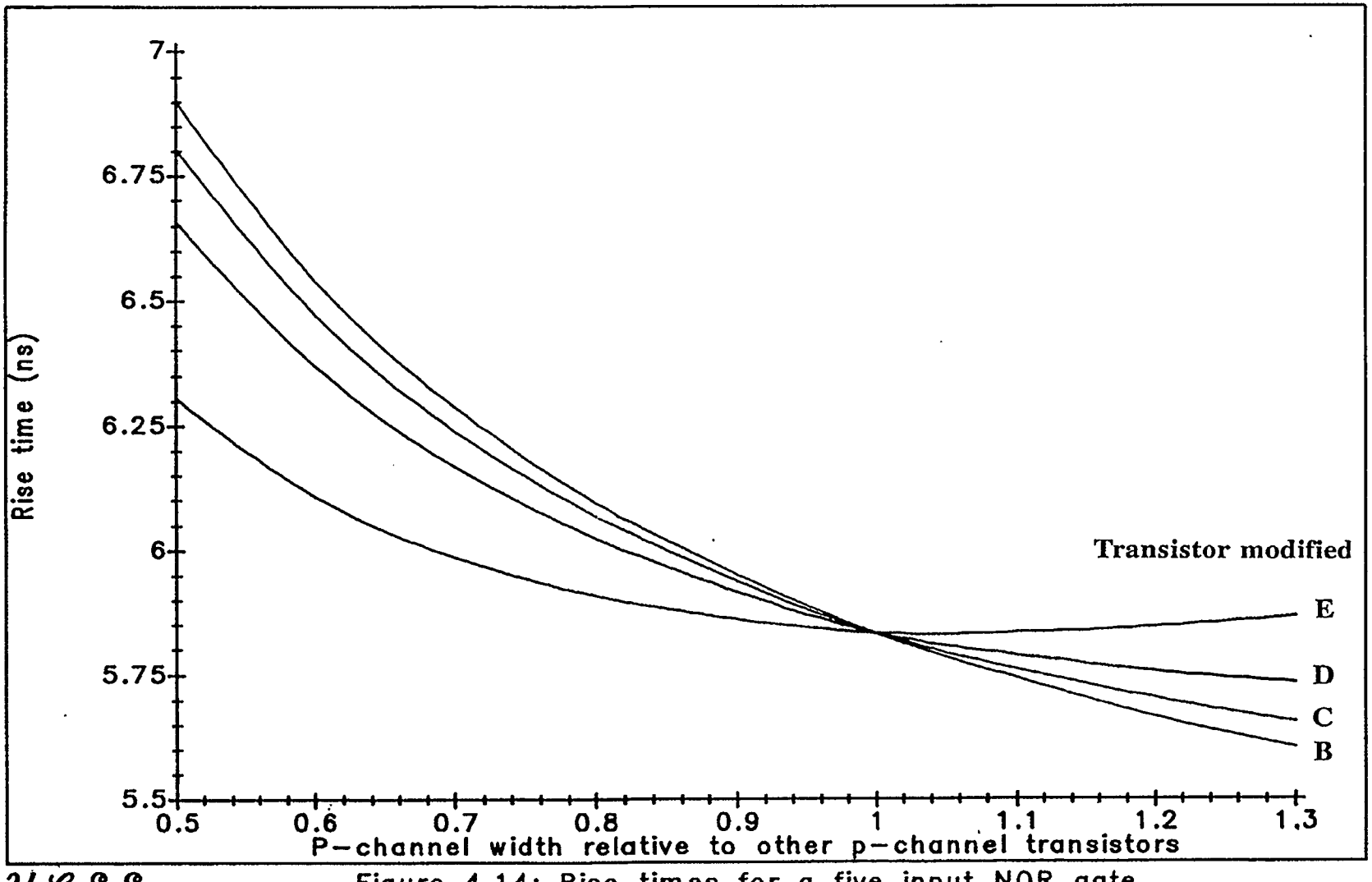

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Figure 4.14: Rise times for a five input NOR gate

4.4.6 XOR gate

A single two-input XOR gate has been designed. Several logical equivalents were available, the simplest of which is shown in Figure 4.15. Essentially, this is an inverter with two pass transistors. As such, the design is extremely poor since it is not fully restoring when input A is low. Also note that when B is low, the input A becomes a source for the output; the cell is incapable of properly driving a full load and therefore violates one of our library specifications.

A slight variation of this design is shown in Figure 4.16. Here, the addition of a transmission gate helps to reduce the threshold voltage drops incurred when A is low, but in doing so input B becomes a source for the output. As such, this design also has poor drive capability and was rejected.

Alternate schemes using pass transistors are shown in Figures 4.17 and 4.18. As with the other designs shown thus far, criticisms are non-restoring logic and/or poor drive capability.

A better scheme employing cascaded logic is given in Figure 4.19a. Sixteen transistors can be used in implementation. If, however, the OR and the AND gate are logically collapsed, the twelve transistor structure in Figure 4.19b is obtained.

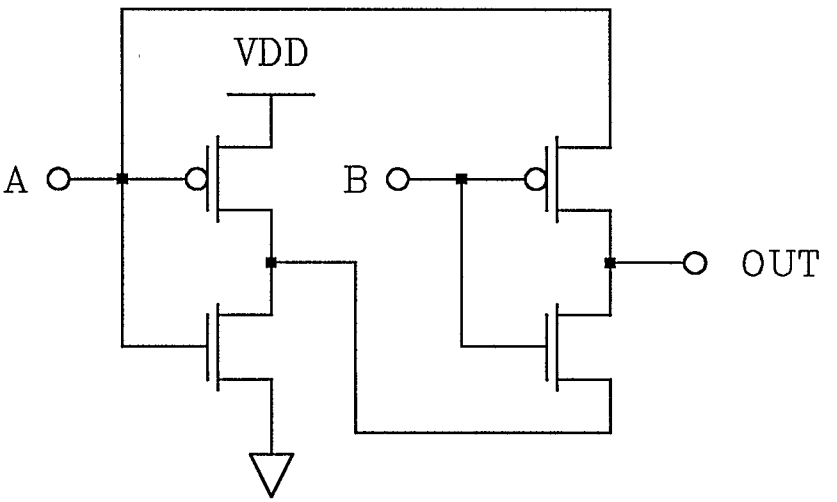


Figure 4.15: Simple two input XOR gate

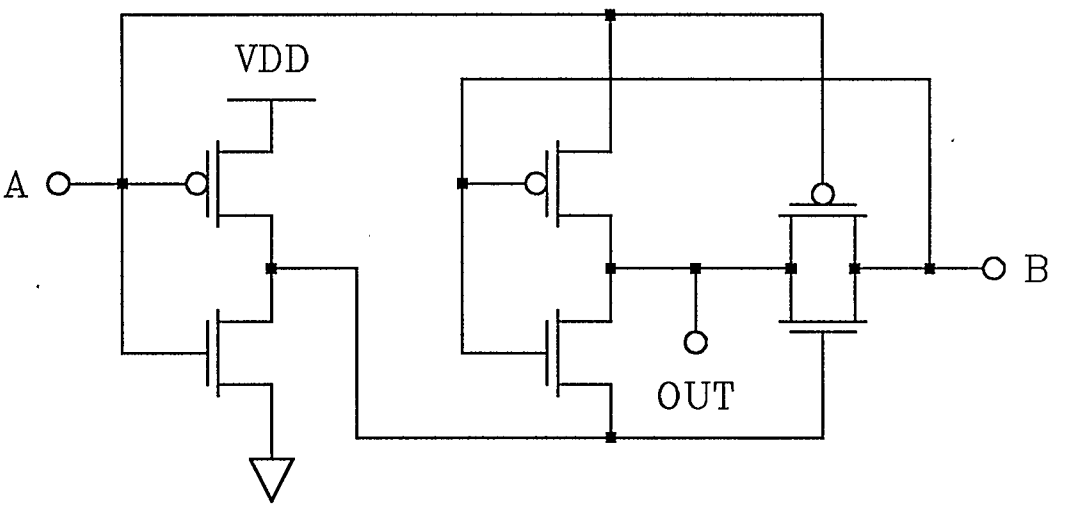


Figure 4.16: Simple two input XOR gate with a transmission gate

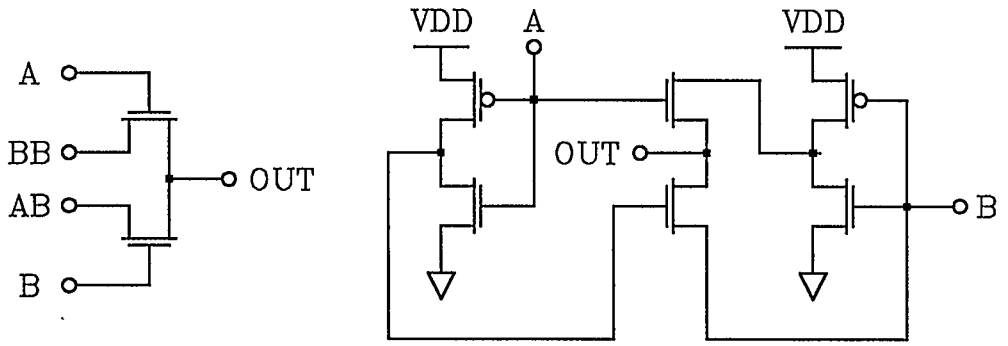


Figure 4.17: Two input XOR gate with pass transistor output

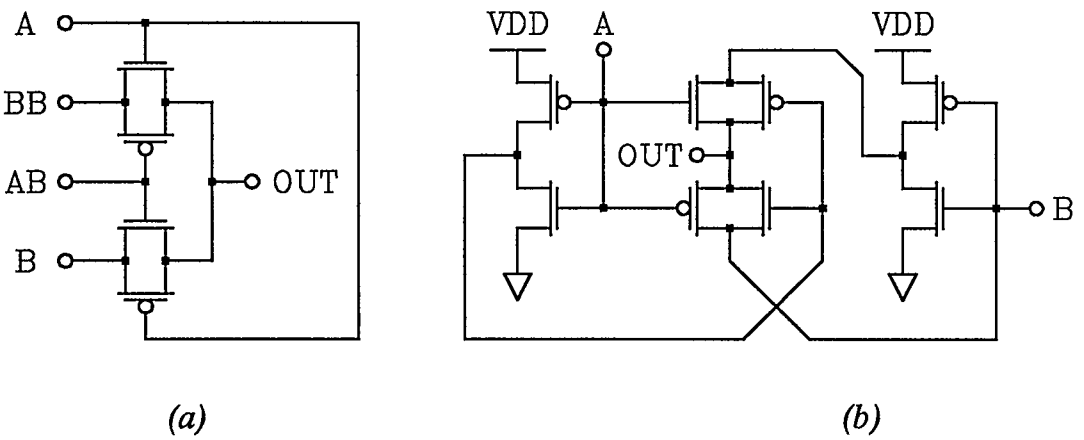
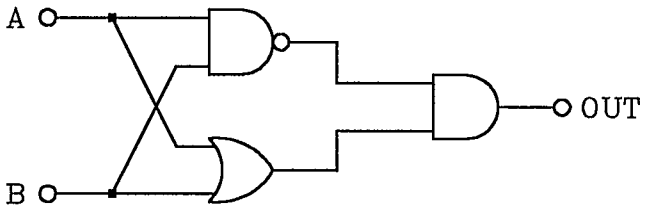
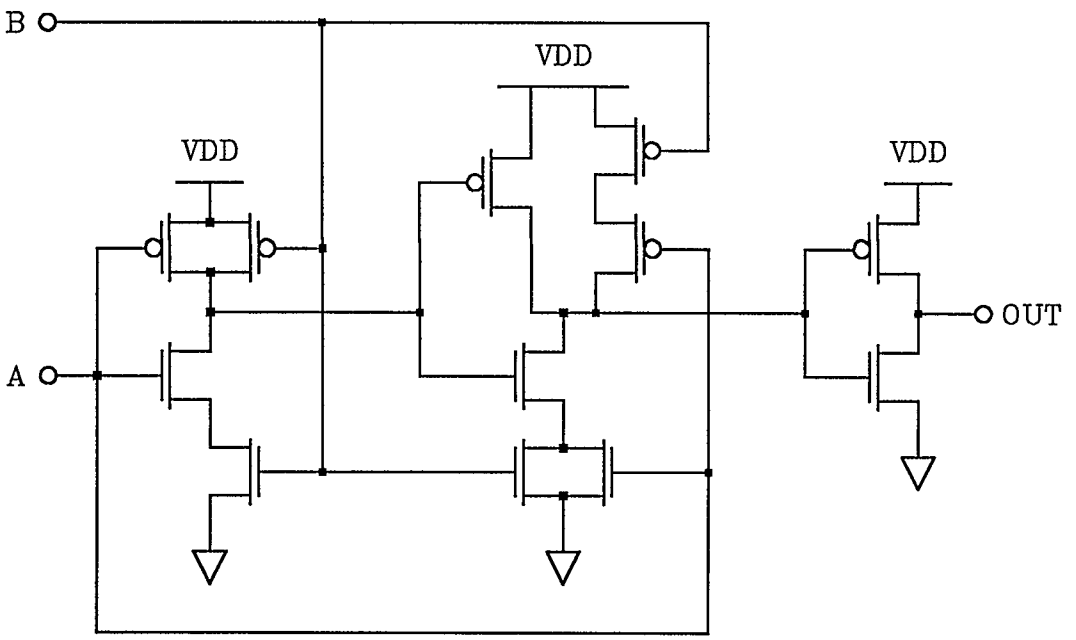


Figure 4.18: Two input XOR gate with transmission gate output



(a)



(b)

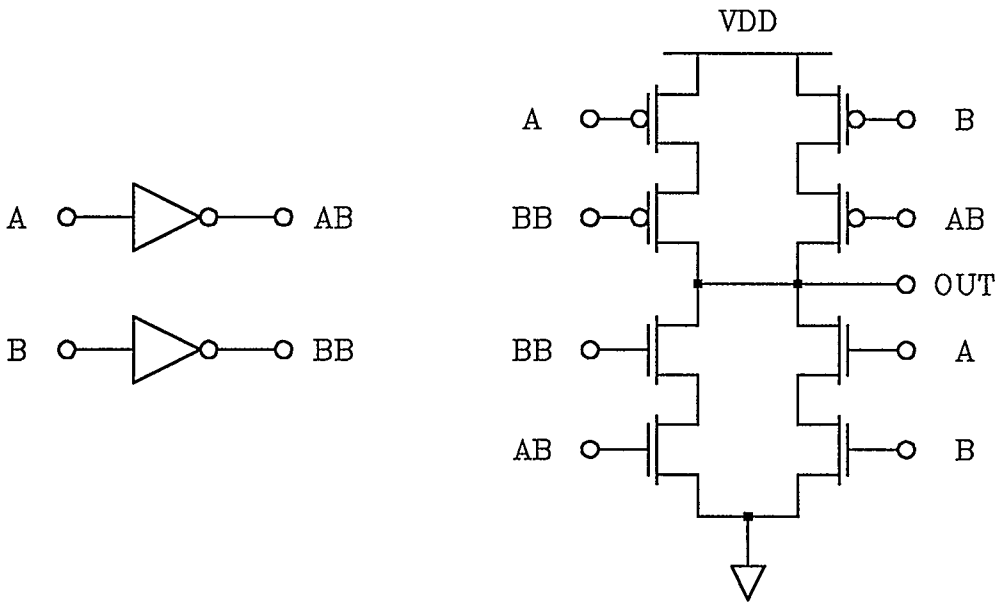
Figure 4.19: Two input XOR gate based on cascaded logic

Another twelve transistor design (refer to Figure 4.20) was accepted for layout. While the problems inherent in Figures 4.15 through 4.18 could have been alleviated by the addition of a buffering output stage, they were still avoided. Also, though probably no better than the design in Figure 4.19, it was chosen solely because it had already been endorsed by some vendors. The inverters are medium-drive and have a transistor ratio of about 1.6 while the random logic of the XOR uses a ratio of approximately 2.2.

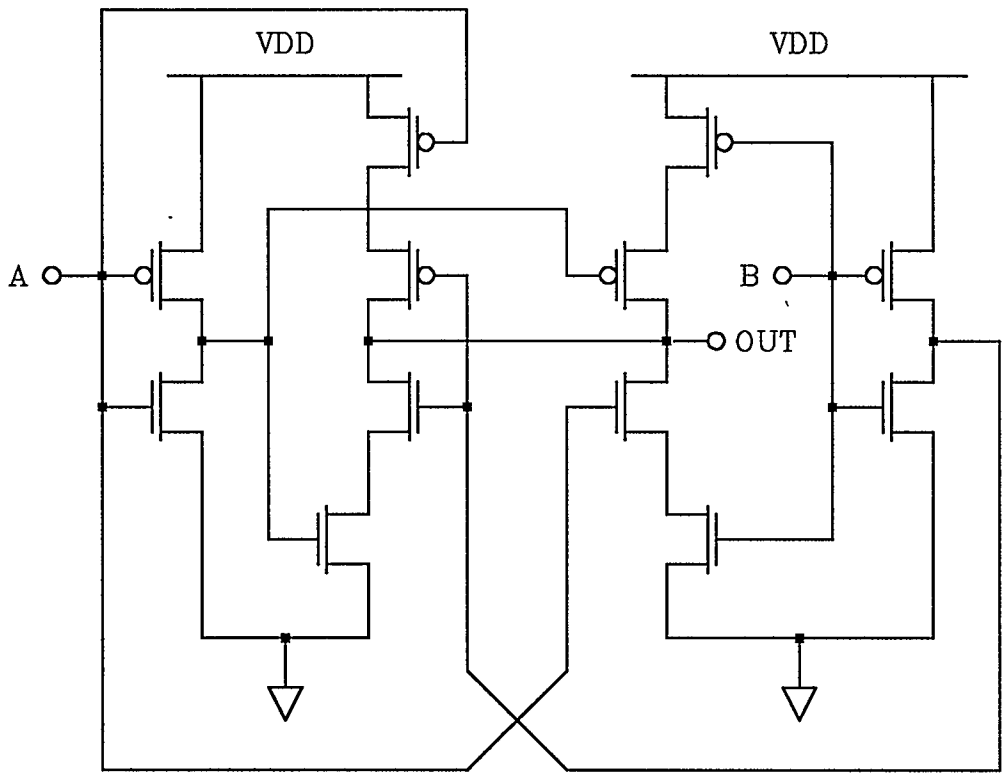
4.4.7 XNOR gate

Like the XOR cells, only a single two-input device has been designed. And although complementary forms of Figures 4.15 through 4.19 may be generated, their inclusion is merely academic. Figure 4.21 shows the transistor-level schematic of the XNOR gate. The inverters are medium-drive but due to internal routing constraints, both they and the random logic have a transistor ratio of about 1.5.

Note that because of the differences between the XOR and XNOR schematics, the XOR gate had to be basically designed from scratch. In this respect, perhaps it would have been better to implement the XOR gate based on Figure 4.19 as the XNOR could have been quickly realized via removal of the inverting output stage.

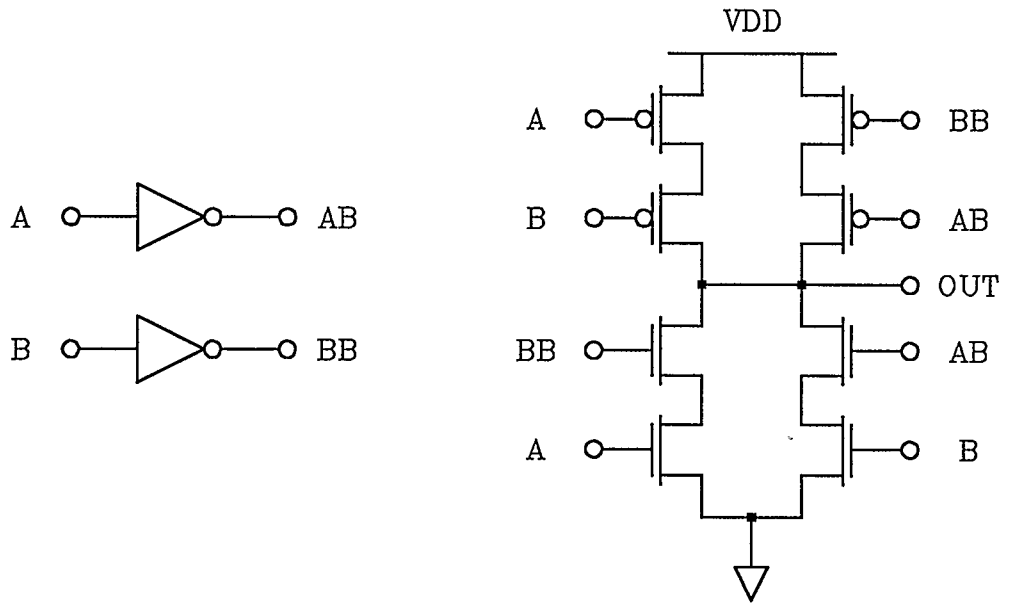


(a)

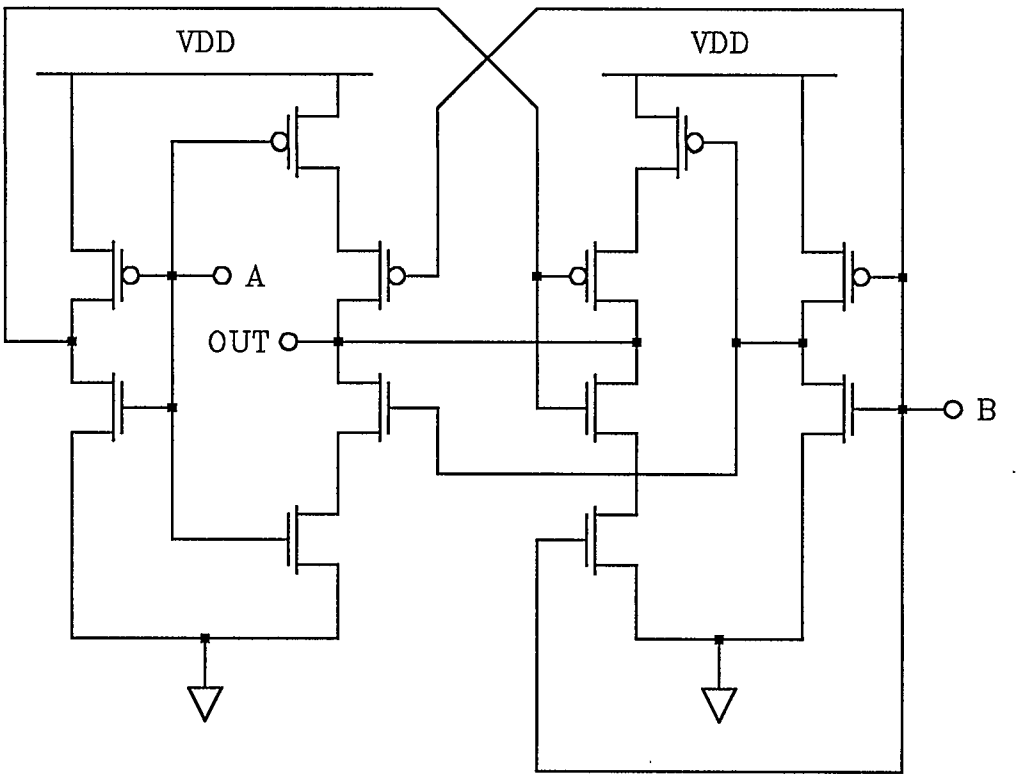


(b)

Figure 4.20: Actual implementation of a two input XOR gate



(a)



(b)

Figure 4.21: Actual implementation of a two input XNOR gate

4.4.8 Transmission gates

Three transmission gates have been designed; one requiring both an enable and its complement (Figure 4.22), one with an active-high enable (Figure 4.23), and one with an active-low enable (Figure 4.24).

These cells are the only ones in the library which violate the constraint of fully-restoring logic. Dependent on the loading conditions, cells may be succeeded logically with either a medium-drive or large-drive buffer (section 4.4.12) if required.

The inverters in Figures 4.23 and 4.24 are medium-drive. As the nature of the cell does not promote the use of large devices, transmission gate transistors have channel widths about one half the size of their medium-drive counterparts.

4.4.9 D-type latches

Twelve different D-type latches have been designed. Cells may be categorized as latching on either the positive or negative clock edge. Further, a cell may have a latched output, *Q*, an inverted output, *QB*, an active-low reset, *RB*, or any combination thereof. Table 4.3 lists all cells and their attributes.

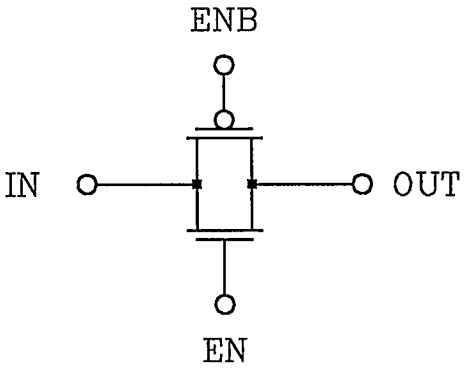


Figure 4.22: Transmission gate requiring both an enable and its complement

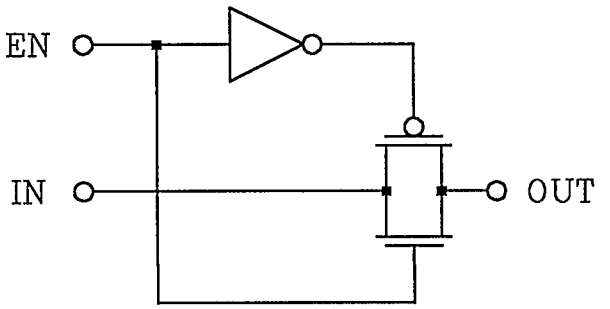


Figure 4.23: Transmission gate with an active high enable

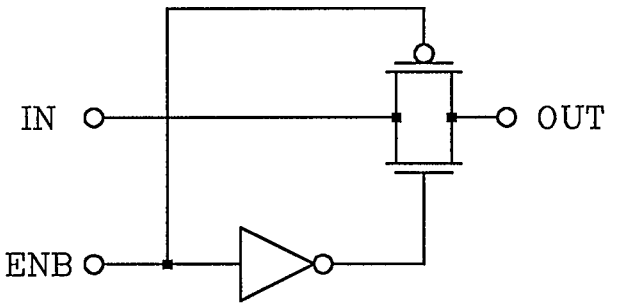


Figure 4.24: Transmission gate with an active low enable

Table 4.3: Latches and their attributes

	Q	QB	RB	latching edge
latch1	Y			-
latch2	Y		Y	-
latch3	Y	Y		-
latch4	Y	Y	Y	-
latch5		Y		-
latch6		Y	Y	-
latchA	Y			+
latchB	Y		Y	+
latchC	Y	Y		+
latchD	Y	Y	Y	+
latchE		Y		+
latchF		Y	Y	+

Figure 4.25 shows *latch1*. Note that in the design, a pair of transmission gates is used to control cell operation. In practice, only one transmission gate is needed if the drive of one inverter in the feedback loop is sufficient enough to overwhelm the other. Latches implemented in this fashion are commonly referred to as high-impedance designs. Figure 4.26 shows the high-impedance equivalent of *latch1*. None of the latches in the library are high-impedance as the author regards any strategy promoting contention as dangerous.

Features such as the inverted output, reset, and positive-edge latching are all illustrated in Figures 4.27, 4.28, and 4.29 respectively. Together with Figure 4.25, a schematic for any of the latches may be easily composed by superimposing desired attributes.

All devices in the latches are medium-drive except for the transmission gate transistors which are considerably smaller. Because of the logical flow within each cell, several common sources and drains were implemented.

4.4.10 D-type flip-flops

Eight different D-type flip-flops have been designed. All cells have been assembled from D-type latches and are designed to store the input on the positive clock edge. Various cell attributes include an output, *Q*, inverted output, *QB*, an active-low reset, *RB*, and an active-low set, *SB*. Table 4.4 shows existing cell

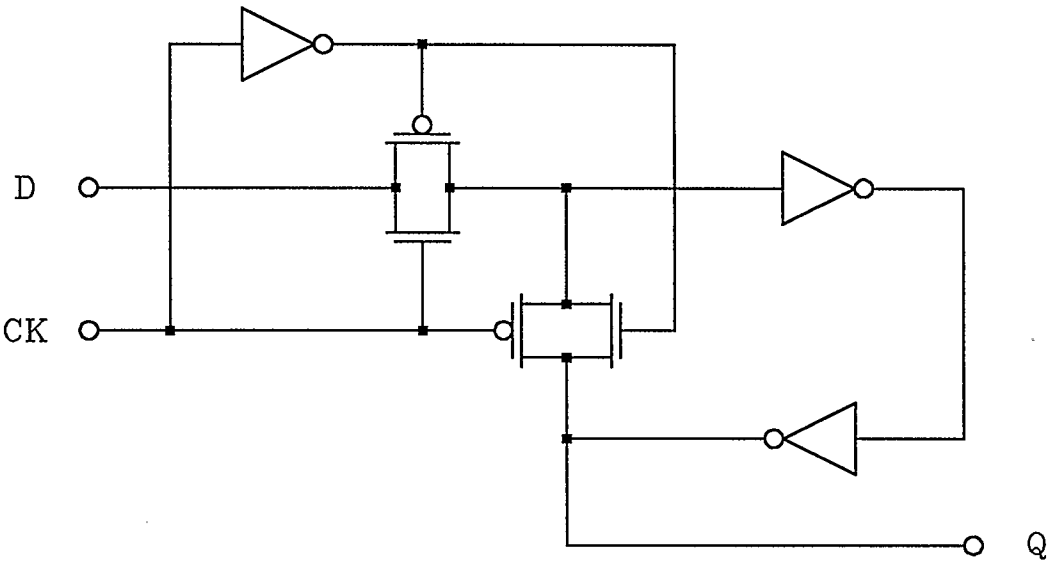


Figure 4.25: Simple D-type latch

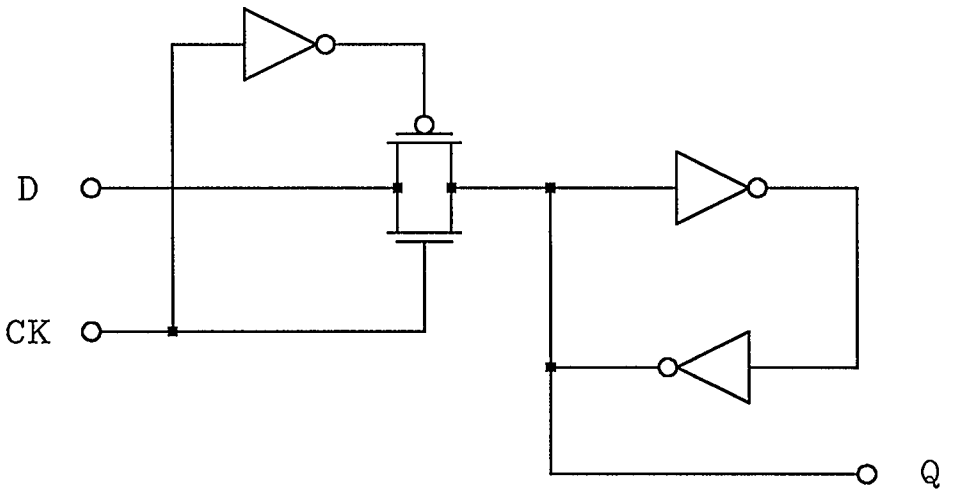


Figure 4.26: High-impedance version of a simple D-type latch

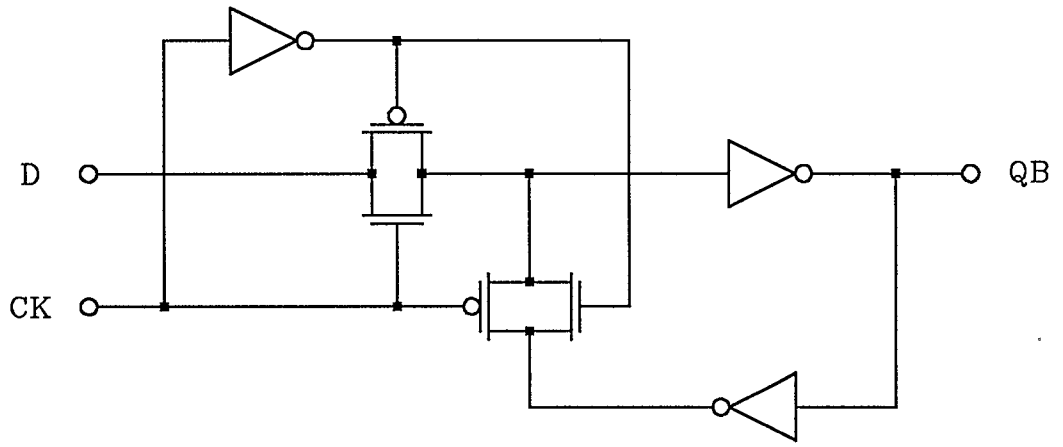


Figure 4.27: Simple D-type latch with an inverted output

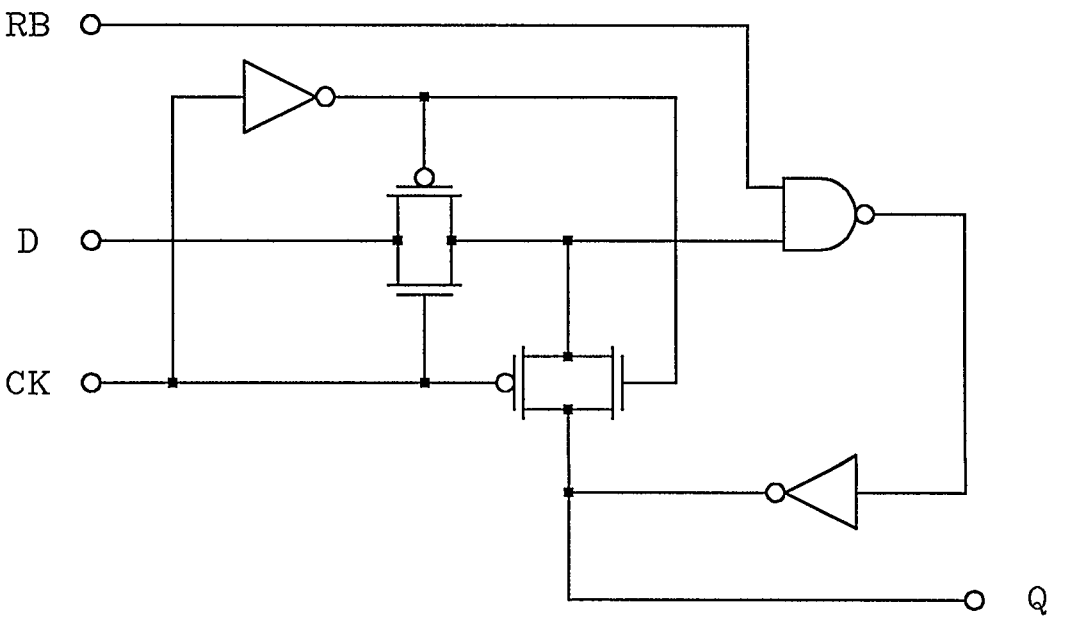


Figure 4.28: Simple D-type latch with an active low reset

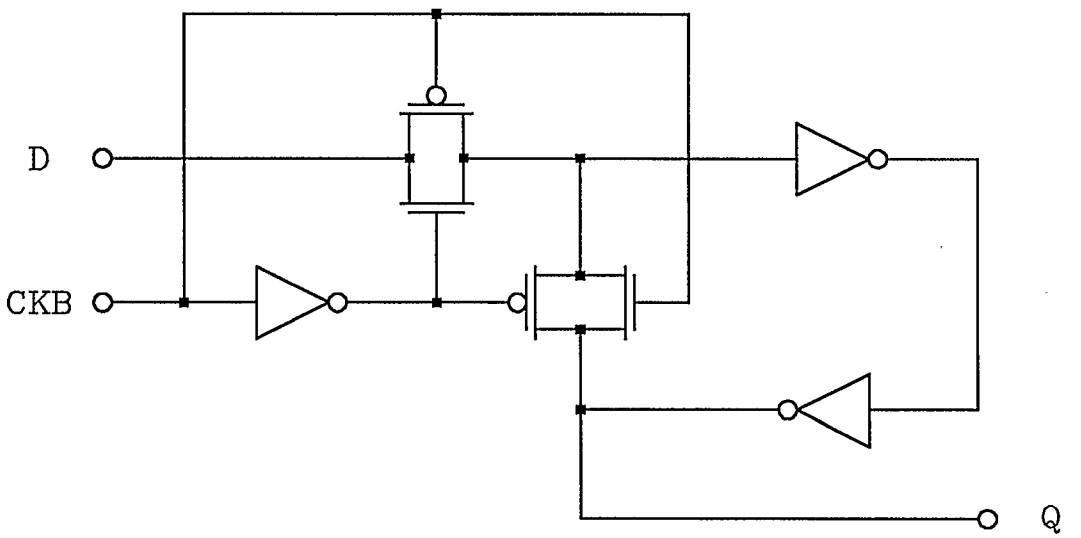


Figure 4.29: Simple D-type latch with capture on the positive edge of CKB

Table 4.4: D-type flip-flops and their attributes

	Q	QB	RB	SB
dflop1	Y			
dflop2	Y		Y	
dflop3	Y			Y
dflop4	Y		Y	Y
dflop5	Y	Y		
dflop6	Y	Y	Y	
dflop7	Y	Y		Y
dflop8	Y	Y	Y	Y

characteristic combinations.

Schematics span a range of complexity from that of *dflop1* (Figure 4.30) to that of *dflop8* (Figure 4.31).

4.4.11 RS-type flip-flop

In the development of the RS flip-flop, one has the option of designing a cell with active-high set and reset (Figure 4.32) or active-low set and reset (Figure 4.33). Only the latter has been implemented. Both NAND gates are medium-drive and share a common source.

4.4.12 Two-stage clock buffers

Four buffers have been designed; two of these are medium-drive and the other two are large-drive. All cells supply a fully buffered output and have been realized via two cascaded inverting stages. Further, one of the medium-drive cells and one of the large-drive cells provide the intermediate signal or inverted output.

Medium-drive buffers, of course, have been developed using two medium-drive inverters, whereas large-drive buffers entail two large-drive inverters. In the case of the large-drive buffer without the inverted output, use of a leading large-drive inverter was actually unnecessary. A medium-drive inverter would suffice and

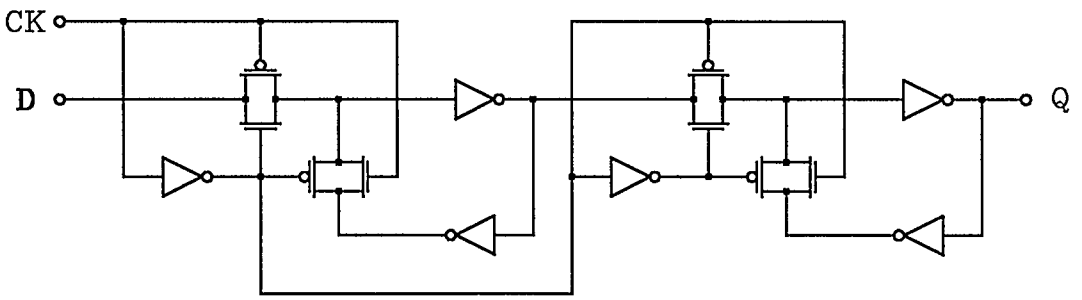


Figure 4.30: Simple D-type flip-flop

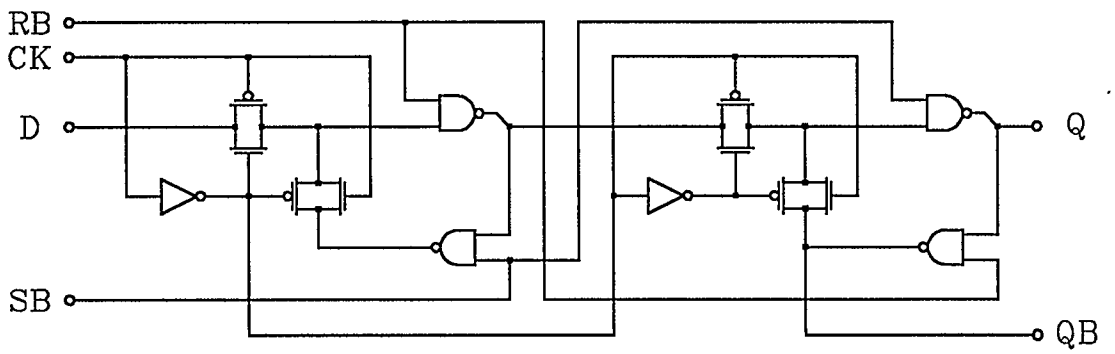


Figure 4.31: D-type flip-flop with active low set and reset

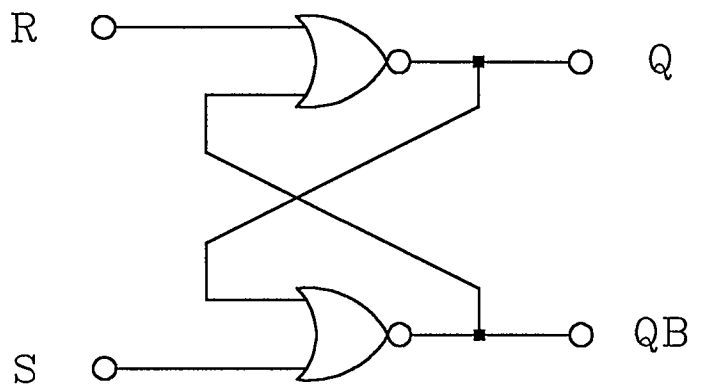


Figure 4.32: RS flip-flop with active high inputs

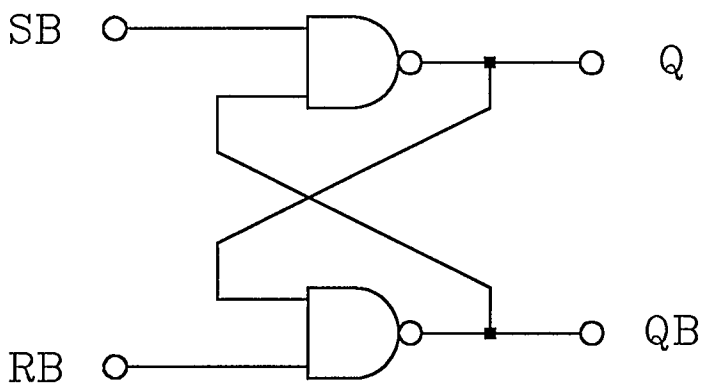


Figure 4.33: RS flip-flop with active low inputs

would also lower the input or gate capacitance.

All large-drive inverters have been realized by connecting two medium-drive inverters in parallel. Here, a common drain reduces output capacitance. In all cells, inverting stages have been grouped to minimize cell area through common sources.

4.4.13 Tri-state buffers

Four different tri-state buffers have been designed; two of these operate with an active-high enable (Figure 4.34) while the other two use an active-low enable (Figure 4.35). Both enable schemes have one cell with a medium-drive output stage and one with a large-drive output stage.

The enable inverter, NAND, and NOR gate in each design is medium-drive. Further, in all designs the inverter and NAND gate share common sources as do the NOR gate and output stage.

4.4.14 Multiplexer

Only a single two-input multiplexer was designed. Translating a Karnaugh map to a transistor-level schematic yields Figure 4.36. A silicon realization of this design would be similar to that of either the two-input XOR gate or the two-input XNOR gate. As internal routing made both of these cells challenging to design,

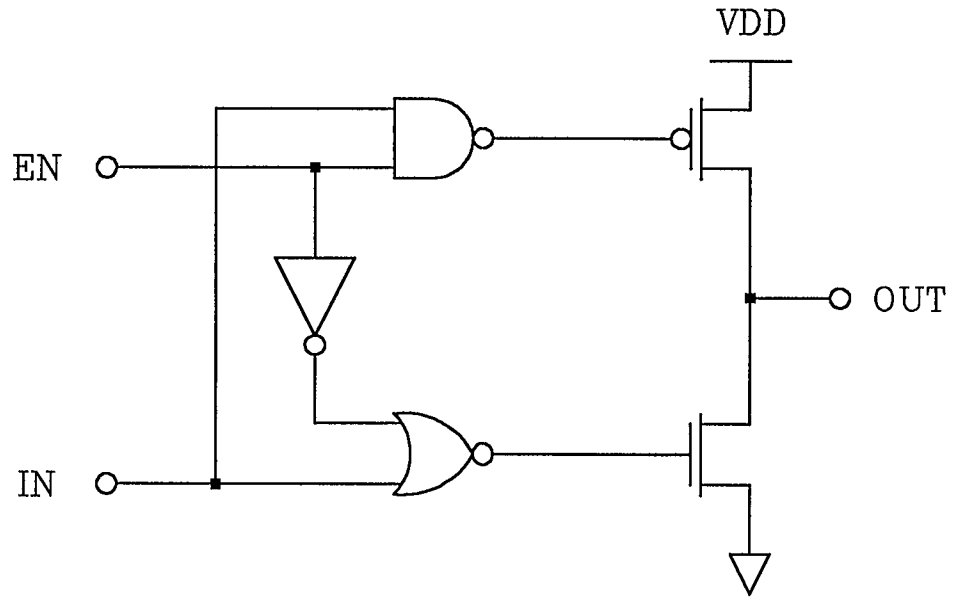


Figure 4.34: Tri-state buffer with an active high enable

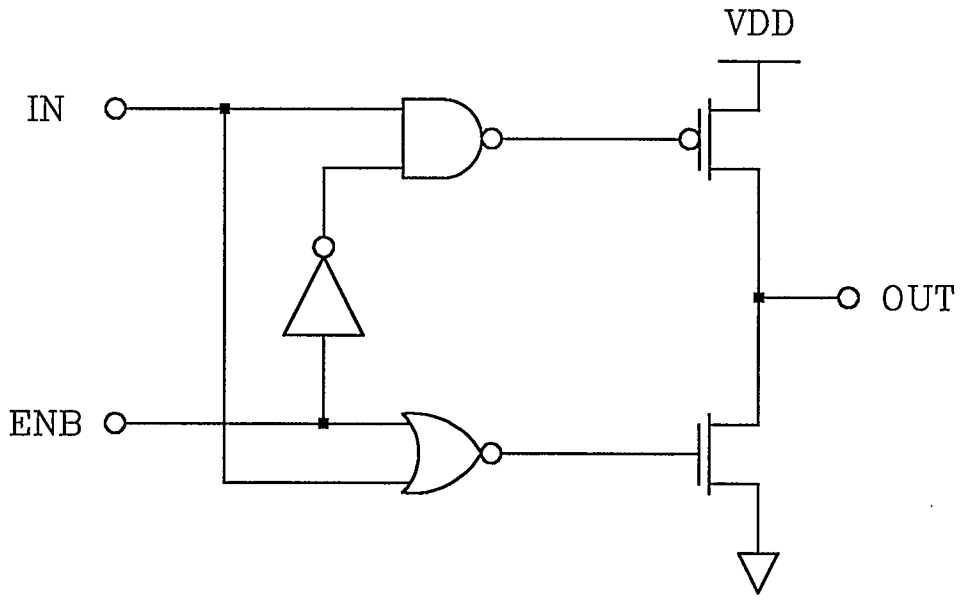


Figure 4.35: Tri-state buffer with an active low enable

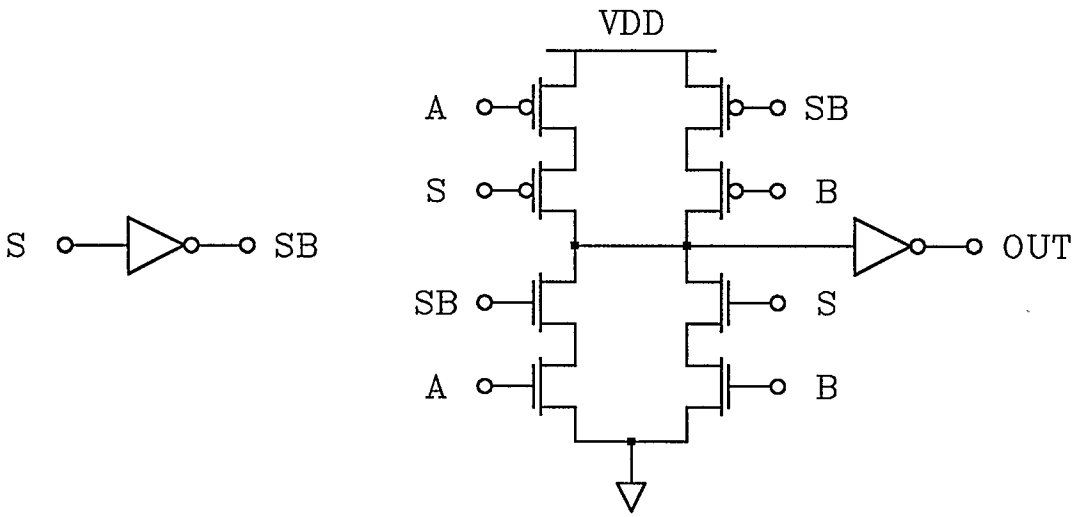


Figure 4.36: Random logic implementation of a two input multiplexer

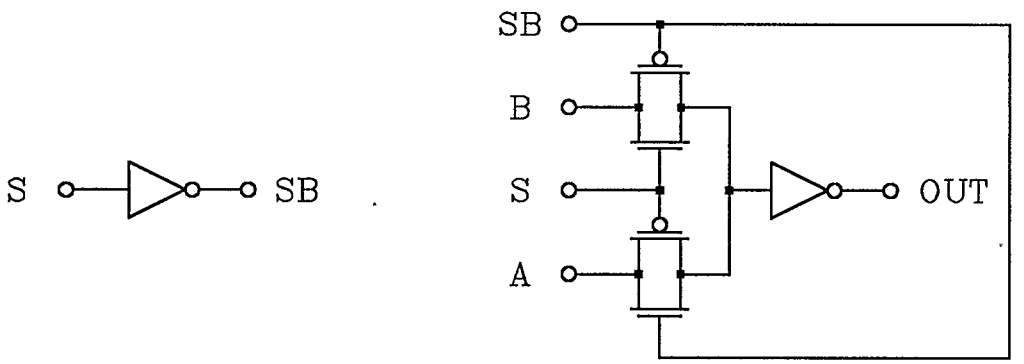


Figure 4.37: Transmission gate implementation of a two input multiplexer

there was no desire to repeat the exercise. Rather, the transmission gate implementation in Figure 4.37 was selected.

All inverters are medium-drive and have device sizes much larger than those of the transmission gates. Because the cell is fully buffered, inputs A and B experience no greater load than the D input of a D-type latch or D-type flip-flop.

4.4.15 Feedthrough

The feedthrough cell is nothing more than a second-level metal feedthrough path and a pair of large substrate contacts.

4.5 Library simulation

For this section, the text has been logically partitioned into subsections for clarity. To begin, we elaborate on the simulation environment. Then. we discuss simulation as it relates to body effect. The loading conditions used and the input waveforms are then described. Finally, we discuss the simulation results found in Appendix C.

While it would have been interesting to have considered classic simulation variables such as temperature and supply voltage, we were bound by time. All

simulations in this thesis have been performed assuming nominal ambient temperature and a supply of precisely five volts.

4.5.1 Simulation environment

In the generation of the simulation environment, there were three tasks to perform. Firstly, transistor models had to be created for use by SPICE. Secondly, LPE had to be configured. Lastly, the actual value of a unit load had to be calculated.

At the beginning of this chapter it was mentioned that the library has been designed with three N-well and two P-well processes in mind. For each of these processes, we had at our disposal a vendor document detailing, among other things, parasitic interlayer capacitive values and level two SPICE modelling parameters. One of the N-well process documents actually provided two sets of SPICE parameters; one parameter set pertained to fabrication runs yielding fast devices and the other to runs yielding slow devices. One of the P-well process documents included three sets of SPICE parameters - sets for fast, slow, and average device runs. Effectively then, whenever simulations were performed they were done using eight different transistor models.

LPE is configured by supplying it with interlayer capacitive values. These values are all area-based and are used to calculate the parasitic capacitance arising

from the overlap of two unconnected layers. LPE was not configured on a per process basis as this would have entailed an enormous amount of computation. Rather, all process descriptions were compared and the highest parasitic parameters collected.

For any given cell, LPE is executed four times; once to extract gate and I/O loading information assuming an N-well process, once to extract P-well loading information, once to assemble a SPICE deck assuming an N-well process, and once to assemble a P-well SPICE deck. If LPE were configured on a per process basis, this would increase the computational burden by a factor of eight.

To determine the exact value of a unit load, LPE was applied to a complete two input NAND gate with seventy horizontal pitches of metal interconnect. This produced

$$C_U = 0.149609\ pF$$

It is understood that using the largest available capacitive values within LPE results in parasitic capacitances and a unit load greater than actual for some processes. Ramifications include slower than actual simulation times. However, it is decidedly better to be conservative in any simulation analysis.

4.5.2 Simulation and body effect

What we are actually interested in, when we simulate a cell, is the combination of inputs which will produce the slowest simulation times. For cells having several inputs and a series transistor chain, two avenues exist. The first is to exhaustively simulate the cell for all input combinations. A far superior method takes advantage of body effect.

As an example, consider the four input NAND gate in Figure 4.9. The slowest fall time and falling propagation delay time must occur when the cell has to discharge not only the load but all S/D areas within the series n-channel chain. Since all four p-channel transistors are connected in parallel, slowest rise and rising propagation delay times result when the cell must charge the load and all S/D areas in the n-channel chain through a single p-channel transistor. Waveforms which realize this scenario are given in Figure 4.38. Note that what we have actually done is converted the cell operation from a four input NAND to an inverter. For a NAND gate of any length, limiting simulation times may be found by tying all inputs to the supply except the one whose n-channel drain is grounded.

For a NOR gate of the same length, we simply invert the logic. All inputs are grounded except for the one whose p-channel drain is connected to the supply (see Figure 4.39).

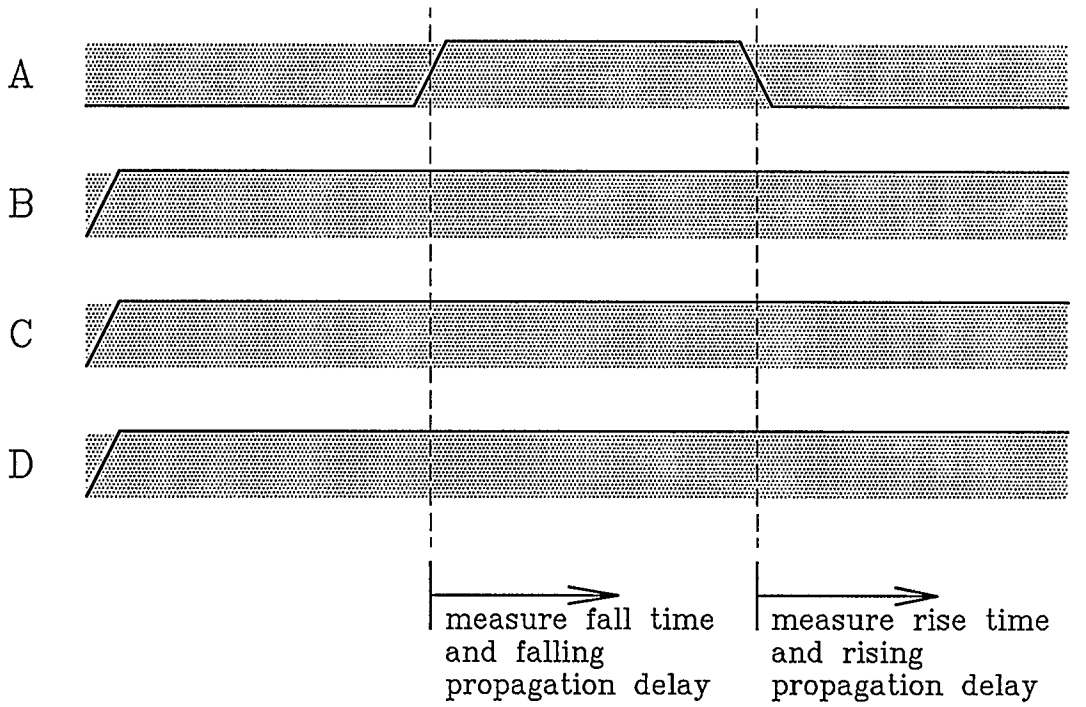


Figure 4.38: Simulation vectors for a four input NAND gate

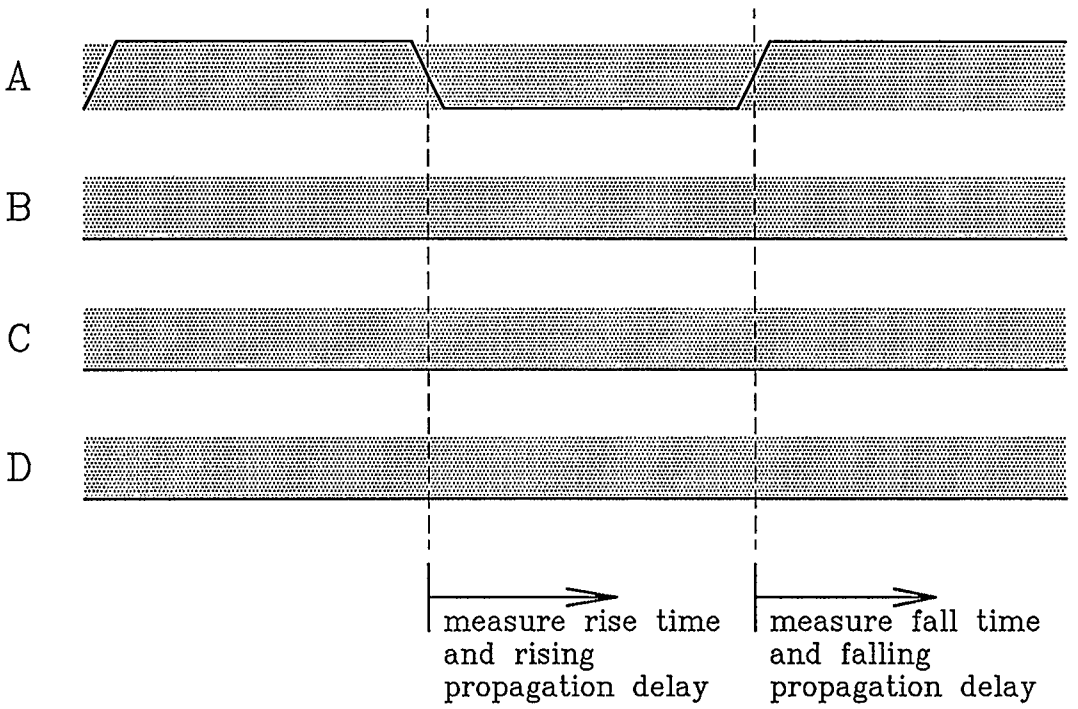


Figure 4.39: Simulation vectors for a four input NOR gate

As an extension of this simulation strategy, if one of the transistors in a series chain is driven by an enable line - or something which rarely changes state - then it is best if its drain is connected to either ground (n-channel) or the supply rail (p-channel).

4.5.3 Loading conditions and input waveforms

As mentioned earlier in the thesis, we have defined a full load to be a fanout of four. Using a unit load to translate half, full, and double loads to absolute values:

$$C_H = 0.299218\ pF$$
$$C_F = 0.598436\ pF$$
$$C_D = 1.196872\ pF$$

There are five cells which have been designed with high-power output stages. These are by name *invl*, *buf2*, *buf4*, *tri2*, and *tri4*. For these cells a double load is used in lieu of a full load and a full load is used in place of a half load when simulating.

In the introduction, it was stated that *15 MHz* operation was desired given four asynchronous devices between synchronous ones and with each device driving a full load. Consider that if two phase design is employed, then each cell must promise propagation delay less than

$$T_{Plim} = 1 / [(15\ MHz)\ (2\ phases)\ (4\ cells)] = 8.33\ ns$$

Further, to some extent simulation times are dependant on the speed at which inputs change state. That is, the slower an input switches, the slower the resulting times. For operational verification, we switch cell inputs at a relatively slow *10 ns* ramp time. Resulting cell rise and fall times should be no slower.

While a full load and *10 ns* input ramps may suffice for cell verification, they are not indicative of how each cell will behave given different load or input conditions. Accordingly, four complete sets of simulations have been performed. These entail

- a full load and *10 ns* input ramps
- a full load and *5 ns* input ramps
- a half load and *5 ns* input ramps
- a half load and *3 ns* input ramps

When compounded with the eight different transistor models we are simulating with per cell, the amount of data generated becomes somewhat unwieldy. Therefore, in Appendix C, for each set of load and input conditions, two documents have been prepared. One of these contains the worst simulation times of the eight transistor models and the other holds an average time calculated from the eight transistor model simulations.

From the documents in Appendix C it should be clear that virtually any load and input conditions may be estimated using extrapolation.

4.5.4 Simulation results

Examining the worst transistor model simulation times for a full load and *10 ns* input ramp time, there are some criticisms that can be made regarding each cell or cell class. For example, if the rise and fall time for a cell are mismatched, as is the case for *nand6*, then this is indicative of an error in the transistor ratio. Ideally, these times should be identical but in some cases the ratio cannot be adjusted to correct the situation because of some layout related problem such as insufficient cell height.

All cells seem to meet specification (rise and fall times less than *10 ns* and propagation delay times less than *8.33 ns*) except *nor4*, *nor5*, and *nor6*. Perhaps these cells should have been designed using cascaded logic. If these cells are to be used in any time critical path, the author can only suggest the use of an output buffer to reduce load requirements.

Chapter 5

Library Comparison

5.1 Introduction

In any field where there is precedent, merit can only be truly evaluated through comparison with similar works. Our library is no exception to this maxim. To ascertain fully how our library compares to other libraries on the market, both physical (cell height, horizontal pitch) and electrical (propagation delay, maximum D-type flip-flop toggle frequency) properties must be considered. To facilitate comparison, relevant values pertaining to two-micron double-level metal CMOS cell libraries have been procured from [20, 13] and documentation from various vendors.

This is by no means an exhaustive comparison but should still suffice. Benchmarks such as the sheer number of cells per library would not be fair as time restrictions have precluded extensive library development. The remainder of this chapter presents, *paucis verbis*, results and particulars of the comparison.

5.2 Comparison Details

Physical properties are simple to contrast as geometric characteristics are not subject to interpretation or easily misconstrued; they just are. Electrical properties, on the other hand, are not easily compared. As integrated circuits produced using our library can be fabricated by several different vendors, it should be apparent that transistor models, and therefore device behaviour, may vary from process to process. So not only will propagation delay and toggle frequency be a function of load and the shape of the input waveform, but in our case process as well.

To limit the number of variables present in propagation delay, a two-input NAND gate was used to represent each library. The load was set identically to a fanout of *2* with a *1 mm* length of metal interconnect. Also, for our library all processes were simulated and the average calculated. With these constraints, the only unknown remaining was the shape of the input waveform. Few vendors disclosed their input waveform shape; in all likelihood a square wave was used. It seemed just, given the times tabled in Appendix C, to use a waveform with rising and falling edges represented by *3 ns* ramps.

Toggle frequency turned out to be the most difficult to compare as each vendor's toggle circuitry is undocumented; loading conditions and the number of asynchronous devices between flip-flops are unknown. A practical model suggested by Ian Roane [43] at NovAtel entails the placement of a three-stage inverter chain

between flip-flops (refer to Figure 5.1). In our analysis, the slowest D-type flip-flop in the library (largest internal capacitances due to set and reset transistors) was used. And again, the input waveform used by the vendors was unknown. Two different clocks were applied; a square wave and one having *3 ns* rising and falling edges. Resultant toggle frequencies are attainable by all processes.

Results of the comparison are shown in Table 5.1.

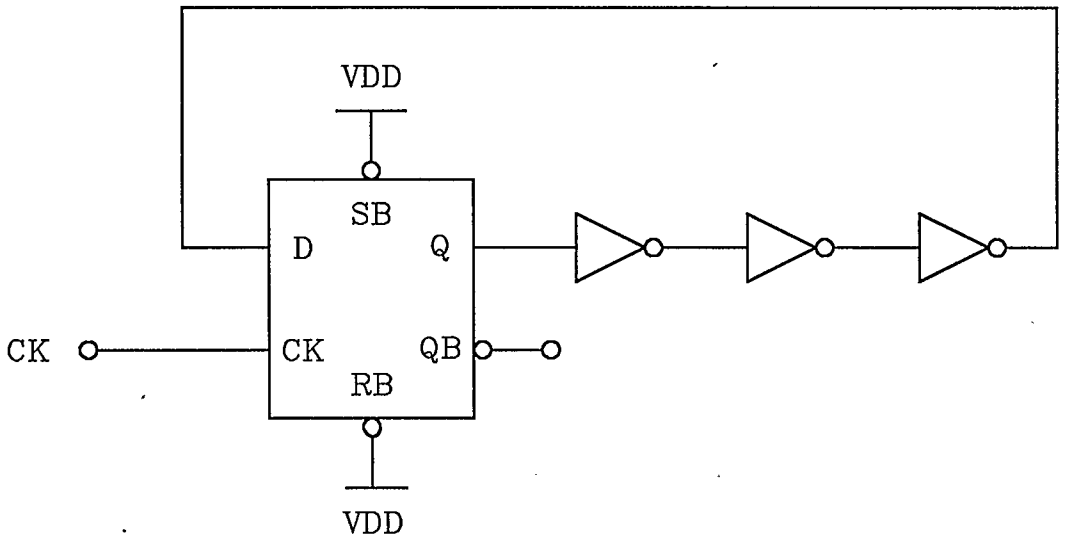


Figure 5.1: Maximum toggle frequency circuitry

Table 5.1: Library Comparison

	Generic cell	Vendor's composite	
		Number vendors	Average
Cell height	63.0 lambda	6	75.4 μm
Horizontal pitch	9.0 lambda	22	6.9 μm
Propagation delay	1.1 ns (3 ns ramp)	34	1.26 ns (unknown ramp)
Toggle frequency	147 MHz (3 ns ramp) 161 MHz (square clk)	34	80.6 MHz (unknown ramp)

Chapter 6

Conclusions

6.1 Accomplishments

To facilitate rapid design of VLSI systems, a limited double-level metal standard cell library has been developed. Unlike many libraries currently on the market, we have managed to incorporate powerful features such as longevity and vendor and process independence. Note that the last two of these features are in all likelihood not supported by any vendor.

The standard cell methodology for the library is based upon fixed height and variable width cells. Supply rails have a fixed width and are aligned with the top and bottom cell faces. All cell I/O are made available in second-level metal at both the cell top and bottom. Process independence is realized within the confines of the methodology through inclusion of both N- and P-well masks in layout.

The library was developed within a well-integrated CAE environment. Transistor-level schematics and symbolic schematics have been created to complement each layout. All cells have been verified using DRC, LVS, and simulation. In addition, place and route software allows system design to be performed at the symbolic level once library development is complete.

A set of design rules has been assembled which not only promotes longevity but also vendor independence. Horizontal pitch has been calculated based on the design rules. These design rules have also been coupled with noise margin, propagation delay, and metal migration analyses to yield other standard cell dimensions such as the cell height, supply rail widths, and individual well heights.

To date, fifty-four asynchronous logic gates, latches, flip-flops, signal conditioners, and multiplexers have been generated, verified, and characterized through simulation. As well, the latch-up phenomenon has been investigated and precautions have been taken in design to minimize the library's susceptibility.

Comparing our library to those on the market, simulations suggest that our library offers, on average, comparable or better performance, a smaller cell height, and a larger horizontal pitch. As a larger pitch does not necessarily imply a wider cell, cells should prove comparable or smaller in size.

6.2 Future work

The thesis content is basic yet broad enough that it affords future growth in any one of several different directions. Possibilities include cell design, cell verification, and systems design. Each of these points is addressed in turn.

Future work in cell design entails not only library expansion but also better optimization of existing cells. Though some optimization has been performed on each cell, there is still room for improvement. Recall that in the body of the thesis, individual designs were analyzed and criticized. In some cases, optimization will entail architectural change. Detailed measures should be taken to ensure that all cells attain both optimal performance and reliability.

Library expansion should be performed with a specific application in mind. For example, adders and multipliers for DSP. This is not to suggest that additional general purpose cells should not be designed but that future work should probably be more direct. The inclusion of analog cells should at some point be considered as should the development of I/O pads.

With respect to verification, perhaps a more rigorous characterization should be performed. The unit load and parasitic values should be reduced to the process-specific level. Also, temperature and power supply voltage analyses would be valuable. More importantly though, in the future, verification should extend beyond the realm of software. The relative worth of simulations only becomes apparent when compared with measured values. Circuitry capable of testing all library cells should be fabricated using more than one process line.

Lastly, the library has been designed using some operational specifications. It would be very interesting to see if fabricated systems function within these guidelines.

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APPENDIX A: Design rules

CMOS STANDARD CELL DESIGN RULES

all dimensions in lambda

1.	**N-well**	
	Twin-tub technology	
	a) min. spacing to P-well	5.5
	General	
	a) min. width	4.0
	b) min. spacing (different potential)	10.0
	c) min. overlap of Active	2.5
	d) min. distance to Active	8.0
2.	**P-well**	
	Twin-tub technology	
	a) min. spacing to N-well	5.5
	General	
	a) min. width	4.0
	b) min. spacing (different potential)	10.0
	c) min. overlap of Active	2.5
	d) min. distance to Active	8.0
3.	**Active**	
	a) min. width	3.0
	b) min. spacing of similar dopings	2.5
	c) min. spacing of N+ Active to P+ Active	4.0
	d) min. transistor width	3.0
4.	**Polysilicon**	
	a) min. width	2.0
	b) min. spacing	2.5
	c) min. transistor length	2.0
	d) min. extension of gate over Active	2.0
	e) min. extension of Active over gate	3.5
	f) min. spacing to related Active	0.5
	g) min. spacing to unrelated Active	1.0

CMOS STANDARD CELL DESIGN RULES

all dimensions in lambda

5. N+ (inclusive)

N-well substrate contacts (no splits)

a) min. overlap of Active by N+ in N-well (all sides)	0.0
b) min. spacing of N+ Active to P+ Active in N-well	0.0
c) min. spacing of N+ Active to Poly in N-well	1.5

General

a) min. width	3.0
b) min. spacing	3.0
c) min. overlap of N+ Active	2.0
d) min. overlap to P+ Active	2.0

6. P+ (inclusive)

P-well substrate contacts (no splits)

a) min. overlap of Active by P+ in P-well (all sides)	0.0
b) min. spacing of N+ Active to P+ Active in P-well	0.0
c) min. spacing of P+ Active to Poly in P-well	1.5

General

a) min. width	3.0
b) min. spacing	3.0
c) min. overlap of P+ Active	2.0
d) min. overlap to N+ Active	2.0

7. Contact

a) min. dimension	2.0
b) min. spacing	3.0
c) min. overlap by Poly	1.0
d) min. overlap by Poly in the direction of Metal 1	2.0
e) min. overlap by Active	1.5
f) min. overlap by Metal 1	1.0
g) min. spacing to unrelated Poly	3.0
h) min. spacing to unrelated Active	2.0

8. Metal 1

a) min. width	3.0
b) min. spacing	3.0

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all dimensions in lambda

9.	**Via**	
	a) min. dimension	2.5
	b) min. spacing	3.0
	c) min. overlap by Active	2.0
	d) min. overlap by Poly	2.0
	e) min. overlap by Metal 1	1.75
	f) min. overlap by Metal 2	1.5
	g) min. spacing to Active	2.0
	h) min. spacing to Poly	2.0
	i) min. spacing to Contact	3.0
10.	**Metal 2**	
	Step coverage rules	
	a) min. overlap of Poly by Metal 1 under Metal 2	2.0
	b) min. overlap of Metal 1 by Poly under Metal 2	2.0
	c) min. intersection of Metal 1 and Poly under Metal 2	2.0
	d) min. spacing of Metal 1 to Poly under Metal 2	2.5
	General	
	a) min. width	3.0
	b) min. spacing	3.0
11.	**Pads/Overglass**	
	a) min. pad metal (Metal 1 and Metal 2) dimension	115.0
	b) min. pad metal width at the pad junction	50.0
	c) min. pad metal spacing	140.0
	d) min. pad metal overlap of Via	5.0
	e) min. Via overlap of Overglass	5.0
	f) min. pad metal spacing to well, Active, Poly, or metal	30.0
12.	**Metal guard-ring**	
	a) min. width	40.0
	b) min. spacing to pad metal	50.0

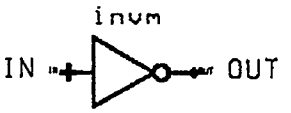
APPENDIX B: Cell documentation

NAME: invm
SYNOPSIS: small to medium power inverter

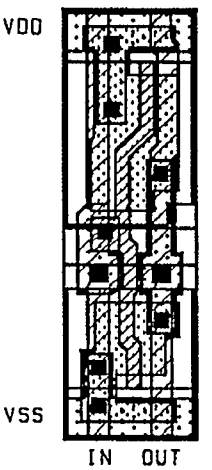
PROPERTIES

DIMENSIONS:	18 * 63 lambda (2 * 7 pitches)			
FEEDTHROUGHS:	0			
INTERFACE:	IN	input	0.706	unit loads
	OUT	output	0.058	unit loads

Logic Diagram



Layout

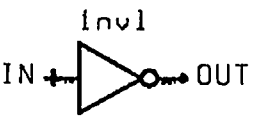


NAME: invl
SYNOPSIS: high power inverter

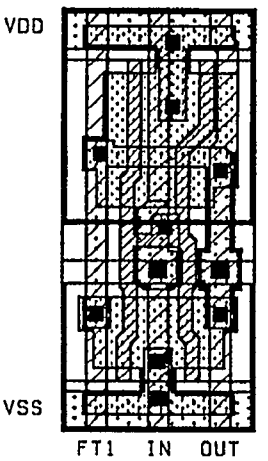
PROPERTIES

DIMENSIONS:	27 * 63 lambda (3 * 7 pitches)			
FEEDTHROUGHS:	1			
INTERFACE:	IN	input	1.332	unit loads
	OUT	output	0.093	unit loads
	FT1	feedthrough	0.053	unit loads

Logic Diagram



Layout

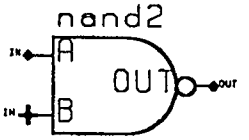


NAME: nand2
SYNOPSIS: 2 input NAND gate

PROPERTIES

DIMENSIONS:	27 * 63 lambda (3 * 7 pitches)		
FEEDTHROUGHS:	0		
INTERFACE:	A	input	0.690 unit loads
	B	input	0.669 unit loads
	OUT	output	0.080 unit loads

Logic Diagram



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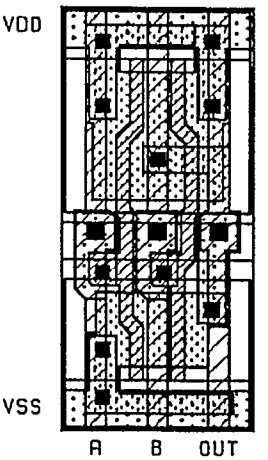
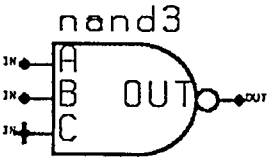


NAME: nand3
SYNOPSIS: 3 input NAND gate

PROPERTIES
DIMENSIONS: 36 * 63 lambda (4 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.690	unit loads
B	input	0.671	unit loads
C	input	0.666	unit loads
OUT	output	0.087	unit loads

Logic Diagram



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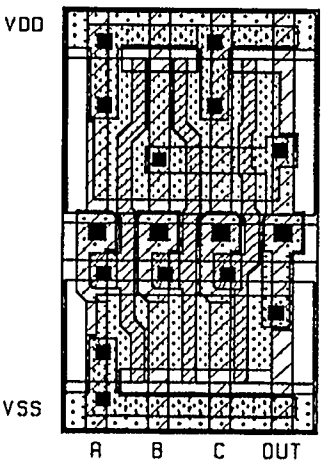
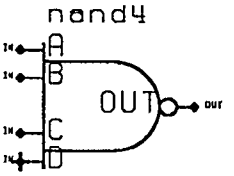


NAME: nand4
SYNOPSIS: 4 input NAND gate

PROPERTIES
DIMENSIONS: 45 * 63 lambda (5 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.690	unit loads
B	input	0.700	unit loads
C	input	0.706	unit loads
D	input	0.698	unit loads
OUT	output	0.105	unit loads

Logic Diagram



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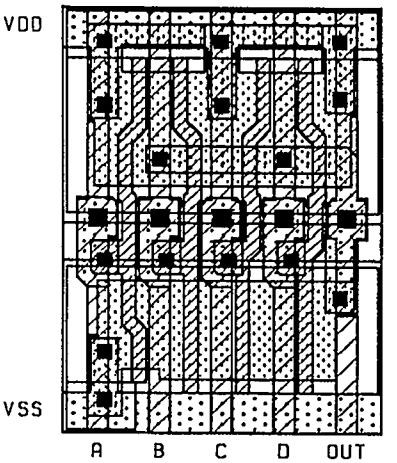
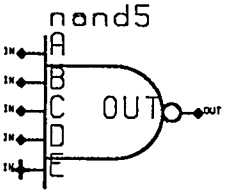


NAME: nand5
SYNOPSIS: 5 input NAND gate

PROPERTIES
DIMENSIONS: 54 * 63 lambda (6 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.690	unit loads
B	input	0.700	unit loads
C	input	0.706	unit loads
D	input	0.698	unit loads
E	input	0.705	unit loads
OUT	output	0.113	unit loads

Logic Diagram



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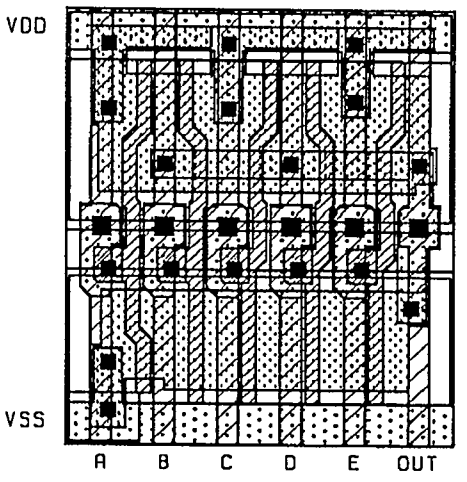
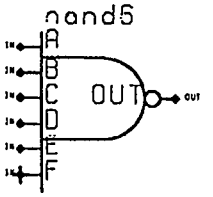


NAME: nand6
SYNOPSIS: 6 input NAND gate

PROPERTIES
DIMENSIONS: 63 * 63 lambda (7 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.690	unit loads
B	input	0.700	unit loads
C	input	0.706	unit loads
D	input	0.698	unit loads
E	input	0.705	unit loads
F	input	0.698	unit loads
OUT	output	0.134	unit loads

Logic Diagram



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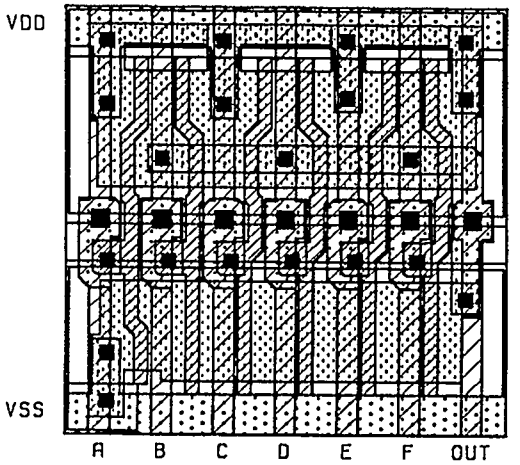
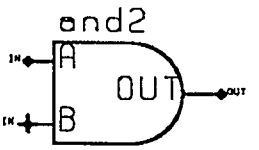


NAME: and2
SYNOPSIS: 2 input AND gate

PROPERTIES

DIMENSIONS:	36 * 63 lambda (4 * 7 pitches)			
FEEDTHROUGHS:	0			
INTERFACE:	A	input	0.675	unit loads
	B	input	0.690	unit loads
	OUT	output	0.056	unit loads

Logic Diagram



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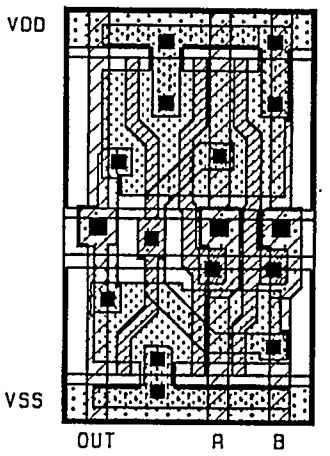
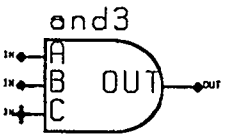


NAME: and3
SYNOPSIS: 3 input AND gate

PROPERTIES
DIMENSIONS: 45 * 63 lambda (5 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.675	unit loads
B	input	0.679	unit loads
C	input	0.670	unit loads
OUT	output	0.056	unit loads

Logic Diagram



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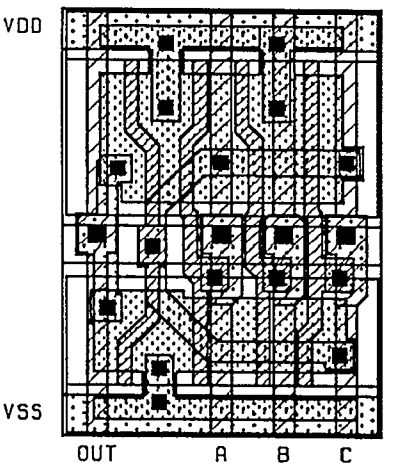
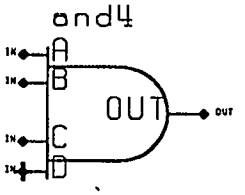


NAME: and4
SYNOPSIS: 4 input AND gate

PROPERTIES
DIMENSIONS: 54 * 63 lambda (6 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.675	unit loads
B	input	0.681	unit loads
C	input	0.673	unit loads
D	input	0.690	unit loads
OUT	output	0.056	unit loads

Logic Diagram



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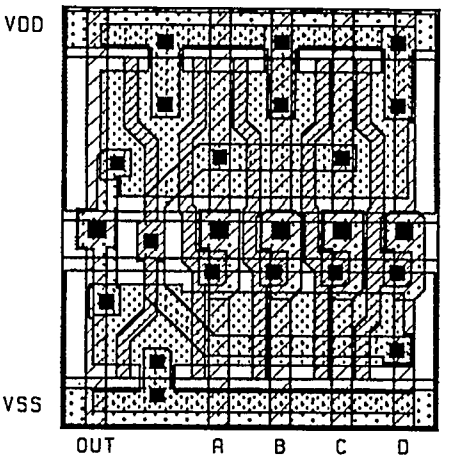
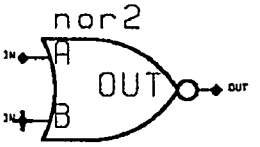


NAME: nor2
SYNOPSIS: 2 input NOR gate

PROPERTIES

DIMENSIONS:	27 * 63 lambda (3 * 7 pitches)			
FEEDTHROUGHS:	0			
INTERFACE:	A	input	0.678	unit loads
	B	input	0.699	unit loads
	OUT	output	0.075	unit loads

Logic Diagram



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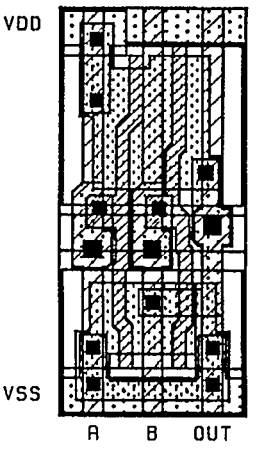
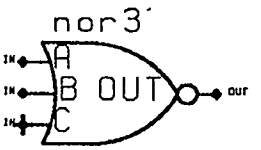


NAME: nor3
SYNOPSIS: 3 input NOR gate

PROPERTIES
DIMENSIONS: 36 * 63 lambda (4 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.756	unit loads
B	input	0.724	unit loads
C	input	0.695	unit loads
OUT	output	0.083	unit loads

Logic Diagram



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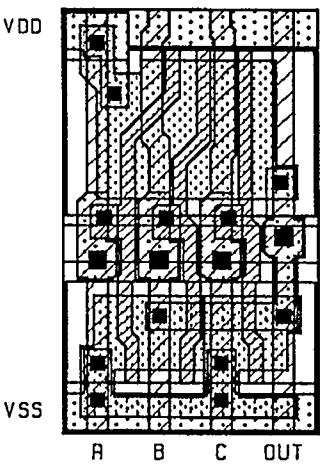
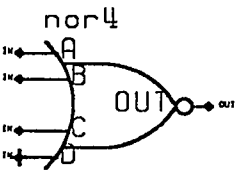


NAME: nor4
SYNOPSIS: 4 input NOR gate

PROPERTIES
DIMENSIONS: 45 * 63 lambda (5 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.818	unit loads
B	input	0.790	unit loads
C	input	0.751	unit loads
D	input	0.729	unit loads
OUT	output	0.103	unit loads

Logic Diagram



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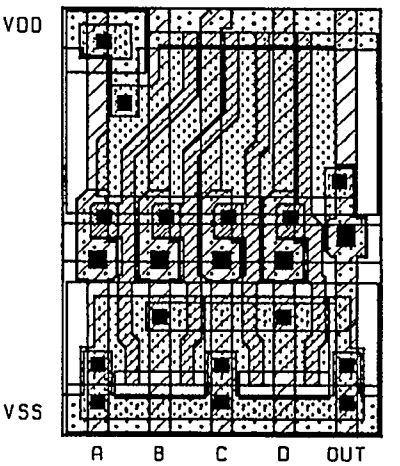
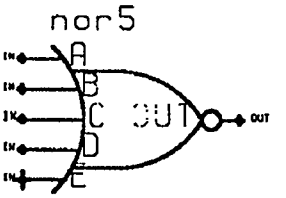


NAME: nor5
SYNOPSIS: 5 input NOR gate

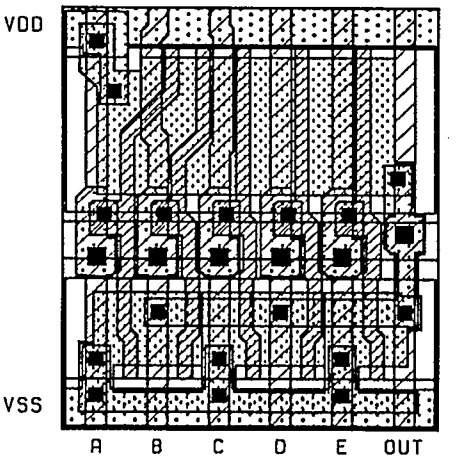
PROPERTIES
DIMENSIONS: 54 * 63 lambda (6 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.756	unit loads
B	input	0.724	unit loads
C	input	0.695	unit loads
D	input	0.690	unit loads
E	input	0.694	unit loads
OUT	output	0.112	unit loads

Logic Diagram



Layout

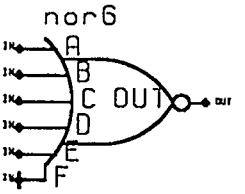


NAME: nor6
SYNOPSIS: 6 input NOR gate

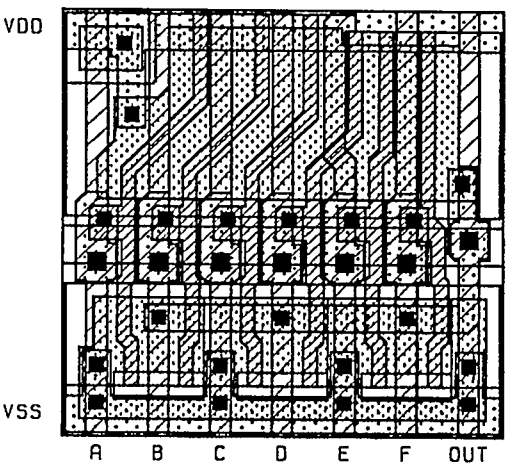
PROPERTIES
DIMENSIONS: 63 * 63 lambda (7 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.891	unit loads
B	input	0.893	unit loads
C	input	0.878	unit loads
D	input	0.800	unit loads
E	input	0.761	unit loads
F	input	0.739	unit loads
OUT	output	0.134	unit loads

Logic Diagram



Layout

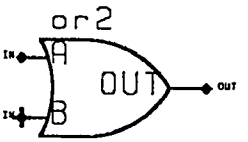


NAME: or2
SYNOPSIS: 2 input OR gate

PROPERTIES
DIMENSIONS: 36 * 63 lambda (4 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.732	unit loads
B	input	0.715	unit loads
OUT	output	0.054	unit loads

Logic Diagram



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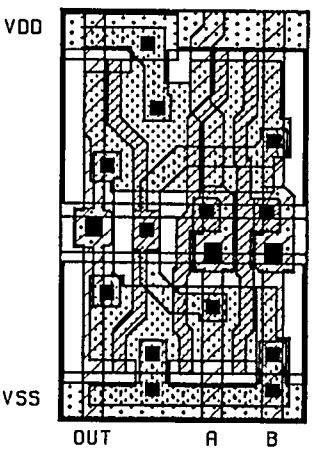


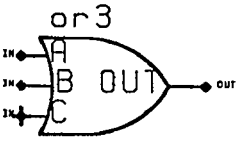
NAME: or3
SYNOPSIS: 3 input OR gate

PROPERTIES

DIMENSIONS: 45 * 63 lambda (5 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.732	unit loads
B	input	0.696	unit loads
C	input	0.710	unit loads
OUT	output	0.054	unit loads

Logic Diagram



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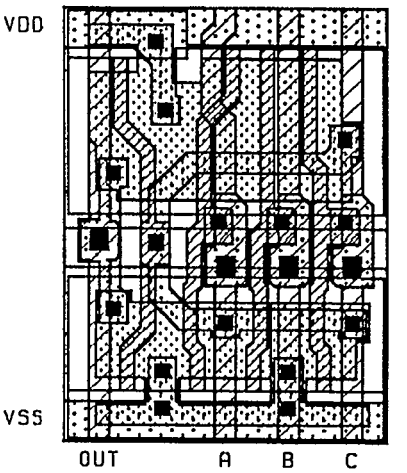
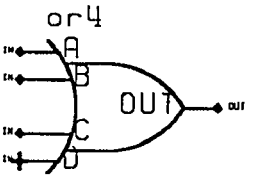


NAME: or4
SYNOPSIS: 4 input OR gate

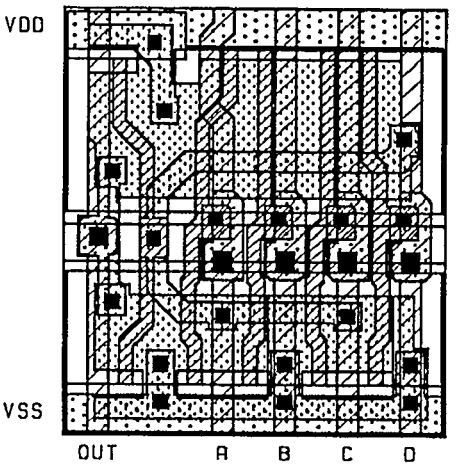
PROPERTIES
DIMENSIONS: 54 * 63 lambda (6 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

A	input	0.732	unit loads
B	input	0.696	unit loads
C	input	0.693	unit loads
D	input	0.710	unit loads
OUT	output	0.054	unit loads

Logic Diagram



Layout

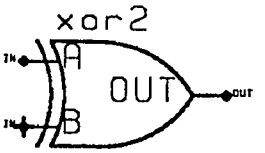


NAME: xor2
SYNOPSIS: 2 input EXCLUSIVE OR gate

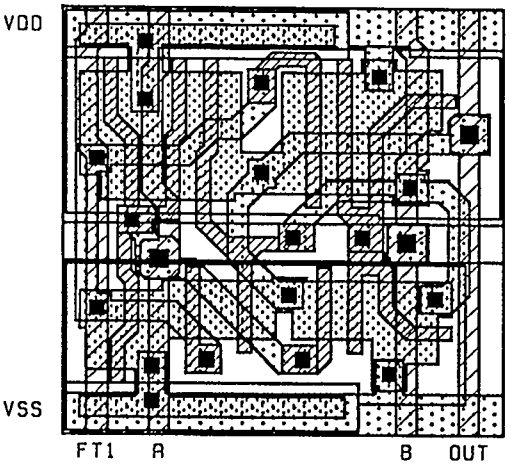
PROPERTIES

DIMENSIONS:	63 * 63 lambda (7 * 7 pitches)			
FEEDTHROUGHS:	1			
INTERFACE:	A	input	1.293	unit loads
	B	input	1.254	unit loads
	OUT	output	0.103	unit loads
	FT1	feedthrough	0.047	unit loads

Logic Diagram



Layout



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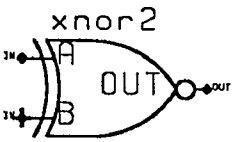
NAME: xnor2
SYNOPSIS: 2 input EXCLUSIVE NOR gate

PROPERTIES

DIMENSIONS: 63 * 63 lambda (7 * 7 pitches)
FEEDTHROUGHS: 1
INTERFACE:

A	input	1.315	unit loads
B	input	1.324	unit loads
OUT	output	0.116	unit loads
FT1	feedthrough	0.048	unit loads

Logic Diagram



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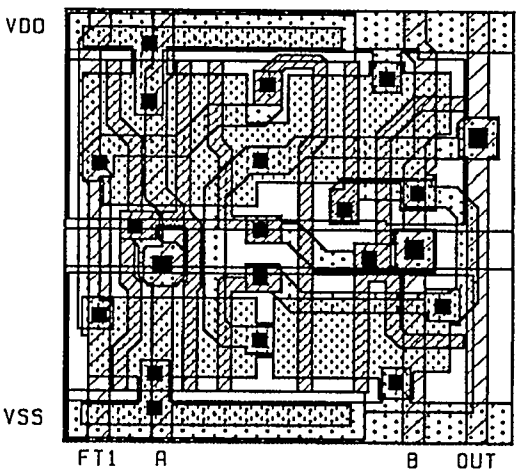
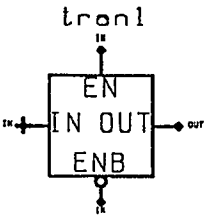


NAME: tran1
SYNOPSIS: transmission gate: n-channel active-high enable (EN) and p-channel active-low enable (ENB)

PROPERTIES
DIMENSIONS: 36 * 63 lambda (4 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

IN	input	0.075	unit loads
EN	enable	0.240	unit loads
ENB	enable	0.413	unit loads
OUT	output	0.074	unit loads

Logic Diagram



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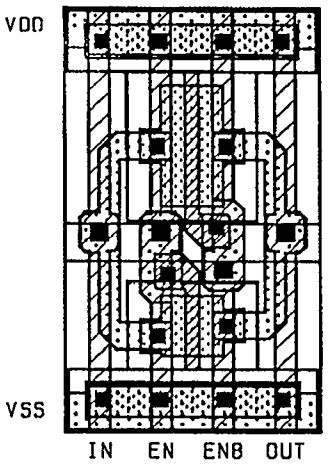
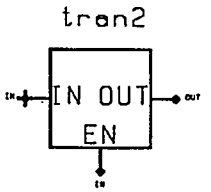


NAME: tran2
SYNOPSIS: transmission gate: active-high enable (EN)

PROPERTIES
DIMENSIONS: 36 * 63 lambda (4 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

IN	input	0.059	unit loads
EN	enable	0.901	unit loads
OUT	output	0.069	unit loads

Logic Diagram



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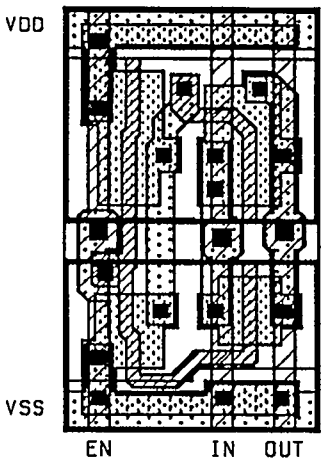
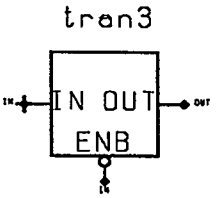


NAME: tran3
SYNOPSIS: transmission gate: active-low enable (ENB)

PROPERTIES
DIMENSIONS: 36 * 63 lambda (4 * 7 pitches)
FEEDTHROUGHS: 0
INTERFACE:

IN	input	0.059	unit loads
ENB	enable	1.119	unit loads
OUT	output	0.068	unit loads

Logic Diagram



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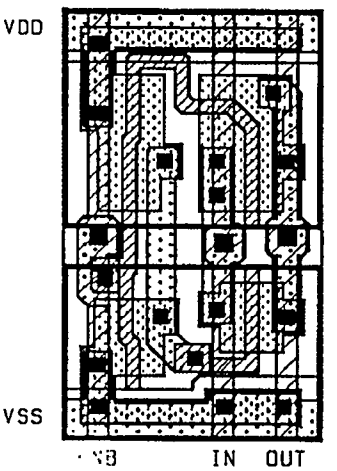
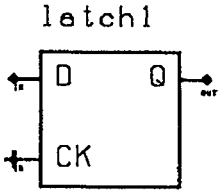


NAME: latch1
SYNOPSIS: transmission gate type latch: output (Q) follows input (D): value latched on negative edge of clock (CK)

PROPERTIES
DIMENSIONS: 72 * 63 lambda (8 * 7 pitches)
FEEDTHROUGHS: 2
INTERFACE:

D	input	0.061	unit loads
CK	input	1.158	unit loads
Q	output	0.060	unit loads
FT1	feedthrough	0.054	unit loads
FT2	feedthrough	0.034	unit loads

Logic Diagram



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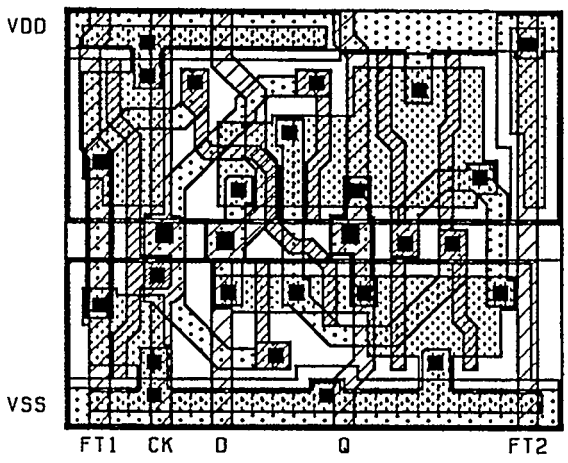


NAME: latch2

SYNOPSIS: transmission gate type latch: output (Q) follows input (D): value latched on negative edge of clock (CK): asynchronous active-low reset (RB)

PROPERTIES

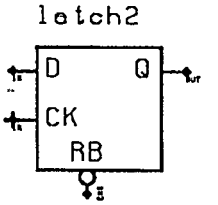
DIMENSIONS: 81 * 63 lambda (9 * 7 pitches)

FEEDTHROUGHS: 2

INTERFACE:

D	input	0.061	unit loads
CK	input	1.158	unit loads
RB	enable	0.727	unit loads
Q	output	0.060	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.039	unit loads

Logic Diagram



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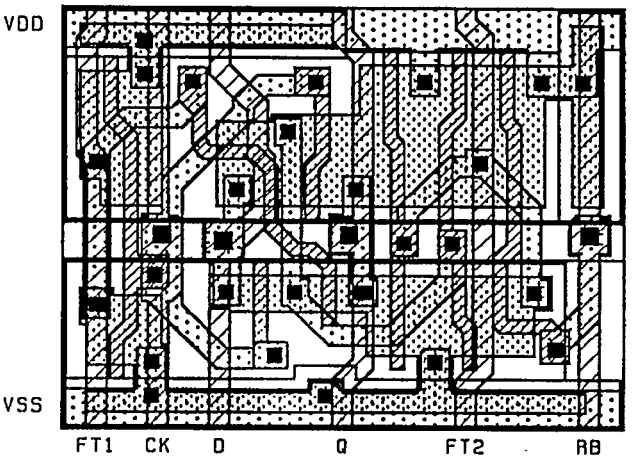
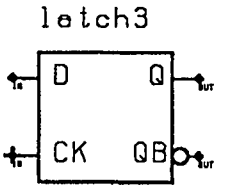


NAME: latch3
SYNOPSIS: transmission gate type latch: output (Q) follows input (D): output (QB) inverse of input (D): values latched on negative edge of clock (CK)

PROPERTIES
DIMENSIONS: 72 * 63 lambda (8 * 7 pitches)
FEEDTHROUGHS: 1
INTERFACE:

D	input	0.061	unit loads
CK	input	1.158	unit loads
Q	output	0.060	unit loads
QB	output	0.741	unit loads
FT1	feedthrough	0.054	unit loads

Logic Diagram



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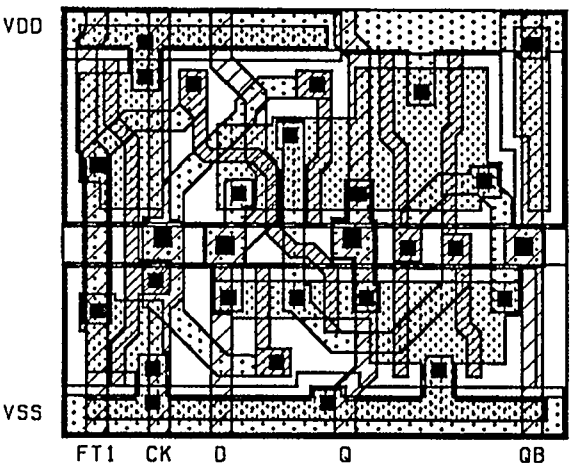
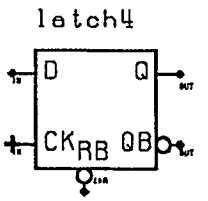


NAME: latch4
SYNOPSIS: transmission gate type latch: output (Q) follows input (D): output (QB) inverse of input (D): values latched on negative edge of clock (CK): asychronous active-low reset (RB)

PROPERTIES
DIMENSIONS: 81 * 63 lambda (9 * 7 pitches)
FEEDTHROUGHS: 1
INTERFACE:

D	input	0.061	unit loads
CK	input	1.157	unit loads
RB	enable	0.727	unit loads
Q	output	0.060	unit loads
QB	output	0.740	unit loads
FT1	feedthrough	0.053	unit loads

Logic Diagram



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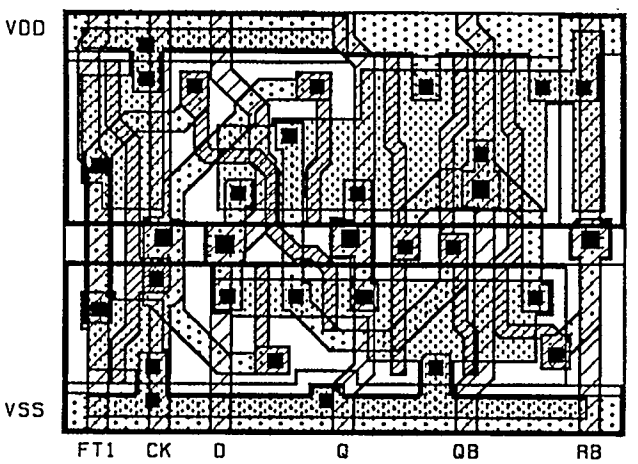
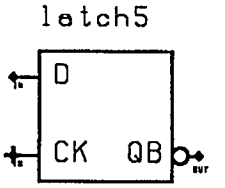


NAME: latch5
SYNOPSIS: transmission gate type latch: output (QB) inverse of input (D): value latched on negative edge of clock (CK)

PROPERTIES
DIMENSIONS: 72 * 63 lambda (8 * 7 pitches)
FEEDTHROUGHS: 2
INTERFACE:

D	input	0.061	unit loads
CK	input	1.158	unit loads
QB	output	0.741	unit loads
FT1	feedthrough	0.054	unit loads
FT2	feedthrough	0.049	unit loads

Logic Diagram



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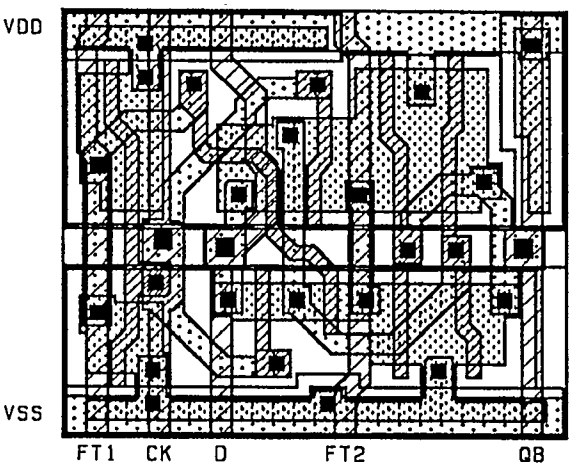


NAME: latch6

SYNOPSIS: transmission gate type latch: output (QB) inverse of input (D): value latched on negative edge of clock (CK): asynchronous active-low reset (RB)

PROPERTIES

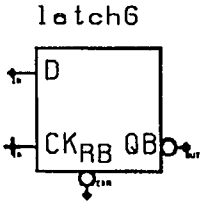
DIMENSIONS: 81 * 63 lambda (9 * 7 pitches)

FEEDTHROUGHS: 2

INTERFACE:

D	input	0.061	unit loads
CK	input	1.157	unit loads
RB	enable	0.727	unit loads
QB	output	0.740	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.050	unit loads

Logic Diagram



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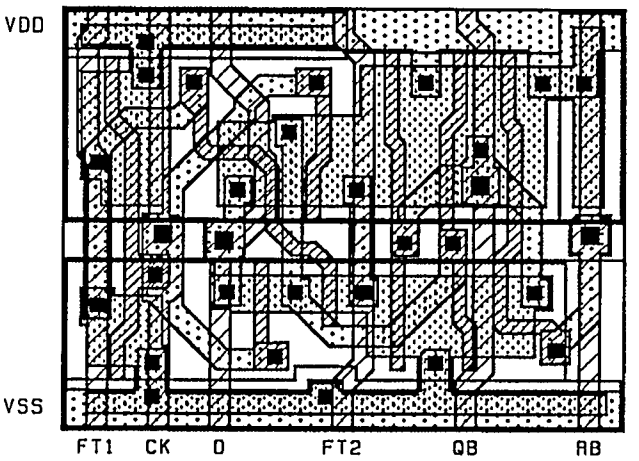
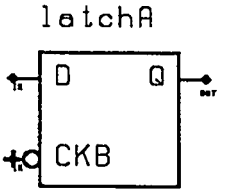


NAME: latchA
SYNOPSIS: transmission gate type latch: output (Q) follows input (D): value latched on positive edge of clock (CKB)

PROPERTIES
DIMENSIONS: 72 * 63 lambda (8 * 7 pitches)
FEEDTHROUGHS: 2
INTERFACE:

D	input	0.058	unit loads
CKB	input	1.145	unit loads
Q	output	0.060	unit loads
FT1	feedthrough	0.054	unit loads
FT2	feedthrough	0.034	unit loads

Logic Diagram



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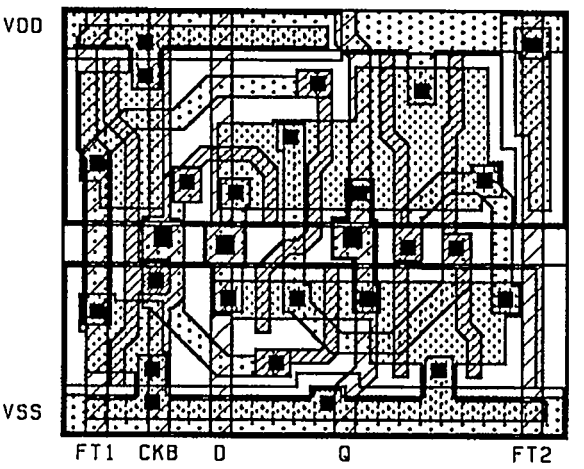
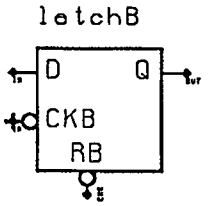


NAME: latchB
SYNOPSIS: transmission gate type latch: output (Q) follows input (D): value latched on positive edge of clock (CKB): asynchronous active-low reset (RB)

PROPERTIES
DIMENSIONS: 81 * 63 lambda (9 * 7 pitches)
FEEDTHROUGHS: 2
INTERFACE:

D	input	0.058	unit loads
CKB	input	1.145	unit loads
RB	enable	0.727	unit loads
Q	output	0.060	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.039	unit loads

Logic Diagram



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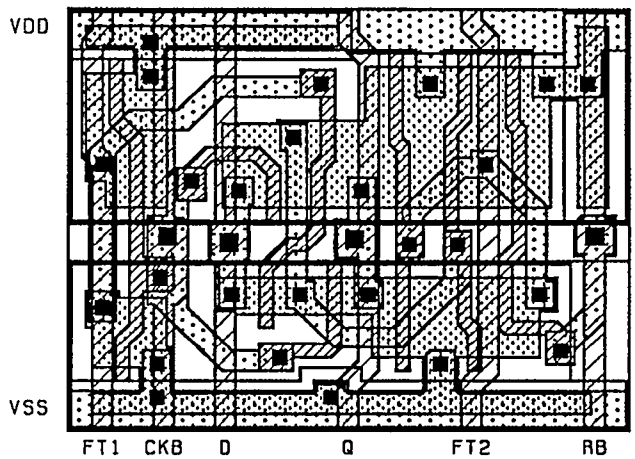
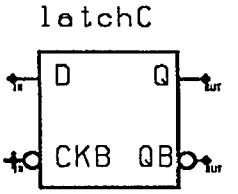


NAME: latchC
SYNOPSIS: transmission gate type latch: output (Q) follows input (D): output (QB) inverse of input (D): values latched on positive edge of clock (CKB)

PROPERTIES
DIMENSIONS: 72 * 63 lambda (8 * 7 pitches)
FEEDTHROUGHS: 1
INTERFACE:

D	input	0.058	unit loads
CKB	input	1.145	unit loads
Q	output	0.060	unit loads
QB	output	0.742	unit loads
FT1	feedthrough	0.053	unit loads

Logic Diagram



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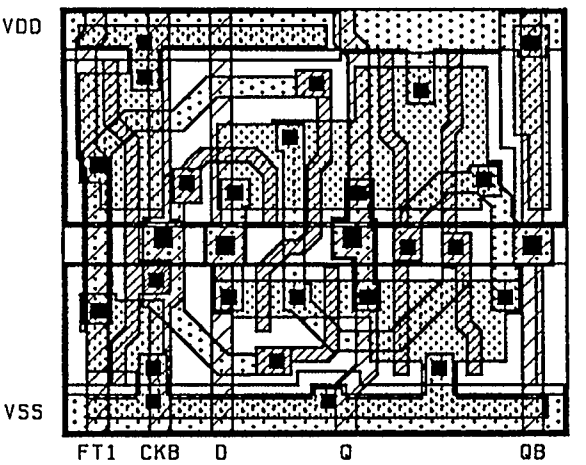
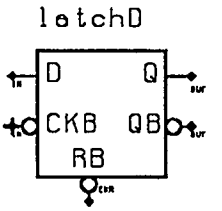


NAME: latchD
SYNOPSIS: transmission gate type latch: output (Q) follows input (D): output (QB) inverse of input (D): values latched on positive edge of clock (CKB): asychronous active-low reset (RB)

PROPERTIES
DIMENSIONS: 81 * 63 lambda (9 * 7 pitches)
FEEDTHROUGHS: 1
INTERFACE:

D	input	0.058	unit loads
CKB	input	1.145	unit loads
RB	enable	0.727	unit loads
Q	output	0.060	unit loads
QB	output	0.740	unit loads
FT1	feedthrough	0.053	unit loads

Logic Diagram



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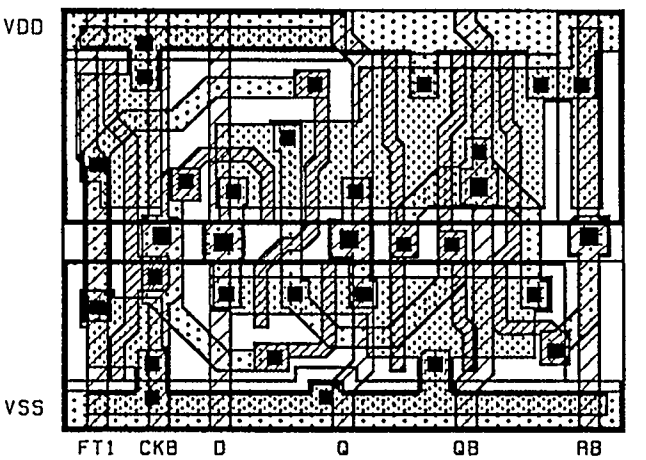
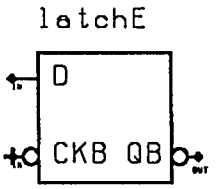


NAME: latchE
SYNOPSIS: transmission gate type latch: output (QB) inverse of input (D): value latched on positive edge of clock (CKB)

PROPERTIES
DIMENSIONS: 72 * 63 lambda (8 * 7 pitches)
FEEDTHROUGHS: 2
INTERFACE:

D	input	0.058	unit loads
CKB	input	1.145	unit loads
QB	output	0.742	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.049	unit loads

Logic Diagram



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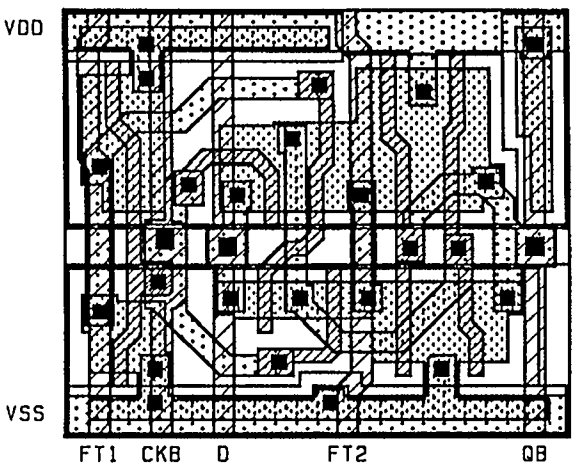


NAME: latchF

SYNOPSIS: transmission gate type latch: output (QB) inverse of input (D): value latched on positive edge of clock (CKB): asynchronous active-low reset (RB)

PROPERTIES

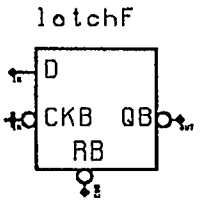
DIMENSIONS: 81 * 63 lambda (9 * 7 pitches)

FEEDTHROUGHS: 2

INTERFACE:

D	input	0.058	unit loads
CKB	input	1.145	unit loads
RB	enable	0.727	unit loads
QB	output	0.740	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.050	unit loads

Logic Diagram



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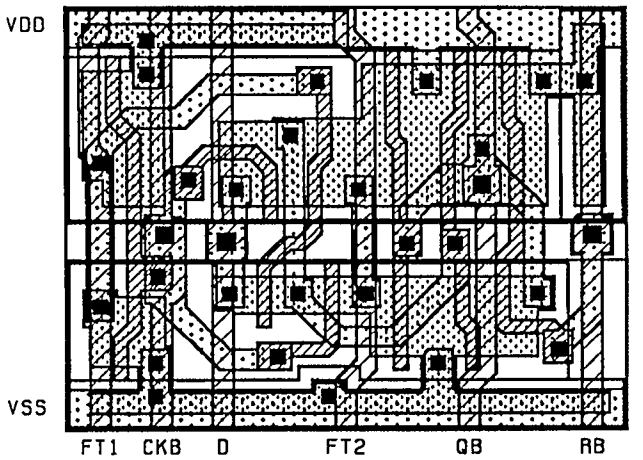
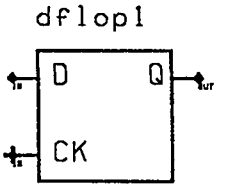


NAME: dflop1
SYNOPSIS: transmission gate type D flip-flop: input (D) stored on positive clock (CK) edge: positive output (Q)

PROPERTIES
DIMENSIONS: 135 * 63 lambda (15 * 7 pitches)
FEEDTHROUGHS: 6
INTERFACE:

D	input	0.058	unit loads
CK	input	1.145	unit loads
Q	output	0.750	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.054	unit loads
FT3	feedthrough	0.045	unit loads
FT4	feedthrough	0.061	unit loads
FT5	feedthrough	0.047	unit loads
FT6	feedthrough	0.052	unit loads

Logic Diagram



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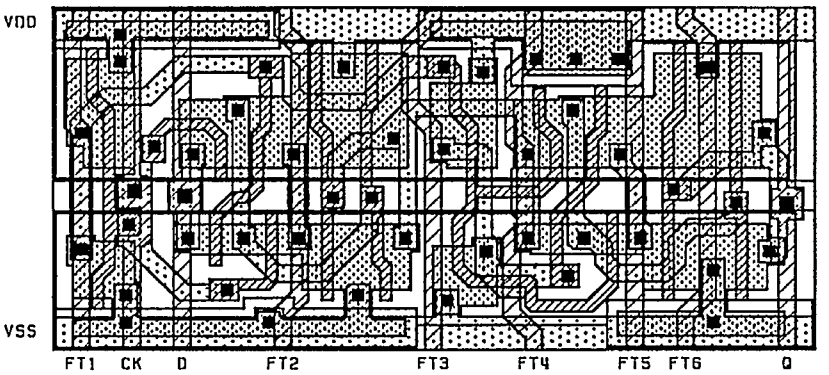


NAME: dflop2

SYNOPSIS: transmission gate type D flip-flop: input (D) stored on positive clock (CK) edge: positive output (Q): asynchronous active-low reset (RB)

PROPERTIES

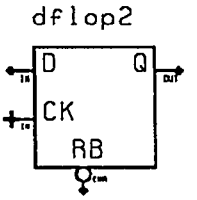
DIMENSIONS: 153 * 63 lambda (17 * 7 pitches)

FEEDTHROUGHS: 4

INTERFACE:

D	input	0.058	unit loads
CK	input	1.145	unit loads
RB	enable	1.521	unit loads
Q	output	0.734	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.054	unit loads
FT3	feedthrough	0.062	unit loads
FT4	feedthrough	0.043	unit loads

Logic Diagram



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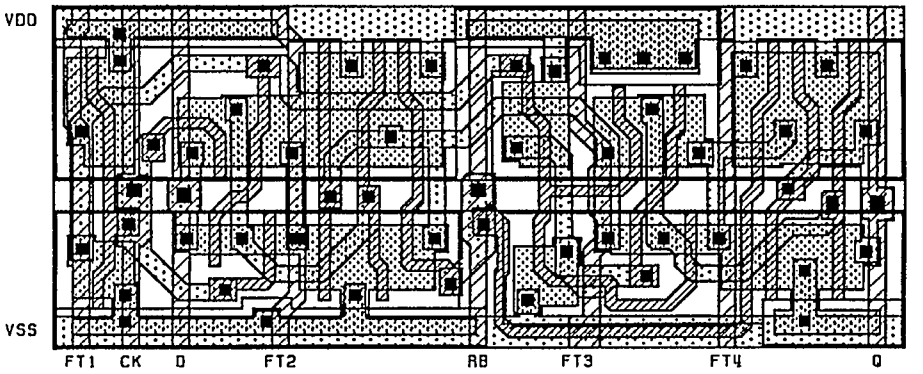


NAME: dflop3

SYNOPSIS: transmission gate type D flip-flop: input (D) stored on positive clock (CK) edge: positive output (Q): asynchronous active-low set (SB)

PROPERTIES

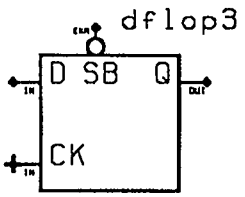
DIMENSIONS: 153 * 63 lambda (17 * 7 pitches)

FEEDTHROUGHS: 5

INTERFACE:

D	input	0.058	unit loads
CK	input	1.145	unit loads
SB	enable	1.637	unit loads
Q	output	0.770	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.054	unit loads
FT3	feedthrough	0.055	unit loads
FT4	feedthrough	0.054	unit loads
FT5	feedthrough	0.051	unit loads

Logic Diagram



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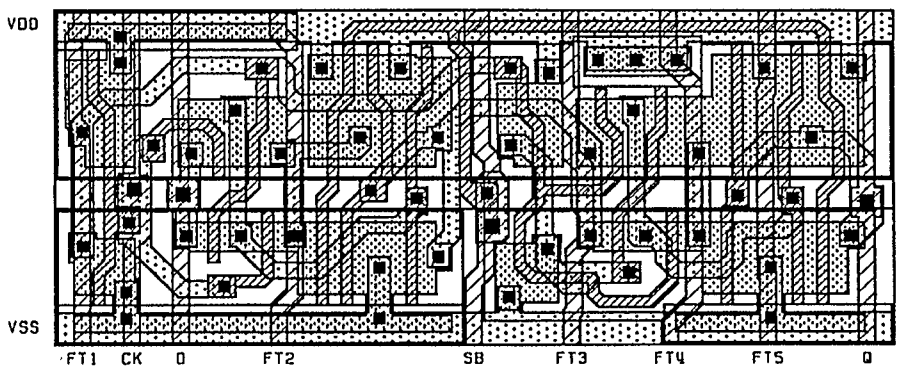


NAME: dflop4

SYNOPSIS: transmission gate type D flip-flop: input (D) stored on positive clock (CK) edge: positive output (Q): asynchronous active-low set (SB) and reset (RB)

PROPERTIES

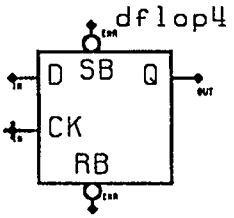
DIMENSIONS: 171 * 63 lambda (19 * 7 pitches)

FEEDTHROUGHS: 4

INTERFACE:

D	input	0.058	unit loads
CK	input	1.145	unit loads
RB	enable	1.530	unit loads
SB	enable	1.597	unit loads
Q	output	0.757	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.054	unit loads
FT3	feedthrough	0.065	unit loads
FT4	feedthrough	0.049	unit loads

Logic Diagram



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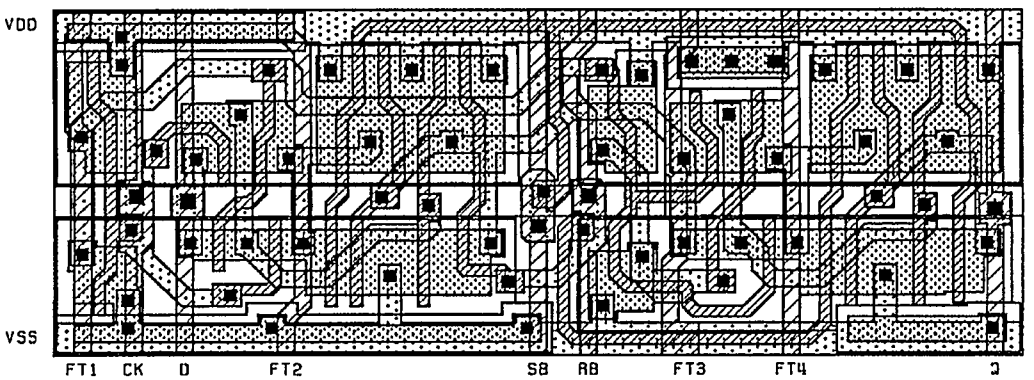
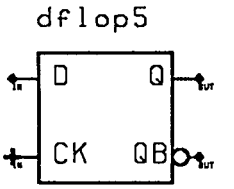


NAME: dflop5
SYNOPSIS: transmission gate type D flip-flop: input (D) stored on positive clock (CK) edge: positive (Q) and inverted (QB) outputs

PROPERTIES
DIMENSIONS: 135 * 63 lambda (15 * 7 pitches)
FEEDTHROUGHS: 5
INTERFACE:

D	input	0.058	unit loads
CK	input	1.145	unit loads
Q	output	0.750	unit loads
QB	output	0.060	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.054	unit loads
FT3	feedthrough	0.045	unit loads
FT4	feedthrough	0.061	unit loads
FT5	feedthrough	0.052	unit loads

Logic Diagram



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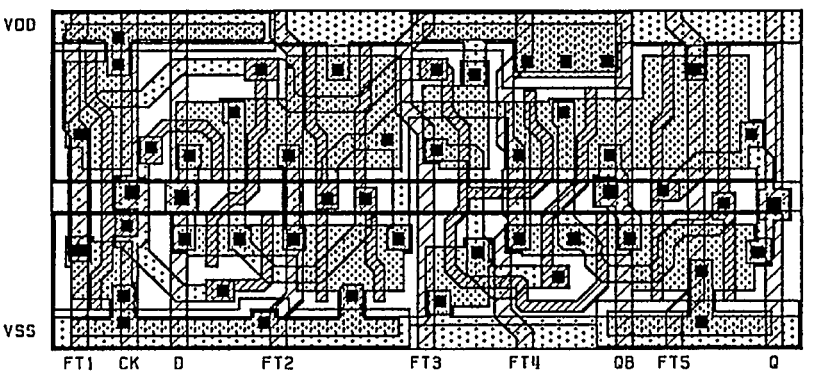


NAME: dflop6

SYNOPSIS: transmission gate type D flip-flop: input (D) stored on positive clock (CK) edge: positive (Q) and inverted (QB) outputs: asynchronous active-low reset (RB)

PROPERTIES

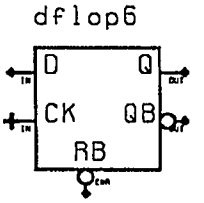
DIMENSIONS: 153 * 63 lambda (17 * 7 pitches)

FEEDTHROUGHS: 3

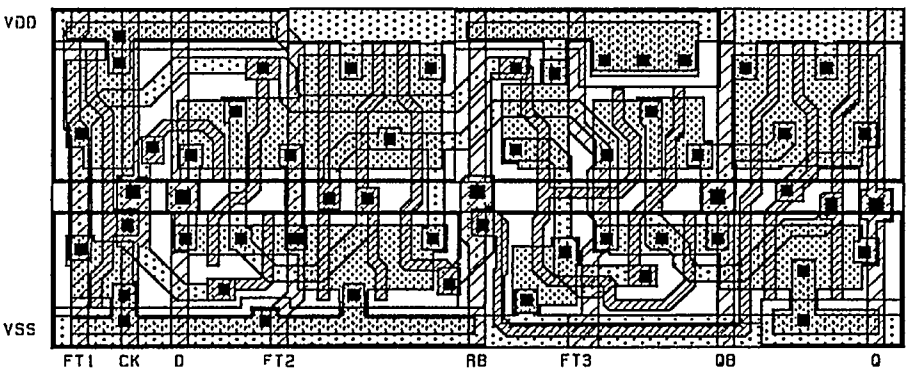
INTERFACE:

D	input	0.058	unit loads
CK	input	1.145	unit loads
RB	enable	1.521	unit loads
Q	output	0.734	unit loads
QB	output	0.077	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.054	unit loads
FT3	feedthrough	0.062	unit loads

Logic Diagram



Layout



NAME: dflop7

SYNOPSIS: transmission gate type D flip-flop: input (D) stored on positive clock (CK) edge: positive (Q) and inverted (QB) outputs: asynchronous active-low set (SB)

PROPERTIES

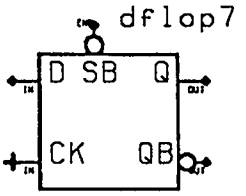
DIMENSIONS: 153 * 63 lambda (17 * 7 pitches)

FEEDTHROUGHS: 4

INTERFACE:

D	input	0.058	unit loads
CK	input	1.145	unit loads
SB	enable	1.637	unit loads
Q	output	0.770	unit loads
QB	output	0.066	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.054	unit loads
FT3	feedthrough	0.055	unit loads
FT4	feedthrough	0.051	unit loads

Logic Diagram



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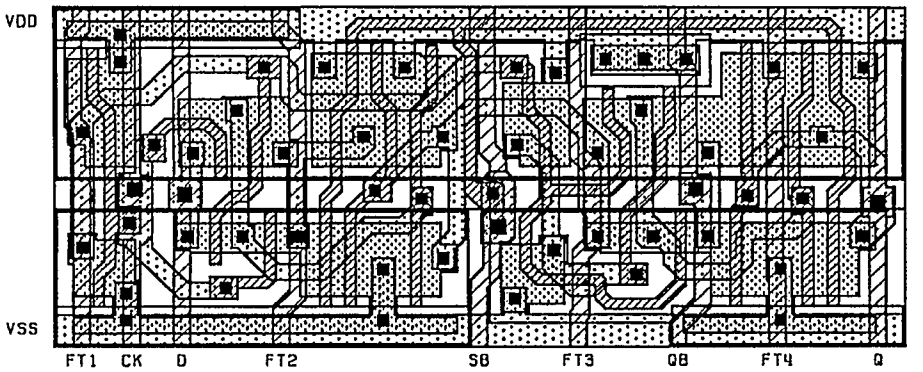


NAME: dflop8

SYNOPSIS: transmission gate type D flip-flop: input (D) stored on positive clock (CK) edge: positive (Q) and inverted (QB) outputs: asynchronous active-low set (SB) and reset (RB)

PROPERTIES

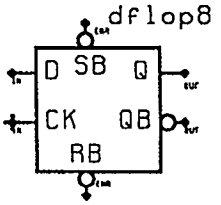
DIMENSIONS: 171 * 63 lambda (19 * 7 pitches)

FEEDTHROUGHS: 3

INTERFACE:

D	input	0.058	unit loads
CK	input	1.145	unit loads
RB	enable	1.530	unit loads
SB	enable	1.597	unit loads
Q	output	0.757	unit loads
QB	output	0.075	unit loads
FT1	feedthrough	0.053	unit loads
FT2	feedthrough	0.054	unit loads
FT3	feedthrough	0.065	unit loads

Logic Diagram



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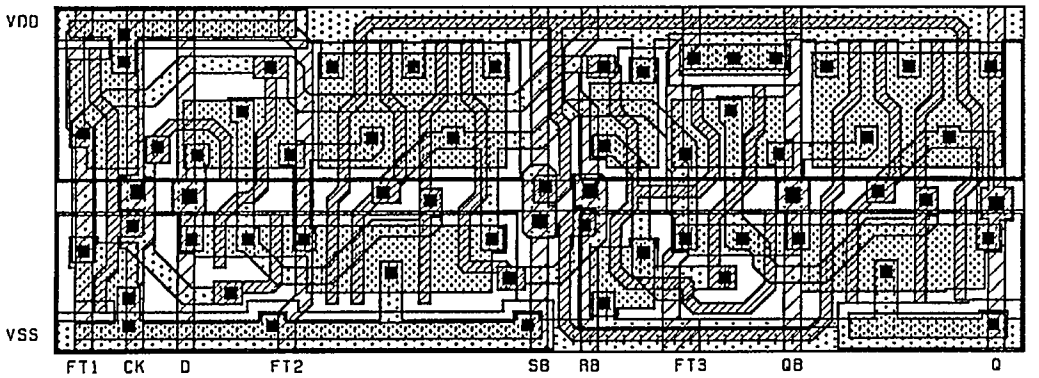
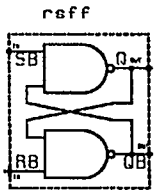


NAME: rsff
SYNOPSIS: an RS flip-flop: positive (Q) and inverted (QB) outputs: active-low set (SB) and reset (RB)

PROPERTIES
DIMENSIONS: 54 * 63 lambda (6 * 7 pitches)
FEEDTHROUGHS: 1
INTERFACE:

RB	input	0.693	unit loads
SB	input	0.673	unit loads
Q	output	0.735	unit loads
QB	output	0.747	unit loads
FT1	feedthrough	0.054	unit loads

Logic Diagram



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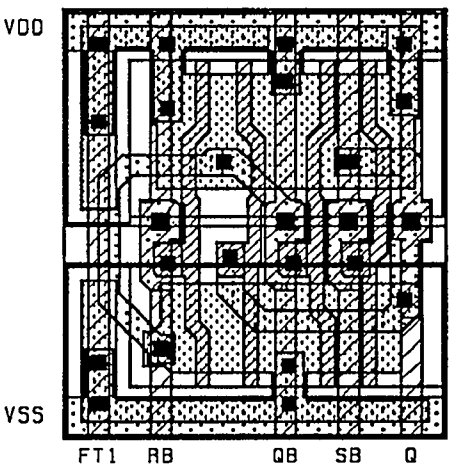
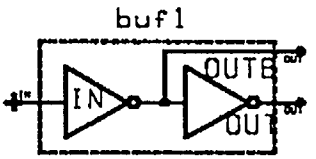


NAME: buf1
SYNOPSIS: standard buffer: positive (OUT) and inverted (OUTB) outputs

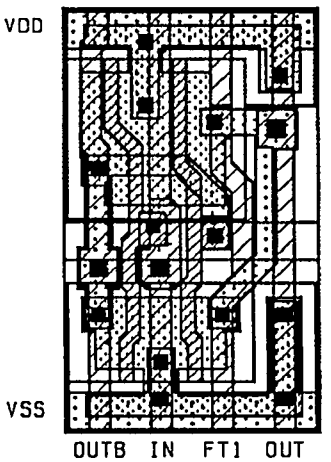
PROPERTIES
DIMENSIONS: 36 * 63 lambda (4 * 7 pitches)
FEEDTHROUGHS: 1
INTERFACE:

IN	input	0.710	unit loads
OUT	output	0.095	unit loads
OUTB	output	0.717	unit loads
FT1	feedthrough	0.045	unit loads

Logic Diagram



Layout

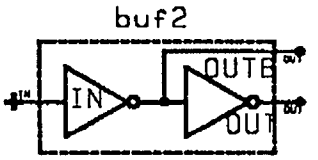


NAME: buf2
SYNOPSIS: high power buffer: positive (OUT) and inverted (OUTB) outputs

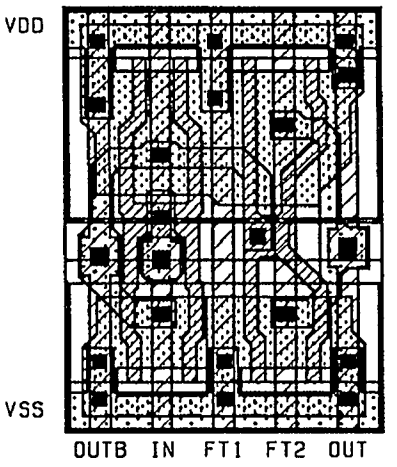
PROPERTIES
DIMENSIONS: 45 * 63 lambda (5 * 7 pitches)
FEEDTHROUGHS: 2
INTERFACE:

IN	input	1.271	unit loads
OUT	output	0.093	unit loads
OUTB	output	1.404	unit loads
FT1	feedthrough	0.046	unit loads
FT2	feedthrough	0.040	unit loads

Logic Diagram



Layout

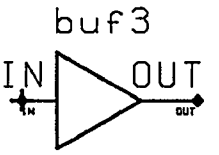


NAME: buf3
SYNOPSIS: standard buffer: positive output (OUT)

PROPERTIES

DIMENSIONS:	27 * 63 lambda (3 * 7 pitches)		
FEEDTHROUGHS:	1		
INTERFACE:	IN	input	0.657 unit loads
	OUT	output	0.058 unit loads
	FT1	feedthrough	0.052 unit loads

Logic Diagram



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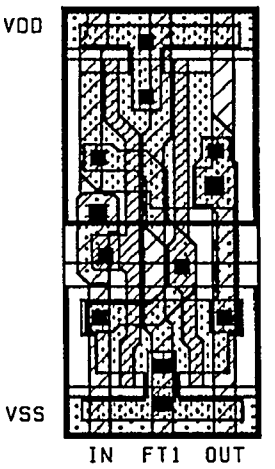
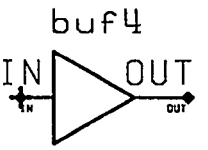


NAME: buf4
SYNOPSIS: high power buffer: positive output (OUT)

PROPERTIES
DIMENSIONS: 45 * 63 lambda (5 * 7 pitches)
FEEDTHROUGHS: 3
INTERFACE:

IN	input	1.269	unit loads
OUT	output	0.090	unit loads
FT1	feedthrough	0.046	unit loads
FT2	feedthrough	0.050	unit loads
FT3	feedthrough	0.040	unit loads

Logic Diagram



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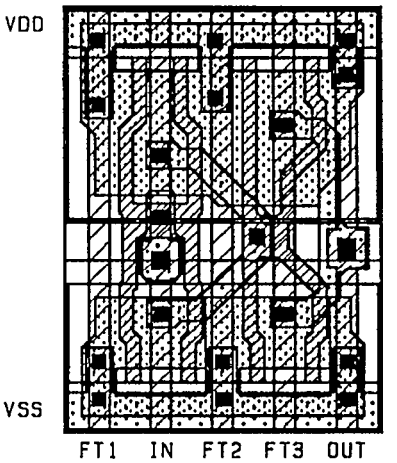
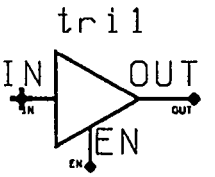


NAME: tri1
SYNOPSIS: standard tristate buffer: positive output (OUT): active-high enable (EN)

PROPERTIES
DIMENSIONS: 72 * 63 lambda (8 * 7 pitches)
FEEDTHROUGHS: 2
INTERFACE:

IN	input	1.412	unit loads
EN	enable	1.265	unit loads
OUT	output	0.083	unit loads
FT1	feedthrough	0.044	unit loads
FT2	feedthrough	0.045	unit loads

Logic Diagram



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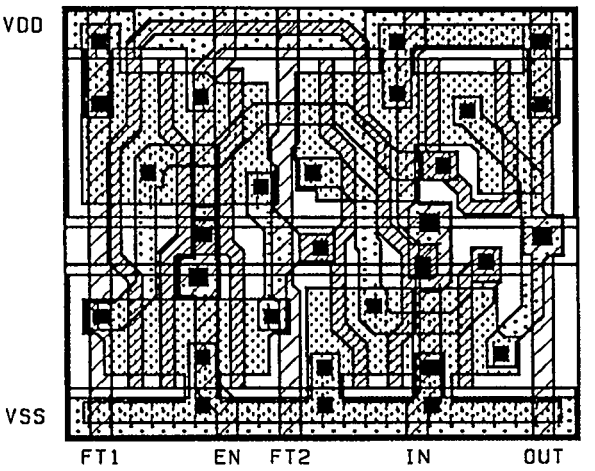
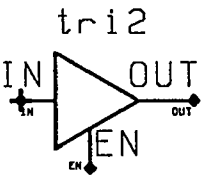


NAME: tri2
SYNOPSIS: high power tristate buffer: positive output (OUT): active-high enable (EN)

PROPERTIES
DIMENSIONS: 81 * 63 lambda (9 * 7 pitches)
FEEDTHROUGHS: 3
INTERFACE:

IN	input	1.412	unit loads
EN	enable	1.265	unit loads
OUT	output	0.101	unit loads
FT1	feedthrough	0.044	unit loads
FT2	feedthrough	0.045	unit loads
FT3	feedthrough	0.051	unit loads

Logic Diagram



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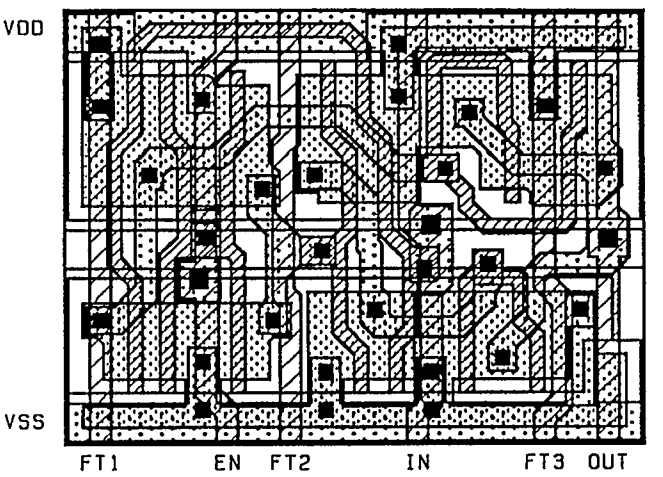
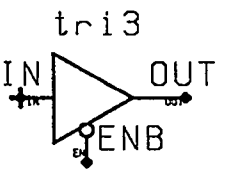


NAME: tri3
SYNOPSIS: standard tristate buffer: positive output (OUT): active-low enable (ENB)

PROPERTIES
DIMENSIONS: 72 * 63 lambda (8 * 7 pitches)
FEEDTHROUGHS: 2
INTERFACE:

IN	input	1.412	unit loads
ENB	enable	1.335	unit loads
OUT	output	0.083	unit loads
FT1	feedthrough	0.044	unit loads
FT2	feedthrough	0.047	unit loads

Logic Diagram



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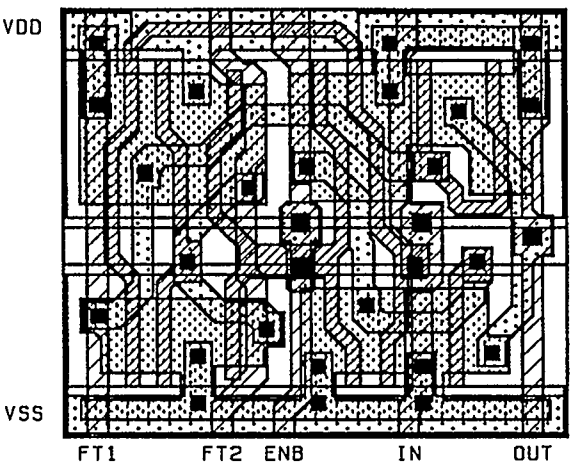
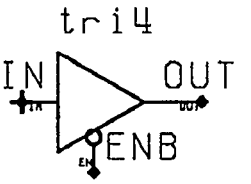


NAME: tri4
SYNOPSIS: high power tristate buffer: positive output (OUT): active-low enable (ENB)

PROPERTIES
DIMENSIONS: 81 * 63 lambda (9 * 7 pitches)
FEEDTHROUGHS: 3
INTERFACE:

IN	input	1.412	unit loads
ENB	enable	1.335	unit loads
OUT	output	0.101	unit loads
FT1	feedthrough	0.044	unit loads
FT2	feedthrough	0.047	unit loads
FT3	feedthrough	0.051	unit loads

Logic Diagram



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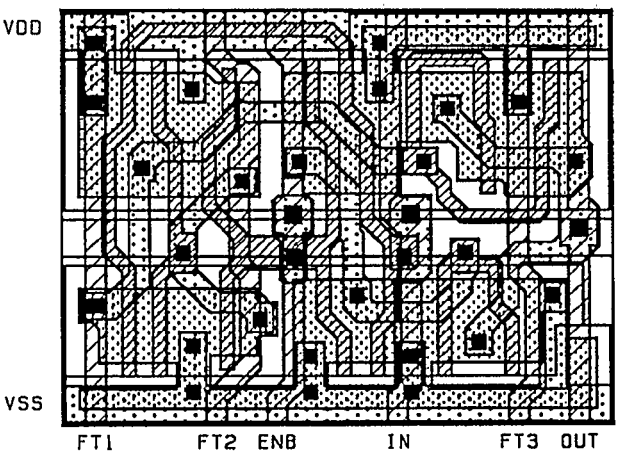
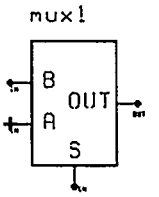


NAME: mux1
SYNOPSIS: 2 input multiplexer

PROPERTIES
DIMENSIONS: 72 * 63 lambda (8 * 7 pitches)
FEEDTHROUGHS: 2
INTERFACE:

A	input	0.059	unit loads
B	input	0.062	unit loads
S	enable	1.175	unit loads
OUT	output	0.055	unit loads
FT1	feedthrough	0.054	unit loads
FT2	feedthrough	0.052	unit loads

Logic Diagram



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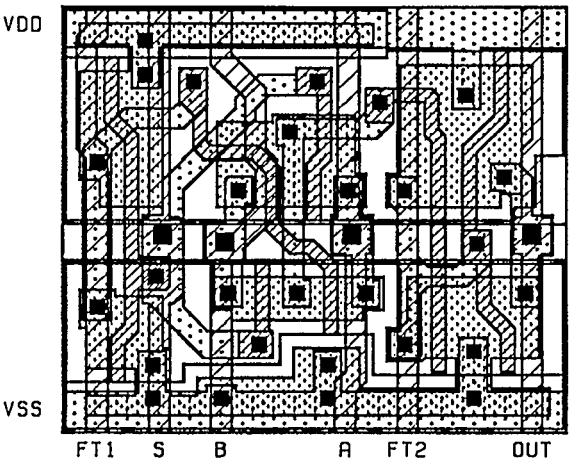
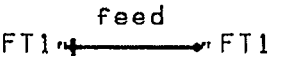


NAME: feed
SYNOPSIS: feedthrough and substrate contact

PROPERTIES
DIMENSIONS: 9 * 63 lambda (1 * 7 pitches)
FEEDTHROUGHS: 1
INTERFACE: FT1 feedthrough 0.061 unit loads

Logic Diagram



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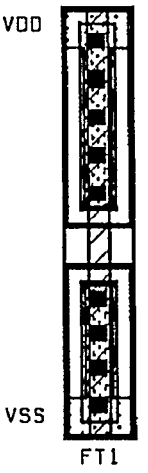

APPENDIX C: Simulation results

AVERAGE PROCESS TIMES

10 ns inputs : full load : nominal temperature : all times in ns

COMBINATIONAL LOGIC

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
invm		3.6	3.4	2.6	2.1
invl		3.6	3.4	2.6	2.1
nand2		3.9	3.9	2.7	2.1
nand3		4.1	4.8	2.8	2.5
nand4		4.4	4.9	3.1	2.3
nand5		4.7	5.8	3.2	2.7
nand6		4.8	6.7	3.2	3.1
and2		2.1	1.5	1.9	2.2
and3		2.2	1.5	2.2	2.3
and4		2.3	1.6	2.5	2.4
nor2		4.8	3.7	3.1	2.0
nor3		6.1	3.9	3.5	2.1
nor4		7.3	4.0	4.0	2.2
nor5		9.7	4.1	5.2	2.1
nor6		10.0	4.3	5.3	2.3
or2		2.1	1.7	1.9	2.4
or3		2.1	1.8	1.9	2.7
or4		2.2	1.9	2.0	3.3
xor2		5.0	5.2	3.1	3.3
xnor2		5.1	4.1	3.1	2.8
tran1	EN/ENB to OUT	4.7	4.1	1.6	1.5
	IN to OUT	8.3	7.9	0.7	0.8
tran2	EN to OUT	2.9	3.3	1.2	1.2
	IN to OUT	8.3	7.8	0.7	0.7
tran3	ENB to OUT	4.0	2.6	1.4	1.6
	IN to OUT	8.3	7.9	0.6	0.7

AVERAGE PROCESS TIMES
10 ns inputs : full load : nominal temperature : all times in ns

LATCHES

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
latch1	CK to Q	1.8	1.5	2.0	2.2
latch2	CK to Q	1.9	1.6	2.2	2.2
	RB to Q	---	1.6	---	2.0
latch3	CK to Q	2.1	1.8	3.0	3.4
	CK to QB	2.2	1.6	2.2	1.8
latch4	CK to Q	2.3	2.0	3.7	3.5
	CK to QB	3.9	2.5	2.2	2.2
	RB to Q	---	2.0	---	4.0
	RB to QB	3.9	---	2.6	---
latch5	CK to QB	2.2	1.6	2.2	1.7
latch6	CK to QB	3.9	2.5	2.2	2.2
	RB to QB	3.9	---	2.6	---
latchA	CKB to Q	1.9	1.4	2.2	2.5
latchB	CKB to Q	1.9	1.6	2.4	2.6
	RB to Q	---	1.6	---	2.0
latchC	CKB to Q	2.1	1.8	3.4	3.7
	CKB to QB	2.1	1.7	2.5	2.1
latchD	CKB to Q	2.3	2.0	4.0	3.8
	CKB to QB	3.9	2.6	2.5	2.5
	RB to Q	---	2.0	---	4.0
	RB to QB	3.9	---	2.6	---
latchE	CKB to QB	2.1	1.7	2.5	2.0
latchF	CKB to QB	3.9	2.6	2.5	2.4
	RB to QB	3.9	---	2.6	---

AVERAGE PROCESS TIMES

10 ns inputs : full load : nominal temperature : all times in ns

FLIP-FLOPS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
dflop1	CK to Q	2.1	1.7	2.7	2.5
dflop2	CK to Q	2.1	1.8	2.8	2.5
	RB to Q	---	1.8	---	2.8
dflop3	CK to Q	2.7	2.4	2.8	2.8
	SB to Q	2.7	---	2.3	---
dflop4	CK to Q	2.9	2.7	2.9	3.0
	RB to Q	---	2.7	---	3.2
	SB to Q	2.9	---	2.3	---
dflop5	CK to Q	2.1	1.6	2.8	2.6
	CK to QB	2.1	1.8	3.9	4.0
dflop6	CK to Q	2.1	1.8	2.8	2.6
	CK to QB	3.2	2.5	3.9	4.4
	RB to Q	---	1.8	---	2.8
	RB to QB	3.2	---	2.4	---
dflop7	CK to Q	2.7	2.4	2.8	2.9
	CK to QB	2.3	1.7	4.4	4.0
	SB to Q	2.7	---	2.3	---
	SB to QB	---	1.7	---	3.3
dflop8	CK to Q	2.9	2.7	2.9	3.0
	CK to QB	3.3	2.6	4.6	4.4
	RB to Q	---	2.7	---	3.2
	RB to QB	3.3	---	2.4	---
	SB to Q	2.9	---	2.3	---
	SB to QB	---	2.6	---	3.7
rsff	RB to Q	---	2.7	---	4.6
	RB to QB	3.9	---	3.0	---
	SB to Q	3.9	---	3.0	---
	SB to QB	---	2.7	---	4.6

AVERAGE PROCESS TIMES

10 ns inputs : full load : nominal temperature : all times in ns

SIGNAL CONDITIONERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
buf1	IN to OUT	2.3	2.1	3.8	4.1
	IN to OUTB	3.8	3.5	2.7	2.2
buf2	IN to OUT	2.5	2.2	3.8	4.4
	IN to OUTB	4.0	3.6	2.9	2.2
buf3	IN to OUT	2.1	1.7	1.6	2.3
buf4	IN to OUT	2.2	1.7	1.6	2.3
tri1	IN to OUT	1.7	1.6	1.8	2.3
	EN to OUT	1.7	1.6	1.3	1.5
tri2	IN to OUT	2.1	1.6	2.2	2.5
	EN to OUT	2.1	1.6	1.6	1.5
tri3	IN to OUT	1.7	1.6	1.8	2.3
	ENB to OUT	1.7	1.6	2.0	2.4
tri4	IN to OUT	2.1	1.6	2.2	2.5
	ENB to OUT	2.1	1.6	2.3	2.5

MUXES AND DECODERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
mux1	A to OUT	1.9	1.5	1.7	2.2
	B to OUT	1.9	1.5	1.7	2.2
	S to OUT	1.9	1.5	2.5	2.5

SLOWEST PROCESS TIMES
10 ns inputs : full load : nominal temperature : all times in ns

COMBINATIONAL LOGIC

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
invm		4.5	4.3	3.2	3.4
invl		4.5	4.3	3.3	3.4
nand2		4.9	5.1	3.6	3.6
nand3		5.2	6.5	3.7	4.3
nand4		5.7	6.6	4.2	4.2
nand5		6.0	8.0	4.4	4.9
nand6		6.3	9.5	4.5	5.7
and2		3.3	2.5	3.6	3.5
and3		3.4	2.5	4.1	3.8
and4		3.6	2.6	4.6	4.0
nor2		6.5	4.6	4.2	3.5
nor3		8.7	4.9	5.0	3.7
nor4		10.6	5.1	5.8	3.9
nor5		14.8	5.3	7.8	3.9
nor6		15.4	5.6	8.2	4.1
or2		3.2	2.8	3.6	3.8
or3		3.3	3.0	3.8	4.5
or4		3.3	3.3	4.0	5.4
xor2		6.6	6.4	4.2	5.0
xnor2		6.3	5.1	3.9	3.9
tran1	EN/ENB to OUT	5.7	5.3	2.7	2.8
	IN to OUT	8.6	8.0	1.3	1.4
tran2	EN to OUT	4.1	4.1	2.5	2.5
	IN to OUT	8.7	7.9	1.2	1.3
tran3	ENB to OUT	5.1	3.7	2.3	2.4
	IN to OUT	8.5	7.9	1.1	1.3

SLOWEST PROCESS TIMES
10 ns inputs : full load : nominal temperature : all times in ns

LATCHES

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
latch1	CK to Q	3.0	2.6	4.2	4.5
latch2	CK to Q	3.0	2.7	4.5	4.7
	RB to Q	---	2.7	---	3.3
latch3	CK to Q	3.3	3.1	6.0	6.5
	CK to QB	3.5	2.8	4.1	3.9
latch4	CK to Q	3.7	3.2	7.2	6.6
	CK to QB	4.9	4.4	4.2	4.7
	RB to Q	---	3.2	---	6.0
	RB to QB	4.9	---	3.5	---
latch5	CK to QB	3.6	2.9	4.0	3.8
latch6	CK to QB	5.0	4.4	4.1	4.6
	RB to QB	5.0	---	3.5	---
latchA	CKB to Q	3.0	2.6	3.9	4.5
latchB	CKB to Q	3.1	2.7	4.2	4.7
	RB to Q	---	2.7	---	3.3
latchC	CKB to Q	3.3	3.1	5.8	6.5
	CKB to QB	3.4	3.0	4.1	3.6
latchD	CKB to Q	3.7	3.2	6.9	6.6
	CKB to QB	4.9	4.4	4.2	4.4
	RB to Q	---	3.2	---	6.0
	RB to QB	4.9	---	3.5	---
latchE	CKB to QB	3.5	3.0	4.0	3.6
latchF	CKB to QB	5.0	4.5	4.1	4.3
	RB to QB	5.0	---	3.5	---

SLOWEST PROCESS TIMES
10 ns inputs : full load : nominal temperature : all times in ns

FLIP-FLOPS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
dflop1	CK to Q	3.6	3.2	5.3	5.2
dflop2	CK to Q	3.6	3.2	5.4	5.2
	RB to Q	---	3.2	---	4.9
dflop3	CK to Q	4.1	4.2	5.4	5.7
	SB to Q	4.1	---	3.5	---
dflop4	CK to Q	4.4	4.7	5.6	6.0
	RB to Q	---	4.7	---	5.6
	SB to Q	4.4	---	3.5	---
dflop5	CK to Q	3.5	3.1	5.4	5.3
	CK to QB	3.3	3.1	7.5	7.8
dflop6	CK to Q	3.5	3.2	5.5	5.2
	CK to QB	4.4	4.3	7.6	8.4
	RB to Q	---	3.2	---	4.9
	RB to QB	4.4	---	3.2	---
dflop7	CK to Q	4.1	4.1	5.5	5.8
	CK to QB	3.7	2.9	8.3	7.8
	SB to Q	4.1	---	3.5	---
	SB to QB	---	2.9	---	5.6
dflop8	CK to Q	4.3	4.7	5.6	6.0
	CK to QB	4.5	4.3	8.8	8.6
	RB to Q	---	4.7	---	5.7
	RB to QB	4.5	---	3.2	---
	SB to Q	4.3	---	3.4	---
	SB to QB	---	4.3	---	6.3
rsff	RB to Q	---	4.4	---	7.0
	RB to QB	5.3	---	4.0	---
	SB to Q	5.3	---	3.9	---
	SB to QB	---	4.4	---	7.0

SLOWEST PROCESS TIMES

10 ns inputs : full load : nominal temperature : all times in ns

SIGNAL CONDITIONERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
buf1	IN to OUT	3.5	3.4	6.1	6.1
	IN to OUTB	4.8	4.6	3.5	3.7
buf2	IN to OUT	3.7	3.5	6.1	6.5
	IN to OUTB	5.3	4.6	3.8	3.6
buf3	IN to OUT	3.2	2.9	3.1	3.5
buf4	IN to OUT	3.3	2.9	3.1	3.5
tri1	IN to OUT	2.5	2.7	3.2	3.6
	EN to OUT	2.5	2.7	2.3	2.8
tri2	IN to OUT	3.2	2.7	3.9	3.8
	EN to OUT	3.2	2.7	2.7	2.9
tri3	IN to OUT	2.5	2.7	3.2	3.6
	ENB to OUT	2.5	2.7	3.1	3.4
tri4	IN to OUT	3.2	2.7	3.9	3.8
	ENB to OUT	3.2	2.7	3.5	3.5

MUXES AND DECODERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
mux1	A to OUT	2.9	2.5	3.5	3.6
	B to OUT	2.9	2.5	3.5	3.6
	S to OUT	2.9	2.5	4.1	4.3

AVERAGE PROCESS TIMES

5 ns inputs : full load : nominal temperature : all times in ns

COMBINATIONAL LOGIC

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
invm		2.6	2.3	1.9	1.6
invl		2.6	2.4	1.9	1.7
nand2		2.8	3.0	2.0	1.8
nand3		2.9	4.0	2.0	2.2
nand4		3.2	4.1	2.3	2.1
nand5		3.4	5.0	2.3	2.6
nand6		3.5	6.0	2.4	3.0
and2		2.0	1.4	1.7	1.7
and3		2.1	1.4	2.0	1.9
and4		2.2	1.4	2.2	1.9
nor2		4.1	2.5	2.4	1.7
nor3		5.4	2.6	3.0	1.7
nor4		6.7	2.7	3.5	1.8
nor5		9.2	2.8	4.7	1.8
nor6		9.6	2.9	4.9	1.8
or2		2.0	1.6	1.7	1.9
or3		2.1	1.6	1.8	2.2
or4		2.1	1.8	1.8	2.7
xor2		3.9	4.1	2.2	2.7
xnor2		4.7	3.2	2.7	2.3
tran1	EN/ENB to OUT	3.2	2.8	1.4	1.4
	IN to OUT	4.5	4.1	0.7	0.8
tran2	EN to OUT	2.4	2.2	1.2	1.2
	IN to OUT	4.5	4.0	0.7	0.7
tran3	ENB to OUT	2.7	1.9	1.3	1.3
	IN to OUT	4.4	4.0	0.7	0.7

AVERAGE PROCESS TIMES

5 ns inputs : full load : nominal temperature : all times in ns

LATCHES

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
latch1	CK to Q	1.9	1.4	1.9	1.9
latch2	CK to Q	1.9	1.5	2.1	2.0
	RB to Q	---	1.5	---	1.6
latch3	CK to Q	2.1	1.8	2.9	3.2
	CK to QB	2.1	1.5	1.9	1.7
latch4	CK to Q	2.3	1.8	3.7	3.2
	CK to QB	2.8	2.5	2.0	2.1
	RB to Q	---	1.8	---	3.2
	RB to QB	2.8	---	1.9	---
latch5	CK to QB	2.1	1.6	1.9	1.7
latch6	CK to QB	2.8	2.5	2.0	2.1
	RB to QB	2.8	---	2.0	---
latchA	CKB to Q	1.9	1.4	2.0	2.1
latchB	CKB to Q	1.9	1.5	2.1	2.2
	RB to Q	---	1.5	---	1.6
latchC	CKB to Q	2.1	1.8	3.1	3.4
	CKB to QB	2.1	1.6	2.1	1.8
latchD	CKB to Q	2.3	1.8	3.8	3.4
	CKB to QB	2.8	2.5	2.2	2.2
	RB to Q	---	1.8	---	3.2
	RB to QB	2.8	---	1.9	---
latchE	CKB to QB	2.1	1.6	2.1	1.8
latchF	CKB to QB	2.8	2.6	2.2	2.2
	RB to QB	2.8	---	2.0	---

AVERAGE PROCESS TIMES

5 ns inputs : full load : nominal temperature : all times in ns

FLIP-FLOPS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
dflop1	CK to Q	2.1	1.7	2.5	2.3
dflop2	CK to Q	2.1	1.7	2.6	2.3
	RB to Q	---	1.7	---	2.3
dflop3	CK to Q	2.2	2.4	2.5	2.6
	SB to Q	2.2	---	1.8	---
dflop4	CK to Q	2.2	2.7	2.6	2.8
	RB to Q	---	2.7	---	2.8
	SB to Q	2.2	---	1.8	---
dflop5	CK to Q	2.1	1.6	2.5	2.3
	CK to QB	2.1	1.8	3.6	3.8
dflop6	CK to Q	2.1	1.7	2.6	2.3
	CK to QB	2.3	2.5	3.7	4.1
	RB to Q	---	1.7	---	2.3
	RB to QB	2.3	---	1.8	---
dflop7	CK to Q	2.2	2.4	2.6	2.7
	CK to QB	2.3	1.7	4.2	3.7
	SB to Q	2.2	---	1.8	---
	SB to QB	---	1.7	---	2.8
dflop8	CK to Q	2.2	2.7	2.6	2.8
	CK to QB	2.5	2.5	4.4	4.2
	RB to Q	---	2.7	---	2.8
	RB to QB	2.5	---	1.8	---
	SB to Q	2.2	---	1.8	---
	SB to QB	---	2.5	---	3.3
rsff	RB to Q	---	2.6	---	3.7
	RB to QB	3.0	---	2.2	---
	SB to Q	3.0	---	2.2	---
	SB to QB	---	2.6	---	3.8

AVERAGE PROCESS TIMES

5 ns inputs : full load : nominal temperature : all times in ns

SIGNAL CONDITIONERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
buf1	IN to OUT	2.2	1.9	3.2	3.3
	IN to OUTB	2.7	2.5	2.0	1.7
buf2	IN to OUT	2.3	2.1	3.2	3.5
	IN to OUTB	3.0	2.5	2.1	1.7
buf3	IN to OUT	2.0	1.6	1.5	1.8
buf4	IN to OUT	2.1	1.6	1.5	1.8
tri1	IN to OUT	1.6	1.5	1.5	1.8
	EN to OUT	1.6	1.5	1.2	1.4
tri2	IN to OUT	2.0	1.5	1.9	1.9
	EN to OUT	2.0	1.5	1.4	1.3
tri3	IN to OUT	1.6	1.5	1.5	1.8
	ENB to OUT	1.6	1.5	1.6	1.6
tri4	IN to OUT	2.0	1.5	1.8	1.8
	ENB to OUT	2.0	1.5	1.7	1.6

MUXES AND DECODERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
mux1	A to OUT	1.8	1.4	1.6	1.8
	B to OUT	1.8	1.4	1.6	1.8
	S to OUT	1.8	1.4	2.1	2.1

SLOWEST PROCESS TIMES
5 ns inputs : full load : nominal temperature : all times in ns

COMBINATIONAL LOGIC

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
invm		3.5	3.2	2.5	2.6
invl		3.5	3.3	2.5	2.6
nand2		3.8	4.4	2.7	3.1
nand3		4.1	6.0	2.8	3.8
nand4		4.7	6.2	3.2	3.9
nand5		5.0	7.7	3.4	4.7
nand6		5.2	9.2	3.5	5.5
and2		3.2	2.4	3.1	3.0
and3		3.3	2.4	3.6	3.2
and4		3.5	2.5	4.2	3.4
nor2		6.0	3.4	3.5	2.7
nor3		8.3	3.7	4.6	2.9
nor4		10.3	4.0	5.5	3.0
nor5		14.6	4.1	7.7	3.0
nor6		15.3	4.5	8.2	3.2
or2		3.2	2.7	3.1	3.3
or3		3.2	2.9	3.3	4.0
or4		3.2	3.2	3.5	5.0
xor2		5.8	5.6	3.4	4.6
xnor2		6.7	4.5	3.8	3.3
tran1	EN/ENB to OUT	4.2	3.7	2.1	2.2
	IN to OUT	5.1	4.6	1.4	1.4
tran2	EN to OUT	3.6	3.0	2.1	2.1
	IN to OUT	5.1	4.4	1.3	1.4
tran3	ENB to OUT	3.6	3.0	1.9	2.0
	IN to OUT	4.9	4.5	1.2	1.3

SLOWEST PROCESS TIMES

5 ns inputs ; full load ; nominal temperature ; all times in ns

LATCHES

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
latch1	CK to Q	3.0	2.6	3.7	3.9
latch2	CK to Q	3.0	2.7	4.1	4.1
	RB to Q	---	2.7	---	2.9
latch3	CK to Q	3.3	3.1	5.7	5.9
	CK to QB	3.5	2.8	3.5	3.5
latch4	CK to Q	3.7	3.1	6.8	6.0
	CK to QB	3.9	4.4	3.6	4.3
	RB to Q	---	3.1	---	5.1
	RB to QB	3.9	---	2.7	---
latch5	CK to QB	3.5	2.9	3.4	3.4
latch6	CK to QB	3.9	4.4	3.6	4.3
	RB to QB	3.9	---	2.7	---
latchA	CKB to Q	3.0	2.6	3.5	4.1
latchB	CKB to Q	3.1	2.7	3.8	4.2
	RB to Q	---	2.7	---	2.9
latchC	CKB to Q	3.3	3.1	5.4	6.0
	CKB to QB	3.4	2.9	3.6	3.2
latchD	CKB to Q	3.7	3.1	6.6	6.2
	CKB to QB	3.9	4.4	3.7	4.0
	RB to Q	---	3.1	---	5.1
	RB to QB	3.9	---	2.7	---
latchE	CKB to QB	3.5	3.0	3.6	3.2
latchF	CKB to QB	3.9	4.5	3.7	4.0
	RB to QB	3.9	---	2.7	---

SLOWEST PROCESS TIMES
5 ns inputs : full load : nominal temperature : all times in ns

FLIP-FLOPS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
dflop1	CK to Q	3.6	3.1	4.7	4.6
dflop2	CK to Q	3.6	3.1	4.9	4.6
	RB to Q	---	3.1	---	4.3
dflop3	CK to Q	3.7	4.2	4.9	5.1
	SB to Q	3.7	---	2.7	---
dflop4	CK to Q	3.7	4.7	5.0	5.4
	RB to Q	---	4.7	---	5.1
	SB to Q	3.7	---	2.6	---
dflop5	CK to Q	3.5	3.1	4.8	4.7
	CK to QB	3.3	3.1	6.9	7.2
dflop6	CK to Q	3.6	3.1	4.9	4.7
	CK to QB	3.6	4.3	7.1	7.8
	RB to Q	---	3.1	---	4.3
	RB to QB	3.6	---	2.5	---
dflop7	CK to Q	3.7	4.1	4.9	5.2
	CK to QB	3.7	2.9	7.7	7.2
	SB to Q	3.7	---	2.7	---
	SB to QB	---	2.9	---	4.8
dflop8	CK to Q	3.7	4.7	5.0	5.5
	CK to QB	3.9	4.3	8.2	8.0
	RB to Q	---	4.7	---	5.1
	RB to QB	3.9	---	2.5	---
	SB to Q	3.7	---	2.6	---
	SB to QB	---	4.3	---	5.5
rsff	RB to Q	---	4.3	---	6.0
	RB to QB	4.4	---	3.0	---
	SB to Q	4.4	---	3.0	---
	SB to QB	---	4.3	---	6.0

SLOWEST PROCESS TIMES
5 ns inputs : full load : nominal temperature : all times in ns

SIGNAL CONDITIONERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
buf1	IN to OUT	3.5	3.3	5.1	5.2
	IN to OUTB	3.8	3.5	2.6	2.8
buf2	IN to OUT	3.6	3.5	5.1	5.5
	IN to OUTB	4.3	3.6	2.9	2.8
buf3	IN to OUT	3.1	2.9	2.7	3.1
buf4	IN to OUT	3.2	2.9	2.8	3.1
tri1	IN to OUT	2.4	2.6	2.7	3.1
	EN to OUT	2.4	2.6	2.0	2.6
tri2	IN to OUT	3.1	2.6	3.3	3.2
	EN to OUT	3.1	2.6	2.4	2.7
tri3	IN to OUT	2.4	2.6	2.7	3.1
	ENB to OUT	2.4	2.6	2.6	2.6
tri4	IN to OUT	3.1	2.6	3.3	3.2
	ENB to OUT	3.1	2.6	3.0	2.8

MUXES AND DECODERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
mux1	A to OUT	2.9	2.4	3.1	3.2
	B to OUT	2.9	2.4	3.1	3.2
	S to OUT	2.9	2.4	3.7	3.8

AVERAGE PROCESS TIMES

5 ns inputs : half load : nominal temperature : all times in ns

COMBINATIONAL LOGIC

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
invm		1.9	1.7	1.3	1.1
invl		1.9	1.8	1.3	1.1
nand2		2.1	2.0	1.5	1.1
nand3		2.2	2.6	1.5	1.4
nand4		2.4	2.7	1.7	1.4
nand5		2.6	3.2	1.8	1.7
nand6		2.7	3.8	1.8	2.0
and2		1.2	0.9	1.3	1.4
and3		1.3	0.9	1.5	1.5
and4		1.3	1.0	1.8	1.6
nor2		2.6	1.9	1.7	1.1
nor3		3.3	2.1	2.0	1.2
nor4		4.0	2.2	2.3	1.3
nor5		5.6	2.2	3.1	1.2
nor6		5.9	2.4	3.2	1.3
or2		1.2	1.0	1.3	1.5
or3		1.2	1.1	1.4	1.8
or4		1.2	1.2	1.4	2.3
xor2		2.5	2.7	1.8	1.9
xnor2		3.0	2.3	2.0	1.7
tran1	EN/ENB to OUT	2.5	2.1	0.8	0.8
	IN to OUT	4.2	3.9	0.4	0.4
tran2	EN to OUT	1.8	1.7	0.8	0.7
	IN to OUT	4.2	3.9	0.4	0.4
tran3	ENB to OUT	2.3	1.5	0.8	1.0
	IN to OUT	4.1	3.9	0.3	0.4

AVERAGE PROCESS TIMES

5 ns inputs : half load : nominal temperature : all times in ns

LATCHES

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
latch1	CK to Q	1.1	0.9	1.5	1.6
latch2	CK to Q	1.1	0.9	1.7	1.7
	RB to Q	---	0.9	---	1.3
latch3	CK to Q	1.2	1.0	2.1	2.2
	CK to QB	1.3	1.0	1.5	1.3
latch4	CK to Q	1.3	1.1	2.5	2.3
	CK to QB	2.1	1.5	1.6	1.6
	RB to Q	---	1.1	---	2.2
	RB to QB	2.1	---	1.4	---
latch5	CK to QB	1.4	1.0	1.5	1.3
latch6	CK to QB	2.1	1.5	1.5	1.6
	RB to QB	2.1	---	1.4	---
latchA	CKB to Q	1.1	0.9	1.6	1.8
latchB	CKB to Q	1.1	0.9	1.8	1.9
	RB to Q	---	0.9	---	1.3
latchC	CKB to Q	1.2	1.0	2.2	2.4
	CKB to QB	1.3	1.1	1.7	1.5
latchD	CKB to Q	1.3	1.1	2.5	2.5
	CKB to QB	2.1	1.6	1.8	1.7
	RB to Q	---	1.1	---	2.2
	RB to QB	2.1	---	1.4	---
latchE	CKB to QB	1.3	1.1	1.7	1.4
latchF	CKB to QB	2.1	1.6	1.8	1.7
	RB to QB	2.1	---	1.4	---

AVERAGE PROCESS TIMES
5 ns inputs : half load : nominal temperature : all times in ns

FLIP-FLOPS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
dflop1	CK to Q	1.3	1.1	2.1	1.9
dflop2	CK to Q	1.4	1.2	2.2	1.9
	RB to Q	---	1.2	---	2.0
dflop3	CK to Q	1.8	1.5	2.2	2.1
	SB to Q	1.8	---	1.4	---
dflop4	CK to Q	1.9	1.7	2.2	2.2
	RB to Q	---	1.7	---	2.2
	SB to Q	1.9	---	1.4	---
dflop5	CK to Q	1.3	1.1	2.1	2.0
	CK to QB	1.2	1.0	2.7	2.8
dflop6	CK to Q	1.3	1.2	2.2	2.0
	CK to QB	1.9	1.4	2.7	3.1
	RB to Q	---	1.2	---	2.0
	RB to QB	1.9	---	1.3	---
dflop7	CK to Q	1.8	1.4	2.2	2.2
	CK to QB	1.3	1.0	3.0	2.8
	SB to Q	1.8	---	1.4	---
	SB to QB	---	1.0	---	2.1
dflop8	CK to Q	1.9	1.7	2.2	2.2
	CK to QB	1.9	1.5	3.1	3.2
	RB to Q	---	1.7	---	2.2
	RB to QB	1.9	---	1.3	---
	SB to Q	1.9	---	1.4	---
	SB to QB	---	1.5	---	2.3
rsff	RB to Q	---	1.6	---	2.6
	RB to QB	2.2	---	1.6	---
	SB to Q	2.2	---	1.6	---
	SB to QB	---	1.6	---	2.6

AVERAGE PROCESS TIMES

5 ns inputs : half load : nominal temperature : all times in ns

SIGNAL CONDITIONERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
buf1	IN to OUT	1.3	1.2	2.1	2.3
	IN to OUTB	2.0	1.9	1.5	1.2
buf2	IN to OUT	1.3	1.2	2.1	2.4
	IN to OUTB	2.2	1.9	1.6	1.2
buf3	IN to OUT	1.2	1.0	1.1	1.4
buf4	IN to OUT	1.2	1.0	1.1	1.4
tri1	IN to OUT	1.0	0.9	1.2	1.5
	EN to OUT	1.0	0.9	0.9	1.1
tri2	IN to OUT	1.2	1.0	1.5	1.5
	EN to OUT	1.2	1.0	1.0	1.1
tri3	IN to OUT	1.0	0.9	1.2	1.5
	ENB to OUT	1.0	0.9	1.4	1.4
tri4	IN to OUT	1.2	1.0	1.5	1.5
	ENB to OUT	1.2	1.0	1.5	1.4

MUXES AND DECODERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
mux1	A to OUT	1.1	0.9	1.3	1.5
	B to OUT	1.1	0.9	1.3	1.5
	S to OUT	1.1	0.9	1.8	1.8

SLOWEST PROCESS TIMES
5 ns inputs : half load : nominal temperature : all times in ns

COMBINATIONAL LOGIC

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
invm		2.4	2.2	1.7	1.8
invl		2.4	2.2	1.7	1.8
nand2		2.6	2.7	2.0	2.0
nand3		2.9	3.6	2.1	2.5
nand4		3.3	3.8	2.5	2.6
nand5		3.6	4.8	2.6	3.2
nand6		3.8	5.8	2.7	3.8
and2		1.9	1.4	2.5	2.4
and3		2.0	1.5	2.9	2.6
and4		2.2	1.5	3.4	2.8
nor2		3.6	2.5	2.4	2.0
nor3		4.9	2.7	3.0	2.1
nor4		6.3	2.9	3.7	2.3
nor5		9.0	3.1	5.1	2.3
nor6		9.7	3.3	5.6	2.4
or2		1.8	1.7	2.4	2.6
or3		1.8	1.9	2.6	3.3
or4		1.9	2.2	2.8	4.2
xor2		3.7	3.5	2.7	3.2
xnor2		4.2	2.8	2.7	2.5
tran1	EN/ENB to OUT	3.2	2.7	1.4	1.5
	IN to OUT	4.4	4.0	0.7	0.8
tran2	EN to OUT	2.7	2.2	1.6	1.5
	IN to OUT	4.4	3.9	0.7	0.7
tran3	ENB to OUT	3.0	2.2	1.3	1.5
	IN to OUT	4.3	4.0	0.6	0.7

SLOWEST PROCESS TIMES

5 ns inputs : half load : nominal temperature : all times in ns

LATCHES

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
latch1	CK to Q	1.7	1.5	3.1	3.3
latch2	CK to Q	1.8	1.6	3.5	3.4
	RB to Q	---	1.6	---	2.2
latch3	CK to Q	1.9	1.8	4.1	4.3
	CK to QB	2.2	1.8	2.8	2.8
latch4	CK to Q	2.1	1.8	4.8	4.4
	CK to QB	2.8	2.7	3.0	3.3
	RB to Q	---	1.8	---	3.4
	RB to QB	2.8	---	2.0	---
latch5	CK to QB	2.3	1.8	2.8	2.8
latch6	CK to QB	2.8	2.8	2.9	3.3
	RB to QB	2.8	---	2.0	---
latchA	CKB to Q	1.7	1.5	2.9	3.4
latchB	CKB to Q	1.8	1.6	3.2	3.6
	RB to Q	---	1.6	---	2.2
latchC	CKB to Q	1.9	1.8	3.9	4.4
	CKB to QB	2.2	1.8	3.0	2.6
latchD	CKB to Q	2.1	1.8	4.6	4.5
	CKB to QB	2.8	2.7	3.1	3.1
	RB to Q	---	1.8	---	3.4
	RB to QB	2.8	---	2.0	---
latchE	CKB to QB	2.2	1.9	2.9	2.5
latchF	CKB to QB	2.8	2.8	3.1	3.0
	RB to QB	2.8	---	2.0	---

SLOWEST PROCESS TIMES
5 ns inputs : half load : nominal temperature : all times in ns

FLIP-FLOPS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
dflop1	CK to Q	2.3	2.1	4.1	3.9
dflop2	CK to Q	2.4	2.1	4.2	3.9
	RB to Q	---	2.1	---	3.6
dflop3	CK to Q	2.8	2.7	4.2	4.3
	SB to Q	2.8	---	2.0	---
dflop4	CK to Q	2.8	3.0	4.3	4.4
	RB to Q	---	3.0	---	4.1
	SB to Q	2.8	---	2.0	---
dflop5	CK to Q	2.3	2.0	4.1	4.0
	CK to QB	1.9	1.8	5.3	5.5
dflop6	CK to Q	2.3	2.1	4.2	4.0
	CK to QB	2.5	2.5	5.4	6.0
	RB to Q	---	2.1	---	3.6
	RB to QB	2.5	---	1.8	---
dflop7	CK to Q	2.7	2.6	4.3	4.3
	CK to QB	2.1	1.7	5.8	5.6
	SB to Q	2.7	---	2.0	---
	SB to QB	---	1.7	---	3.3
dflop8	CK to Q	2.8	2.9	4.4	4.5
	CK to QB	2.5	2.5	6.1	6.2
	RB to Q	---	2.9	---	4.1
	RB to QB	2.5	---	1.8	---
	SB to Q	2.8	---	2.0	---
	SB to QB	---	2.5	---	3.7
rsff	RB to Q	---	2.7	---	4.1
	RB to QB	3.0	---	2.2	---
	SB to Q	3.0	---	2.2	---
	SB to QB	---	2.7	---	4.1

SLOWEST PROCESS TIMES

5 ns inputs : half load : nominal temperature : all times in ns

SIGNAL CONDITIONERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
buf1	IN to OUT	2.0	1.9	3.4	3.5
	IN to OUTB	2.7	2.5	2.0	2.1
buf2	IN to OUT	2.0	1.9	3.4	3.6
	IN to OUTB	3.0	2.5	2.1	2.0
buf3	IN to OUT	1.8	1.7	2.1	2.3
buf4	IN to OUT	1.8	1.6	2.1	2.3
tri1	IN to OUT	1.5	1.6	2.2	2.4
	EN to OUT	1.5	1.6	1.5	2.1
tri2	IN to OUT	1.9	1.6	2.6	2.6
	EN to OUT	1.9	1.6	1.8	2.2
tri3	IN to OUT	1.5	1.6	2.2	2.4
	ENB to OUT	1.5	1.6	2.2	2.1
tri4	IN to OUT	1.9	1.6	2.6	2.6
	ENB to OUT	1.9	1.6	2.4	2.2

MUXES AND DECODERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
mux1	A to OUT	1.7	1.4	2.5	2.6
	B to OUT	1.7	1.4	2.5	2.5
	S to OUT	1.7	1.4	3.1	3.2

AVERAGE PROCESS TIMES

3 ns inputs : half load : nominal temperature : all times in ns

COMBINATIONAL LOGIC

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
invm		1.5	1.3	1.0	0.9
invl		1.5	1.3	1.0	0.9
nand2		1.6	1.7	1.1	1.0
nand3		1.8	2.2	1.2	1.3
nand4		2.0	2.4	1.4	1.3
nand5		2.1	2.9	1.5	1.6
nand6		2.2	3.5	1.5	2.0
and2		1.2	0.8	1.2	1.2
and3		1.2	0.9	1.4	1.3
and4		1.3	0.9	1.7	1.4
nor2		2.3	1.4	1.4	1.0
nor3		3.1	1.6	1.8	1.0
nor4		3.8	1.7	2.1	1.1
nor5		5.4	1.7	2.9	1.1
nor6		5.8	1.8	3.2	1.1
or2		1.1	0.9	1.2	1.3
or3		1.2	1.0	1.3	1.6
or4		1.2	1.2	1.3	2.0
xor2		2.2	2.3	1.6	1.7
xnor2		2.7	1.9	1.7	1.5
tran1	EN/ENB to OUT	1.9	1.6	0.8	0.7
	IN to OUT	2.7	2.4	0.4	0.4
tran2	EN to OUT	1.5	1.2	0.7	0.7
	IN to OUT	2.7	2.4	0.4	0.4
tran3	ENB to OUT	1.7	1.2	0.7	0.8
	IN to OUT	2.6	2.4	0.3	0.4

AVERAGE PROCESS TIMES
3 ns inputs : half load : nominal temperature : all times in ns

LATCHES

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
latch1	CK to Q	1.1	0.9	1.5	1.5
latch2	CK to Q	1.1	0.9	1.6	1.5
	RB to Q	---	0.9	---	1.1
latch3	CK to Q	1.1	1.0	2.0	2.1
	CK to QB	1.3	1.0	1.4	1.2
latch4	CK to Q	1.3	1.1	2.4	2.1
	CK to QB	1.7	1.5	1.4	1.5
	RB to Q	---	1.1	---	1.9
	RB to QB	1.7	---	1.2	---
latch5	CK to QB	1.3	1.0	1.4	1.2
latch6	CK to QB	1.7	1.5	1.4	1.5
	RB to QB	1.7	---	1.2	---
latchA	CKB to Q	1.1	0.9	1.5	1.6
latchB	CKB to Q	1.1	0.9	1.6	1.7
	RB to Q	---	0.9	---	1.1
latchC	CKB to Q	1.2	1.0	2.0	2.2
	CKB to QB	1.3	1.0	1.5	1.3
latchD	CKB to Q	1.3	1.1	2.4	2.3
	CKB to QB	1.7	1.5	1.6	1.5
	RB to Q	---	1.1	---	1.9
	RB to QB	1.7	---	1.2	---
latchE	CKB to QB	1.3	1.0	1.5	1.3
latchF	CKB to QB	1.7	1.6	1.6	1.5
	RB to QB	1.7	---	1.2	---

AVERAGE PROCESS TIMES

3 ns inputs : half load : nominal temperature : all times in ns

FLIP-FLOPS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
dflop1	CK to Q	1.3	1.1	1.9	1.8
dflop2	CK to Q	1.4	1.1	2.0	1.8
	RB to Q	---	1.1	---	1.7
dflop3	CK to Q	1.5	1.5	2.0	2.0
	SB to Q	1.5	---	1.1	---
dflop4	CK to Q	1.5	1.6	2.1	2.1
	RB to Q	---	1.6	---	2.0
	SB to Q	1.5	---	1.1	---
dflop5	CK to Q	1.3	1.1	2.0	1.8
	CK to QB	1.2	1.0	2.6	2.7
dflop6	CK to Q	1.3	1.1	2.0	1.8
	CK to QB	1.4	1.4	2.6	2.9
	RB to Q	---	1.1	---	1.8
	RB to QB	1.4	---	1.0	---
dflop7	CK to Q	1.5	1.5	2.0	2.0
	CK to QB	1.3	1.0	2.9	2.7
	SB to Q	1.5	---	1.1	---
	SB to QB	---	1.0	---	1.8
dflop8	CK to Q	1.5	1.6	2.1	2.1
	CK to QB	1.5	1.4	3.0	3.0
	RB to Q	---	1.6	---	2.0
	RB to QB	1.5	---	1.0	---
	SB to Q	1.5	---	1.1	---
	SB to QB	---	1.4	---	2.0
rsff	RB to Q	---	1.6	---	2.3
	RB to QB	1.8	---	1.3	---
	SB to Q	1.8	---	1.3	---
	SB to QB	---	1.6	---	2.3

AVERAGE PROCESS TIMES

3 ns inputs : half load : nominal temperature : all times in ns

SIGNAL CONDITIONERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
buf1	IN to OUT	1.2	1.1	1.8	1.9
	IN to OUTB	1.6	1.5	1.1	1.0
buf2	IN to OUT	1.3	1.1	1.8	2.0
	IN to OUTB	1.8	1.5	1.2	1.0
buf3	IN to OUT	1.1	0.9	1.0	1.2
buf4	IN to OUT	1.2	1.0	1.0	1.2
tri1	IN to OUT	1.0	0.9	1.1	1.2
	EN to OUT	1.0	0.9	0.8	0.9
tri2	IN to OUT	1.2	0.9	1.3	1.3
	EN to OUT	1.2	0.9	0.9	1.0
tri3	IN to OUT	0.9	0.9	1.1	1.2
	ENB to OUT	0.9	0.9	1.1	1.0
tri4	IN to OUT	1.2	0.9	1.3	1.3
	ENB to OUT	1.2	0.9	1.3	1.1

MUXES AND DECODERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
mux1	A to OUT	1.1	0.8	1.2	1.3
	B to OUT	1.1	0.8	1.2	1.3
	S to OUT	1.1	0.8	1.6	1.6

SLOWEST PROCESS TIMES
3 ns inputs : half load : nominal temperature : all times in ns

COMBINATIONAL LOGIC

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
invm		2.0	1.8	1.4	1.5
invl		2.0	1.8	1.4	1.5
nand2		2.2	2.5	1.6	1.8
nand3		2.5	3.5	1.7	2.4
nand4		2.9	3.7	2.1	2.5
nand5		3.2	4.7	2.2	3.1
nand6		3.5	5.8	2.3	3.8
and2		1.8	1.4	2.2	2.1
and3		2.0	1.4	2.7	2.3
and4		2.1	1.5	3.3	2.4
nor2		3.4	2.0	2.1	1.6
nor3		4.8	2.3	2.9	1.8
nor4		6.2	2.5	3.6	1.9
nor5		9.0	2.6	5.1	1.9
nor6		9.7	2.9	5.6	2.0
or2		1.8	1.6	2.2	2.4
or3		1.8	1.8	2.3	3.1
or4		1.9	2.1	2.5	4.1
xor2		3.4	3.2	2.6	3.0
xnor2		4.0	2.6	2.3	2.2
tran1	EN/ENB to OUT	2.5	2.1	1.2	1.2
	IN to OUT	3.0	2.7	0.7	0.8
tran2	EN to OUT	2.4	1.7	1.4	1.3
	IN to OUT	3.0	2.6	0.7	0.7
tran3	ENB to OUT	2.3	1.9	1.1	1.3
	IN to OUT	3.9	2.6	0.7	0.7

SLOWEST PROCESS TIMES
3 ns inputs : half load : nominal temperature : all times in ns

LATCHES

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
latch1	CK to Q	1.7	1.5	2.9	3.0
latch2	CK to Q	1.8	1.5	3.2	3.1
	RB to Q	---	1.5	---	2.0
latch3	CK to Q	1.9	1.8	3.9	3.9
	CK to QB	2.2	1.8	2.5	2.6
latch4	CK to Q	2.1	1.8	4.6	4.1
	CK to QB	2.4	2.7	2.6	3.1
	RB to Q	---	1.8	---	3.0
	RB to QB	2.4	---	1.6	---
latch5	CK to QB	2.2	1.8	2.5	2.6
latch6	CK to QB	2.4	2.8	2.6	3.1
	RB to QB	2.4	---	1.6	---
latchA	CKB to Q	1.7	1.5	2.6	3.1
latchB	CKB to Q	1.8	1.5	3.0	3.3
	RB to Q	---	1.5	---	2.0
latchC	CKB to Q	1.9	1.8	3.6	4.1
	CKB to QB	2.2	1.8	2.7	2.3
latchD	CKB to Q	2.1	1.8	4.3	4.2
	CKB to QB	2.4	2.7	2.8	2.8
	RB to Q	---	1.8	---	3.0
	RB to QB	2.4	---	1.6	---
latchE	CKB to QB	2.2	1.9	2.7	2.3
latchF	CKB to QB	2.4	2.8	2.8	2.8
	RB to QB	2.4	---	1.6	---

SLOWEST PROCESS TIMES
3 ns inputs : half load : nominal temperature : all times in ns

FLIP-FLOPS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
dflop1	CK to Q	2.3	2.1	3.7	3.6
dflop2	CK to Q	2.4	2.0	3.9	3.6
	RB to Q	---	2.0	---	3.3
dflop3	CK to Q	2.5	2.7	3.9	3.9
	SB to Q	2.5	---	1.6	---
dflop4	CK to Q	2.5	3.0	4.0	4.1
	RB to Q	---	3.0	---	3.8
	SB to Q	2.5	---	1.6	---
dflop5	CK to Q	2.3	2.0	3.8	3.7
	CK to QB	1.9	1.8	5.0	5.2
dflop6	CK to Q	2.3	2.0	3.9	3.6
	CK to QB	2.1	2.5	5.1	5.7
	RB to Q	---	2.0	---	3.3
	RB to QB	2.1	---	1.5	---
dflop7	CK to Q	2.4	2.6	4.0	4.0
	CK to QB	2.1	1.7	5.5	5.3
	SB to Q	2.4	---	1.6	---
	SB to QB	---	1.7	---	2.9
dflop8	CK to Q	2.5	2.9	4.4	4.2
	CK to QB	2.3	2.5	5.8	5.8
	RB to Q	---	2.9	---	3.8
	RB to QB	2.3	---	1.5	---
	SB to Q	2.5	---	1.6	---
	SB to QB	---	2.5	---	3.4
rsff	RB to Q	---	2.6	---	3.7
	RB to QB	2.7	---	1.8	---
	SB to Q	2.7	---	1.8	---
	SB to QB	---	2.7	---	3.8

SLOWEST PROCESS TIMES

3 ns inputs : half load : nominal temperature : all times in ns

SIGNAL CONDITIONERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
buf1	IN to OUT	1.9	1.9	3.0	3.1
	IN to OUTB	2.3	2.1	1.6	1.7
buf2	IN to OUT	2.0	1.9	3.0	3.2
	IN to OUTB	2.6	2.1	1.7	1.7
buf3	IN to OUT	1.8	1.6	1.9	2.1
buf4	IN to OUT	1.8	1.6	1.9	2.1
tri1	IN to OUT	1.5	1.5	2.0	2.2
	EN to OUT	1.5	1.5	1.4	1.9
tri2	IN to OUT	1.8	1.5	2.4	2.3
	EN to OUT	1.8	1.5	1.7	2.0
tri3	IN to OUT	1.5	1.5	2.0	2.2
	ENB to OUT	1.5	1.5	2.0	1.8
tri4	IN to OUT	1.8	1.5	2.4	2.3
	ENB to OUT	1.8	1.5	2.2	1.9

MUXES AND DECODERS

Cell name	Condition	T_{lh}	T_{hl}	T_{plh}	T_{phl}
mux1	A to OUT	1.6	1.4	2.3	2.3
	B to OUT	1.6	1.4	2.3	2.3
	S to OUT	1.6	1.4	2.9	2.9